

Integrated circuits

Part 8

May 1982

Analogue circuits

signetics

Analog Data Manual 1982

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PREFACE

The Analog Division, one of ten Signetics divisions, is a major supplier of a broad line of Analog integrated circuits ranging from proprietary high performance original designs to many of the more popular industry standard devices and custom designs.

The 1982 Analog Data Manual provides complete technical data on Signetics Analog Division's full line of standard linear, consumer and data conversion integrated circuit products.

Employing Signetics high quality processing and screening standards, the Analog Division is dedicated to providing high quality analog products to our worldwide customers. Our full product line addresses the needs of the EDP, Automotive, Military, Industrial, Consumer and Communication markets.

Our products include a line of wide performance operational and video amplifiers, timers, comparators, A/D and D/A converters, sample/holds, radio and audio circuits, computer and display interface circuits, phase-locked loops, power controllers and transistor arrays.

A few of the more popular original Signetics analog product designs in this data manual include the NE555 timer, NE5534 low noise op amp, NE592 video amplifier, 5018 and 5020 D/A converters, the 5036 and 5037 A/D converters, and the Dolby circuits, the NE648, NE649 and NE650.

Helpful selection and cross reference guides are included to help the designer search for the correct devices. In addition, a packaging section and hi-rel screening for MIL-STD 38510 devices are included. Contact the Signetics sales office, representative or distributor nearest you for further assistance.

Although every attempt has been made to insure the accuracy of the information in this manual, Signetics assumes no liability for inadvertent errors.

Your suggestions for improvement in further editions are welcome.

Signetics Analog Marketing

PRODUCT DELETIONS/ADDITIONS

DELETIONS

NE5007/5008/SE5008¹	8-Bit High Speed Multiplying D/A Converter
NE/SE5009¹	8-Bit High Speed Multiplying D/A Converter
NE5522	Universal Analog Controller
NE/SE5553/5554	Dual Polarity Regulator
SD210/211/212/213/ 214/215	D-MOS FET Switch N-Channel Enhancement
SD300/303/304	D-MOS FET Dual Gate N-Channel Enhancement
SD305/306	D-MOS FET Dual Gate N-Channel Enhancement
SD5000/5001/5002	D-MOS FET Quad Analog Switch Arrays and Multiplexers
75S107	High Speed Dual Line Receiver
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75S207	High Speed Dual Sense Amplifier for MOS Memories
75S208	High Speed Dual Sense Amplifier for MOS Memories

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ORDERING INFORMATION

ORDERING INFORMATION

Signetics' Analog integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

Minimum Factory Order:

Commercial Product:
 \$1000 per order
 \$250 per line item per order

Military Product:
 \$250 per line item per order

Table 1 provides part number information concerning for both Signetics originated products and industry standard products.

Table 2 is a cross reference of both the old and new package suffixes for all presently existing types, while Table 3 and 4 provide appropriate explanations on the various prefixes employed in the part number descriptions.

As noted in Table 3, Signetics defines device operating temperature range by the appropriate prefix. It should be noted however, that devices with a SE prefix (-55°C to +125°C) indicates only its operating temperature range and *not* its military qualification status. The military qualification status of any analog product can be determined by either looking in the Military Section in this manual and/or contacting your local sales office.

Table 1 PART NUMBER DESCRIPTION

PART NUMBER	CROSS REF PART NO.	PRODUCT FAMILY	PRODUCT DESCRIPTION
NE5534N μA741C	LM741CJ	ANA ANA	Low Noise OP-AMP General Purpose OP-AMP

Diagram illustrating the breakdown of the part number NE5534N μA741C:

- NE5534N: Device Family and Temperature Range Prefix for Industry Standard and Signetics Originated Products—See Table 2.
- μA741C: Device Number and Temperature Range Suffix
- Package Type—See Table 1
- Product Family: ANA (Analog Products)
- Product Description: Low Noise OP-AMP, General Purpose OP-AMP

Product Family Legend:

- ECL Emitter Coupled Logic
- DTL Diode Transistor Logic
- ANA Analog Products
- MOS Metal Oxide Silicon
- BIM Bipolar Memory Products
- MIL Military Products
- TTL Transistor Logic
- ML2 Military Products

Table 2 PACKAGE DESCRIPTIONS

SUFFIX		PACKAGE DESCRIPTION ²
Old	New	
A,AA	N	14-lead plastic DIL
A	N-14	14-lead plastic DIL (Selected Analog products only)
B,BA	N	16-lead plastic DIL
-	D	Microminiature package (SO)
F	F	14, 16, 18, 22 and 24-lead ceramic (Cerdip) DIL
I,IK	I	14, 16, 18, 22, 28 and 4-lead ceramic DIL
K	H	10-lead TO-100
L	H	10-lead high-profile TO-100 can
NA,NX	N	24-lead plastic DIL
Q,R	Q	10, 14, 16 and 24-lead ceramic flat
T,TA	H	8-lead TO-99
U	U	SIL Plastic power
V	N	8-lead plastic DIL
W,WJ	W	10, 14, 16 and 24-lead ceramic (Cerpac) flat
XA	N	18-lead plastic DIL
XC	N	20-lead plastic DIL
XC	N	22-lead plastic DIL
XL,XF	N	28-lead plastic DIL

Table 3 DEVICE TEMPERATURE

PREFIX	DEVICE TEMPERATURE RANGE
N-	0° to +70°C
S-	-55° to +125°C
NE-	0° to +70°C
SE-	-55° to +125°C
SA	-40° to +85°C
SU	-25° to +85°C

Table 4 FAMILY PREFIX

PREFIX	DEVICE FAMILY
CA	Linear Industry Standard
DS	Linear Industry Standard
JB	Mil Rel—Jan Qualified—Old Designator
JM	Mil Rel—Jan Qualified—New Designator
LH	Linear Industry Standard
LM	Linear Industry Standard
M	Mil Rel—Jan Processed
MC	Linear Industry Standard
SD	Linear DMOS
μA	Linear Industry Standard
ULN	Linear Industry Standard

PRODUCT STATUS DEFINITIONS

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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SIGNETICS ANALOG SELECTOR GUIDE

OPERATIONAL AMPLIFIERS

DEVICE	COM- PLEXITY	TEMP. RANGE	MAX. INPUT VOLTAGE		MAX. INPUT CURRENT	MIN. A VOL. (V/mV)	TYP. BW Av = 1 (MHz)	TYP. SLEW RATE (V/μs)	DIFF. INP. VOLT (V)	TYP. COMMON MODE REJ. VOLT.		TYP. PSRR (dB)	SUPPLY VOLT. TYP.		OUTPUT CURR. (mA)	MAX. SUPPLY CURR. (mA)	MIN. OUTPUT VOLT. SWING(V)	INT. COMPEN- SATION	INPUT NOISE VOLT. (N-Hz)
			Offset (mV)	Drift (μV/°C)						Ratio (dB)	Range (V)		Min. (V)	Max. (V)					
NE536	Sing.	Ind.	30	30	5pA	25	1.0	6.0	±30	80	±11	86	±6	±20	5.0	8.0	±12	yes	
SU536	Sing.	Ext.	30	20	5pA	50	1.0	±30	±30	80	±11	86	±6	±18	5.0	5.5	±12	yes	
NE530	Sing.	Ind.	6.0	6.0	80	200	3.0	±30	±30	90	±13	70	±15	±18	25	3.0	±12	yes	
SE530	Sing.	Ind.	3.0	15	20	100	3.0	±30	±30	90	±13	70	±15	±18	25	3.0	±12	yes	
SE538	Sing.	Mil.	3.0	15	20	100	6.0	±30	±30	90	±13	70	±15	±22	3.6	3.6	±12	yes	
NE538	Sing.	Ind.	6.0	6.0	80	200	6.0	±30	±30	90	±13	70	±15	±18	25	2.2	±12	yes	
SE534/A	Sing.	Ext.	4.0	300	1500	30	10.0	±5	±100	100	±13	100	±3	±22	38	6.5	±12	yes	4.5
SE534/A	Sing.	Mil.	3.0	300	1500	25	10.0	±5	±100	100	±13	100	±3	±22	38	9.0	±12	yes	4.5
μA740C	Sing.	Ind.	30	0.06	10.0	500	1.0	±30	±30	80	±12	80	±5	±22	5.0	8.0	±12	yes	
μA741	Sing.	Mil.	6.0	500	1500	25	1.0	±30	±30	90	±13	100	±3	±22	5.0	2.5	±12	yes	
μA741C	Sing.	Ind.	7.5	300	800	15	1.0	±30	±30	90	±13	100	±3	±18	5.0	2.8	±12	yes	
μA748	Sing.	Mil.	6.0	500	1500	25	1.0	±30	±30	90	±13	100	±3	±22	5.0	2.8	±12	no	
μA748C	Sing.	Ind.	7.5	300	800	25	1.0	±30	±30	90	±13	90	±3	±18	5.0	2.8	±12	no	
LM158	Dual	Mil.	7.0	100	300	25	1.0	32	70	VS - 1.5	100	3	30	40	2.0	VS - 2	yes		
LM258	Dual	Ext.	9.0	7	150	500	1.0	32	65	VS - 1.5	100	3	30	40	2.0	VS - 2	yes		
LM358	Dual	Ind.	9.0	7	150	500	1.0	32	65	VS - 1.5	100	3	30	40	2.0	VS - 2	yes		
MC1458	Dual	Ind.	7.5	300	800	15	1.0	±30	±30	90	±13	90	±3	±18	5.0	5.6	±12	yes	
MC1588	Dual	Mil.	6.0	500	1500	25	1.0	±30	±30	90	±13	90	±3	±22	5.0	5.0	±12	yes	
SA1458	Dual	Ext.	7.5	150	500	15	1.0	±30	±30	90	±13	90	±3	±18	5.0	5.0	±12	yes	
NE532	Dual	Ind.	7.5	7	150	500	1.0	±30	±30	70	VS - 1.5	100	3	30	40	1.2	VS - 2	yes	
SA532	Dual	Ext.	7.5	150	500	15	1.0	±30	±30	70	VS - 1.5	100	3	30	40	1.2	VS - 2	yes	
SE532	Dual	Mil.	7.0	7	300	25	1.0	32	70	VS - 1.5	100	3	30	40	1.2	VS - 2	yes		
μA747	Dual	Mil.	6.0	500	1500	25	1.0	±30	±30	90	±13	90	±3	±22	5.0	3.3	±12	yes	
μA747C	Dual	Ind.	7.5	300	800	15	1.0	±30	±30	90	±13	90	±3	±18	5.0	3.3	±12	yes	
SE535	Dual	Mil.	3.0	15	20	100	25	1.0	±30	90	±13	70	±3	±22	5.0	3.3	±12	yes	
NE535	Dual	Ind.	6.0	80	200	25	1.0	±30	±30	90	±13	70	±3	±18	5.0	2.0	±12	yes	
LM124	Quad	Mil.	7.0	7	100	300	25	1.0	32	85	VS - 1.5	100	3	30	40	2.0	VS - 2	yes	
LM224	Quad	Ext.	9.0	7	150	500	15	1.0	32	85	VS - 1.5	100	3	30	40	2.0	VS - 2	yes	
LM324	Quad	Ind.	9.0	7	150	500	15	1.0	32	85	VS - 1.5	100	3	30	40	2.0	VS - 2	yes	
SA534	Quad	Ext.	9.0	7	150	500	15	1.0	32	85	VS - 1.5	100	3	30	40	2.0	VS - 2	yes	
LM2902	Quad	Ext.	15.0	7	200	1000	15	1.0	26	85	VS - 1.5	100	3	26	40	2.0	VS - 2	yes	
SE538	Dual	Mil.	3.0	15	20	100	25	6.0	±30	90	±13	70	±15	±22	25	3.6	±12	yes	6
NE538	Dual	Ind.	6.0	80	200	200	6.0	±30	±30	90	±13	70	±15	±18	25	2.2	±12	yes	
SE530	Dual	Mil.	3.0	15	20	100	25	3.0	±30	90	±13	70	±3	±22	3.6	3.6	±13	yes	
NE530	Dual	Ind.	6.0	80	200	200	3.0	±30	±30	90	±13	70	±3	±18	2.2	2.2	±13	yes	
NE532/A	Dual	Ind.	5.0	200	1000	10	10	9	±5	100	±13	80	±5	±22	16	16	±15	yes	
NE533/A	Dual	Ind.	5.0	400	2000	15	10	13	±5	100	±13	80	±5	±22	8	8	±15	yes	4.5
NE532	Dual	Ind.	1.5	8	200	200	1	1	±5	100	±13	100	±5	±16	5.5	5.5	±8	yes	30
NE5514	Quad	Ind.	1.5	8	8	25	1	1	±5	100	±13	100	±5	±16	12	12	±8	yes	30
NE4558	Dual	Ind.	2.0	200	500	500	0.5	0.5	±5	100	±13	100	±5	±18	±10	±10	±10	yes	
MC3403	Quad	Ind.	10	75	500	500	0.6	0.6	±5	90	±13	30	±5	±18	±18	±18	±18	yes	

NOTES
 1. Military: -55°C to +125°C
 Extended: -25°C to +85°C
 Industrial: 0°C to +70°C
 2. Specifications guaranteed over full temperature range unless otherwise indicated by the following marks:
 ● Typical over full temperature range ▲ Guaranteed at 25°C ■ Typical at 25°C

SIGNETICS ANALOG SELECTOR GUIDE



COMPARATORS

DEVICE	COM- PLEXITY	TEMP. RANGE*	MAX. INP. OFFSET VOLT. (mV)	MAX. INP. CURRENT		SUPPLY VOLTAGE (V)	RESPONSE TIME (TYP.) (ns)	COMMON MODE VOLTAGE RANGE (V)	OUTPUT VOLT.		OUTPUT STRUC- TURE	VOLT. GAIN (TYP.) (V/mV)	TTL FANOUT	MAX. DIFF. INPUT VOLT. (V)	PACK- AGES
				Bias μA	Offset μA				V _{OL} Max. (V)	V _{OH} Min. (V)					
LM111 ¹	Single	M	4.00	0.15	0.02	± 15	200	± 14	0.4		O.C.	200	5	± 30	F,T
LM211	Single	E	4.00	0.15	0.02	to	200	± 14		O.C.	200	5	± 30	F,N,T	
LM311	Single	I	10.0	0.30	0.07	+ 5 and GND	200	± 14	0.4		O.C.	200	5	± 30	F,N,T
NE527 ²	Single	I	10.0	4.00	1.00	± 5 to ± 15	16	± 6	0.5	2.7	TTL	5	± 5	F,K,N	
SE527	Single	M	6.00	4.00	1.00	and GND	16	± 6	0.5	2.5	TTL	5	± 5	F,K	
NE529 ²	Single	I	10.0	50.0	15.0	± 5 to ± 15	12	± 6	0.5	2.7	TTL	5	± 5	F,K,N	
SE529	Single	M	6.00	36.0	9.00	and GND	12	± 6	0.5	2.5	TTL	5	± 5	F,K	
LM119 ¹	Dual	M	7.00	1.00	0.10	± 15	80	± 13	0.6		O.C.	40	2	± 5	K,F
LM219	Dual	E	7.00	1.00	0.10	to	80	± 13	0.6		O.C.	40	2	± 5	K,F
LM319	Dual	I	10.0	1.20	0.30	± 5 and GND	80	± 13	0.6		O.C.	40	2	± 5	F,K,N
LM193 ³	Dual	M	9.00	0.30	0.10	± 1 to ± 18	1300	0 to V _S -2	0.7		O.C.	200	2	36	T
LM293	Dual	E	9.00	0.40	0.15	or	1300	0 to V _S -2	0.7		O.C.	200	2	36	N,T
LM393	Dual	I	9.00	0.40	0.15	+2 to +36 GND	1300	0 to V _S -2	0.7		O.C.	200	2	36	N,T
LM2903	Dual	E	15.0	0.50	0.20		1300	0 to V _S -2	0.7		O.C.	100	2	36	N,T
NE521 ⁴	Dual	I	10.0	40.0	12.0	+5, -5 GND	7	± 3	0.5	2.7	TTL	12	± 6	F,N	
NE522	Dual	I	10.0	40.0	12.0	+5, -5, GND	9	± 3	0.5		O.C.	12	± 6	F,N	
LM139 ³	Quad	M	9.00	0.30	0.10		1300	0 to V _S -2	0.7		O.C.	200	2	36	F,N
LM239	Quad	E	9.00	0.40	0.15	± 1 to ± 18 or	1300	0 to V _S -2	0.7		O.C.	200	2	36	F,N
LM339	Quad	I	9.00	0.40	0.15	+ 2 to + 36	1300	0 to V _S -2	0.7		O.C.	200	2	36	F,N
LM2901	Quad	E	15.0	0.50	0.20		1300	0 to V _S -2	0.7		O.C.	100	2	36	N
MC3302 ³	Quad	E	40.0	1.00	0.20	+2 to +28 GND	2000	0 to V _S -2	0.4		O.C.	30	2	28	N

NOTES

1. With strobe; will work from single supply
2. Complementary output gates with individual strobes.
3. Will operate from single or dual supplies.
4. Ultra high speed

*Temperature Range
 E = Extended
 I = Industrial
 M = Military

D/A CONVERTERS

PRODUCT	# BITS	ACC. %	OUTPUT			INT. REF.	INT. LATCH	PACKAGE		TEMPERATURE RANGE		RELIABILITY	
			V	I	T			N	F	Com'l.	Mil.	SURE II	SUPR II
MC1408-6	8	.78		X				X	X	X		X	
MC1408-7	8	.39		X				X	X	X		X	X
MC1408-8	8	.19		X				X	X	X		X	X
MC1508-8	8	.19		X					X		X	X	X
DAC-08C	8	.39		X	X			X	X	X		X	X
DAC-08E	8	.19		X	X			X	X	X		X	X
DAC-08H	8	.1		X	X			X	X	X		X	X
DAC-08	8	.19		X	X				X		X	X	X
DAC-08A	8	.1		X	X				X		X	X	X
NE5018	8	.19	X			X	X	X	X	X		X	X
NE5019	8	.1	X			X	X	X	X	X		X	X
SE5018	8	.19	X			X	X		X		X	X	X
SE5019	8	.1	X			X	X		X		X	X	X
NE5118	8	.19		X		X	X	X	X	X		X	
NE5119	8	.1		X		X	X	X	X	X		X	
SE5118	8	.19		X		X	X		X		X	X	
SE5119	8	.1		X		X	X		X		X	X	
NE5020	10	.1	X			X	X	X	X	X		X	

ANALOG CROSS REFERENCE GUIDE

ANALOG CROSS REFERENCE							
Manufacturer	T.I.	AMD	FAIRCHILD	INTEL	MOTOROLA	NATIONAL	SIGNETICS
TEMPERATURE RANGE CROSS REFERENCE							
Commercial	72, 74, 75	C	C	—	14, 34, 86	3, 86, 88	NE
Military	52, 54, 55	M	M	M	15, 35, 96	1, 96, 78	SE
PACKAGE CROSS REFERENCE							
Hermetic DIP	J	D	D	C, D	L	D	F-FE
Molded DIP	N	P	P	P	P ₂	N	N
Mini-Molded DIP	P	T	T	—	P ₁	N	N
Metal Can	L	H	H	—	G, R	H	H
Small Outline (SO)	—	—	—	—	D	—	D

PART NUMBER CROSS REFERENCES

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
AD741CN	μA741CN	CA741CE	μA741CN	LM239N	LM239N
AD559JD	MC1408-8F	CA741CF	μA741CFE	LM258JG	LM258FE
AD559K	MC1408-8F	CA741F	μA741FE	LM258P	LM258N
AD559KD	MC1408-8F	CA747CF	μA747CF	LM293P	LM293N
AD559S	MC1508-8F	CA747F	μA747F	LM301AJG	LM301AFE
AD559SD	MC1508-8F	CA748CE	μA748CN	LM311D	LM311F
AM555DC	NE555F	CA748CF	μA748CF	LM311J	LM311F
AM555DM	SE555F	CA748F	μA748F	LM311J-14	LM311F
AM555HC	NE555H	CA1458E	MC1458N	LM311JG	LM311FE
AM555HM	SE555H	CA1458F	MC1458FE	LM311N	LM311N
AM555TC	NE555N	CA3081E	CA3081N	LM311P	LM311N
AM723DC	μA723CF	CA3082E	CA3082N	LM319D	LM319F
AM723DM	μA723F	CA3183E	CA3183N	LM319J	LM319F
AM741DC	μA741CFE	DAC-08A	DAC-08A/SE5009	LM319N	LM319N
AM741DM	μA741FE	DAC-08	DAC-08/SE5008	LM324J	LM324F
AM747DC	μA747CF	DAC-08H	DAC-08H/NE5009	LM324N	LM324N
AM747DM	μA747F	DAC-08E	DAC-08E/NE5008	LM339J	LM339F
AM748DC	μA748CF	DAC-08C	DAC-08C/NE5007	LM339N	LM339N
AM748DM	μA748F	DS1488J	MC1488F	LM358H	LM358H
AMLM211D	LM211F	DS1489AJ	MC1489AF	LM358JG	LM358FE
AMLM311D	LM311F	DS1489J	MC1489F	LM358L	LM358H
CA111F	LM111F	LM111D	LM111F	LM358N	LM358N
CA124F	LM124F	LM111J	LM111F	LM358P	LM358N
CA139AF	LM139AF	LM119D	LM119F	LM361D	NE529F
CA139F	LM139F	LM119J	LM119F	LM361H	NE529H
CA211F	LM211F	LM124D	LM124F	LM361J	NE529F
CA224F	LM224F	LM124J	LM124F	LM361N	NE529N
CA239AF	LM239F	LM139D	LM139F	LM381N	LM381N
CA239F	LM239F	LM139J	LM139F	LM382N	LM382N
CA301AF	LM301AFE	LM158JG	LM158FE	LM387N	LM387N
CA311F	LM311F	LM161D	SE529F	LM393N	LM393N
CA324E	LM324N	LM161H	SE529H	LM393P	LM393N
CA324F	LM324F	LM161J	SE529F	LM555CH	NE555H
CA339E	LM339N	1LM211D	LM211F	LM555CN	NE555N
CA339F	LM339F	LM211J	LM211F	LM555H	SE555H
CA555CE	NE555N	LM219D	LM219F	LM556CD	NE556F
CA555CF	NE555F	LM219J	LM219F	LM556CJ	NE556F
CA555CT	NE555H	LM224D	LM224F	LM556CN	NE556N
CA555F	SE555F	LM224J	LM224F	LM556D	SE556F
CA555T	SE555H	LM224N	LM224N	LM556J	SE556F
CA723CE	μA723CN	LM239D	LM239F	LM565CH	NE565H
CA723E	μA723N	LM239J	LM239F	LM565CN	NE565N

ANALOG CROSS REFERENCE GUIDE

PART NUMBER CROSS REFERENCES (Continued)

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
LM565H	SE565H	MC1458SP1	NE5535N	MLM324P	LM324N
LM566CN	NE566N	MC1458U	MC1458FE	MLM339AL	LM339AF
LM567H	SE567H	MC1488L	MC1488F	MLM339AP	LM339AN
LM567CN	NE567N	MC1489AL	MC1489AF	MLM339L	LM339F
LM567H	SE567H	MC1489L	MC1489F	MLM339P	LM339N
LM723CD	μ A723CF	MC1496G	MC1496H	MLM358G	LM358H
LM723CJ	μ A723CF	MC1496L	MC1496F	MLM358P1	LM358N
LM723CN	μ A723CN	MC1496P	MC1496N	MLM358U	LM358FE
LM723D	μ A723F	MC1508L8	MC1508-8F	MLM565CP	NE565N
LM723J	μ A723F	MC1555G	SE555H	MLM2901P	LM2901N
LM723N	μ A723N	MC1555U	SE555FE	MLM2902P	SA534N
LM733CD	μ A733CF	MC1556U	MC1556FE	μ A124DM	LM124F
LM733CJ	μ A733CF	MC1558JG	MC1558FE	μ A224DM	LM224F
LM733CN	μ A733CN	MC1558SL	SE5535F	μ A301ANC	LM301AN
LM733D	μ A733F	MC1558U	MC1558FE	μ A311TC	LM311N
LM733T	μ A733F	MC1596G	MC1596H	μ A324DC	LM324F
LM741CJ	μ A741CFE	MC1596L	MC1596F	μ A324PC	LM324N
LM741CN	μ A741CN	MC1723CL	μ A723CF	μ A339ADC	LM339AF
LM747CD	μ A747CF	MC1723CP	μ A723CN	μ A339DC	LM339F
LM747CJ	μ A747CF	MC1723L	μ A723F	μ A339PC	LM339N
LM747D	μ A747F	MC1733CL	μ A733CF	μ A555HC	NE555H
LM747J	μ A747F	MC1733CP	μ A733CN	μ A555HM	SE555H
LM748CJ	μ A748CF	MC1733L	μ A733F	μ A555TC	NE555N
LM748CN	μ A748CN	MC1741CP1	μ A741CN	μ A556DC	NE556F
LM748J	μ A748F	MC1741CU	μ A741CFE	μ A556DM	SE556F
LM1458J	MC1458FE	MC1741SCP1	NE535N	μ A556PC	NE556N
LM1458N	MC1458N	MC1741SCU	NE535FE	μ A723CJ	μ A723CF
LM1496J	MC1496F	MC1741SU	SE535FE	μ A723CN	μ A723CN
LM1496N	MC1496N	MC1741U	SE535FE	μ A723DC	μ A723CF
LM1558J	MC1558FE	MC1747CL	μ A747CF	μ A723DM	μ A723F
LM1596H	MC1596H	MC1747CP2	μ A747CN	μ A723MJ	μ A723F
LM1596J	MC1596F	MC1747L	μ A747F	μ A723PC	μ A723CN
LM2901J	LM2901F	MC1748CP1	μ A748CN	μ A733CJ	μ A733CF
LM2901N	LM2901N	MC3302L	MC3302F	μ A733CN	μ A733CN
LM2902J	SA534F	MC3302P	MC3302N	μ A733DC	μ A733CF
LM2902N	SA534N	MC3456L	NE556F	μ A733DM	μ A733F
LM2903N	LM2903N	MC3456P	NE556N	μ A733MJ	μ A733F
LM2903P	LM2903N	MC3556L	SE556F	μ A740HC	μ A740CH
MC1408L6	MC1408-6F	MLM111L	LM111F	μ A741CJG	μ A741CFE
MC1408L7	MC1408-7F	MLM111U	LM111FE	μ A741CP	μ A741CN
MC1408L8	MC1408-8F	MLM124L	LM124F	μ A741MJG	μ A741FE
MC1408P6	MC1408-6N	MLM139AL	LM139AF	μ A741TC	μ A741CN
MC1408P7	MC1408-7N	MLM139L	LM139F	μ A747CJ	μ A747CF
MC1408P8	MC1408-8N	MLM158U	LM158FE	μ A747CN	μ A747CN
MC1411P	ULN2001N	MLM211L	LM211F	μ A747DC	μ A747CF
MC1416P	ULN2004N	MLM211U	LM211FE	μ A747DM	μ A747F
MC1455G	NE555H	MLM224L	LM224F	μ A747MJ	μ A747F
MC1455P1	NE555N	MLM224P	LM224N	μ A747PC	μ A747CN
MC1455U	NE555FE	MLM239AL	LM239AF	μ A748CJ	μ A748CF
MC1456CP1	MC1456N	MLM239AP	LM239AN	μ A748CP	μ A748CN
MC1456CU	MC1456FE	MLM239L	LM239F	μ A748DC	μ A748CF
MC1456P1	MC1456N	MLM239P	LM239N	μ A748DM	μ A748F
MC1456U	MC1456FE	MLM258P1	LM258N	μ A748MJ	μ A748F
MC1458CL	MC1458F	MLM258U	LM258FE	μ A748TC	μ A748CN
MC1458CP1	MC1458N	MLM301AP1	LM301AN	μ A796HC	MC1496H
MC1458CU	MC1458FE	MLM301AU	LM301AFE	μ A0802DC-1	MC1408-8F
MC1458JG	MC1458FE	MLM311L	LM311F	μ A0802DC-2	MC1408-7F
MC1458P	MC1458N	MLM311P1	LM311N	μ A0802DC-3	MC1408-6F
MC1458P1	MC1458N	MLM311U	LM311FE	μ A0802DM-1	MC1508-8F
MC1458SL	NE5535F	MLM324L	LM324F	μ A0802PC-1	MC1408-8N

ANALOG CROSS REFERENCE GUIDE

PART NUMBER CROSS REFERENCES (Continued)

TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT	TYPE TO BE REPLACED	SIGNETICS REPLACEMENT
μ A0802PC-2	MC1408-7N	SN72311J	LM311F	733CJ	μ A733CN
μ A0802PC-3	MC1408-6N	SN72311P	LM311N	747BL	μ A747F
μ A1458TC	MC1458N	SN72555L	NE555H	747CJ	μ A747CN
μ A2901PC	LM2901N	SN72555P	NE555N	747CL	μ A747CF
μ A2902PC	SA534N	SN72558P	MC1458N	748BL	μ A748F
NE555JG	NE555FE	SN72723N	μ A723CN	748CL	μ A748CF
NE555L	NE555H	SN72733J	μ A733CF	1458CP	MC1458N
NE555P	NE555N	SN72733N	μ A733CN	1458P	MC1458N
NE592G	NE592H	SN72741P	μ A741CN	2740CE	μ A740CH
NE592L	NE592F	SN72747J	μ A747CF	9665DC	ULN2001F
RC723D	μ A723CF	SN72747N	μ A747CN	0665PC	ULN2001N
RC733D	μ A733CF	SN72748J	μ A748CF	μ A3089N	CA3089N
RC741DN	μ A741CN	SN72748P	μ A748CN	μ A3089	CA3089N
RC747D	μ A747CF	SN72771N	MC1456N	μ A760HM	NE527H
RC1458DN	MC1458N	SN75188J	MC1488F	μ A760DC	NE527N
RC1488DC	MC1488F	SN75188N	MC1488N	μ A7898TC	NE532N
RC1489ADC	MC1489AF	SN75189AT	MC1489AF	μ A740HM	NE536H
RC1489DC	MC1489F	SN75189AN	MC1489AN	μ A556PC	NE556N
SE555JG	SE555FE	SN75189J	MC1489F	μ A0801	DAC-08N
SE555L	SE555H	SN75189N	MC1489N	μ A0801A	DAC-08AN
SE592G	SE592H	TBB0748B	μ A748CN	μ A758PC	μ A758N
SE592L	SE592F	TBB1458B	MC1458N	μ A739PC	LM387N
SFC2301ADC	LM301AN	TDB0555	NE555H	μ A739PC	LM382N
SFC2741DC	μ A741CN	TDB0555B	NE555N	μ A796PC	MC1496N
SFC2741EC	μ A741CN	TDB0556A	NE556N	μ A760HC	NE529N
SFC2741EM	μ A741N	TDB0723A	μ A723CN	SN7512L	μ A733CH
SFC2748DC	μ A748CN	TDC0555	SE555H	SN7512N	μ A733N
SN52555L	SE555H	ULN2001A	ULN2001N	SN76689N	CA3089N
SN52723J	μ A723F	ULN2003A	ULN2003N	ULN2210A	μ A758N
SN52733J	μ A733F	ULN2004A	ULN2004N	ULN2244	μ A758N
SN52747J	μ A747F	556CJ	NE556CN	μ A740HC	μ A740CH
SN52748J	μ A748F	723CT	μ A723CN		
SN72301AP	LM301AN	723CL	μ A723CF		

Section 2 Quality, Reliability and Assurance

QUALITY, RELIABILITY AND ASSURANCE

QUALITY AND RELIABILITY

Quality and reliability are two important measures of a product's merit. Quality is a measure of an integrated circuit's conformance to agreed-upon criteria at a given time, while Reliability is a measure of the circuit's ability to continue to conform over a period of time. The Signetics SUPR II Program has been designed to upgrade the basic product quality through the use of more rigorous screening criteria at the critical process steps. These additional screens constitute the Level A portion of the Program. A burn-in option is available for those users requiring enhanced reliability performance, and this option is designated as Level B.

Quality

The quality of an integrated circuit is appraised by the user based on the ability of the circuit to meet the specified electrical criteria and external visual appearance. The SUPR II Program focuses on supplying to the user a product that has a high probability of meeting the user's needs through the sampling plans defined in MIL-STD-105D and the quality levels (AQL's) stated in Table II. Many of the inspection methods at critical process steps are now based on MIL-STD-883 criteria in order to build, rather than test, quality into the product.

Reliability

System performance over a period of time is the user's measure of an integrated circuit's reliability. The SUPR II Program improves system reliability by building quality into the product via additional manufacturing inspections and the offering of a burn-in screen. In addition to the SUPR II Program, Signetics performs periodic reliability testing via the SUREIII/883A Program to assure continuing uniformity and long-term reliability of all product lines. This data base is available upon request as is the ten-year reliability summary, Signetics Product Reliability Report, R-363.

How Do Integrated Circuit Failures Occur?

Results from the Signetics Failure Analysis Lab over a three-year period on product returned from board checkout, system checkout, field usage and accelerated life testing are graphically presented in Figure 1. Under typical system operating conditions, random manufacturing defects, as outlined in Table 1, are the primary cause of true device failure. Also shown in Table 1 are the process controls that have been added via the SUPR II Program to minimize these defects prior to shipment to the cus-

tomers. The device failure models are categorized as:

Half of the devices analyzed were found to be electrically good. They are attributed to being "false pulls" that occur during normal troubleshooting at the board and system levels.

Devices damaged by electrical over-stress account for 25% of the failures. Typical causes for electrical over-stress are incorrect board insertion, board shorts between device pins, power supply transients, and poor handling techniques.

The remaining 25% were verified to be true failures which occurred as a result of an in-process manufacturing defect or test escape.

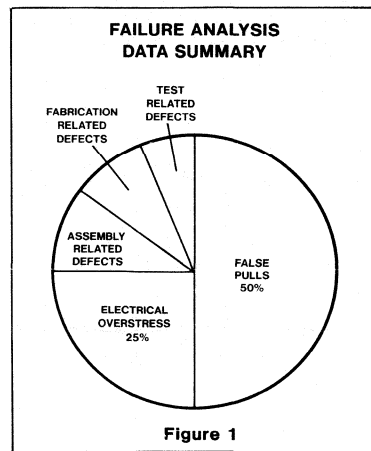
SIGNETICS SUPR II LEVEL A

Improved Quality Benefits

From the user's point of view, improved integrated circuit quality from the supplier means a lower cost of ownership. This cost saving can be effected through the reduction or elimination of involved incoming inspection testing, reduced PC board rework, simplified system checkout, reduced in-line inventories, and less complicated part tracking by Purchasing Management.

The SUPR II Program is Corporate in scope and covers Logic (Standard TTL, Schottky TTL, Low Power Schottky TTL, ECL, 8T Interface), Analog (Industrial, Consumer, Interface), Bipolar Memories (RAM's, ROM's, PROM's), and MOS Memories (RAM's, ROM's, Shift Registers), All package options are also available.

The SUPR II flow is detailed in Figure 5, including the test methods and Quality acceptance levels (Table 2 provides the electrical/mechanical finished product AQL's). Highlights of the flow are visual in-



spectations, thermal shock preconditioning, hermeticity, and burn-in, all based on MIL-STD-883 criteria.

A good example of the savings which can be achieved by purchasing tighter inspection levels is given in Figure 2. Here we are comparing the various levels of inspection (AQL's) available for device functionality and its impact on the number of PC boards which must be reworked during system manufacturing. Using the standard commercial AQL in functionality of 1.0%, at 120 integrated circuit packages per board, typically more than 90% of boards will require rework. At 0.15% AQL, rework is reduced to 25%, and at 0.1%, typically only 12% rework is required.

SIGNETICS SUPR II LEVEL B

Infant Mortality Failures

Failure rates are most severe during the first few months of operating life. This is known as the "infant mortality" phase. A system

FAILURE MECHANISMS	CAUSES	SUPR II CONTROL
Die Fabrication Related	Metalization Oxide Defects Mechanical Scratches Contamination	SEM Monitor Visual Stabilization Bake Burn-In
Assembly Related	Bonding, Wire, Package and Seal Defects	Preseal Visual Thermal Shock Stabilization Bake Hermeticity Hot-Rail Testing
Test Related	Test Escapes	Tightened AQL Guarantees High Temperature Testing

Table 1

QUALITY, RELIABILITY AND ASSURANCE

AQL LEVELS ON FUNCTIONALITY VERSUS BOARD REWORK RATES

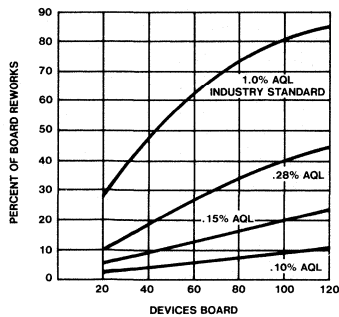


Figure 2

manufacturer has various options to solve problems arising from infant failures. He can ship his system to the end customer and repair field failures as they occur. He can operate the system in-house for this period and repair failures. Or he can purchase devices which have already been preconditioned to eliminate the early failures. Each customer must choose the most cost-effective method for his particular business. A considerable number of the reliability defects which cause early failures are elimi-

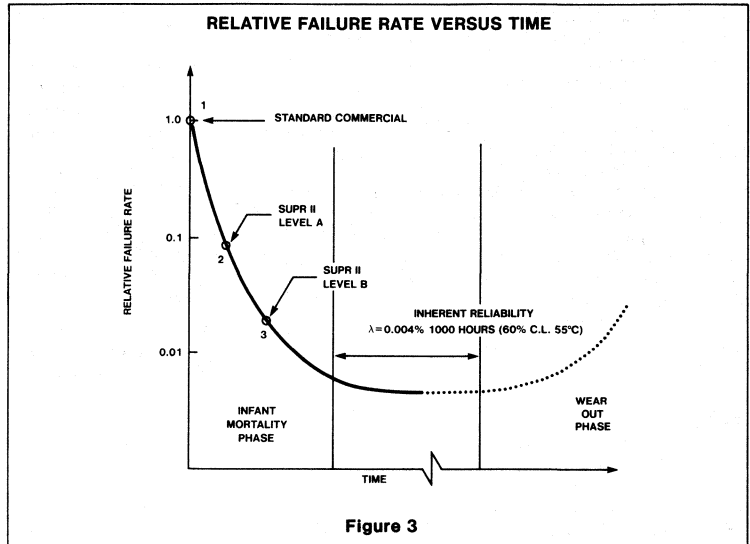


Figure 3

nated by the manufacturing control and preconditioning steps of SUPR II Level A processing. More persistent defects can be removed by the use of "burn-in" techniques. The "burn-in" processing of SUPR II Level B effectively allows the system manufacturer to ship his equipment at Point 3 on the failure rate curve in Figure 3.

Burn-In Conditions

MIL-STD-883A, Method 1015 describes a number of different conditions for integrated circuit burn-in. For SUPR II Level B, Signetics has selected Condition F. This is the accelerated burn-in method derived from MIL-STD-883A, utilizing a high temperature reversed bias condition. This bias scheme is preferred for infant mortality screening, while operating conditions are generally utilized for internal reliability programs oriented toward generating MTBF data for the system designer.

Integrated Burn-In Flow

Signetics SUPR II Level B burn-in is performed to provide reliability assurance equivalent to a 168-hour/125°C screen. This process has been integrated into the standard manufacturing flow to provide the customer with the most cost effective screen and significantly reduced delivery times.

ANALOG AQL GUARANTEES

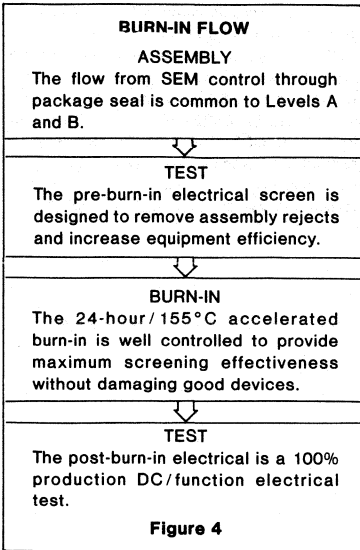
		ANALOG AQL GUARANTEES	
		Standard	SUPR IIA/B
HOT OPENS	100°C	0.015	0.015
DC PARAMETRIC/FUNCTIONAL	25°C	0.25	0.10
DC PARAMETRIC/FUNCTIONAL	MIN./MAX. RATED TEMP. (Combined)	0.40	0.25
AC PARAMETRIC	25°C	0.40	0.40
MECHANICAL	MAJOR/MINOR (Combined)	0.40	0.40
SEAL TESTS (CERAMIC/METAL CANS ONLY)	FINE LEAK 5 x 8 ⁻³ cc/s GROSS LEAK (Combined)	0.40	0.40

NOTE

1. To insure AQL levels tighter than 0.65% on D.C. parameters usually requires continual correlation of test equipment between customer and vendor to avoid test interpretation problems. If the objective is to reduce system rework costs, functional operation of a device (does it switch or toggle in the system) is often more critical than the absolute value of a parameter. For this reason SUPR II focuses on tightened AQLs on functionality.

Table 2 SUPR II AQL GUARANTEE

QUALITY, RELIABILITY AND ASSURANCE



Marking Format

Product processed to the SUPR II manufacturing flow can be identified by an SA for Level A, and an SB for the Level B burn-in option.

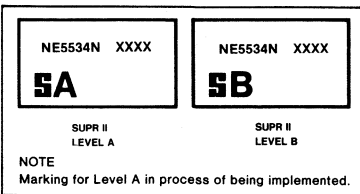
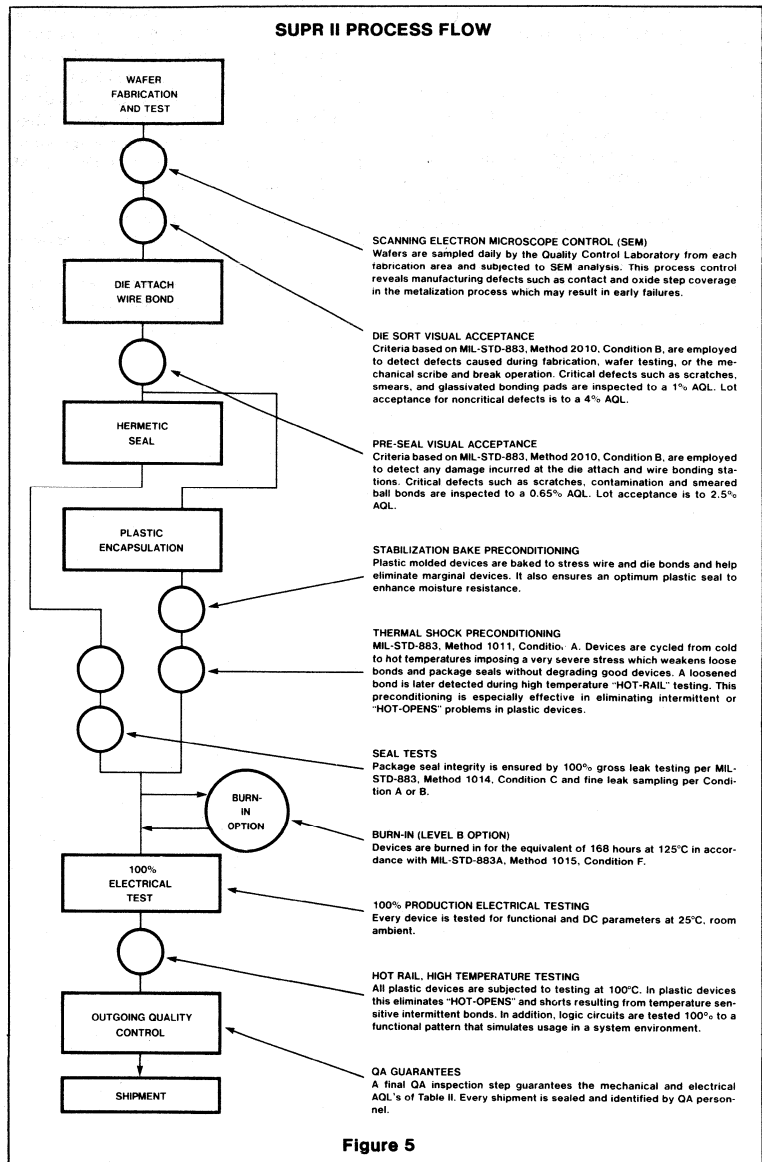


Figure 5 shows the generalized process flow for all Signetics integrated circuits purchased to the SUPR II program. Each product group (Analog, Bipolar Memory, Logic, and MOS) may follow slightly different procedures dictated by the specific device characteristics.



QUALITY, RELIABILITY AND ASSURANCE

SURE III/883B RELIABILITY PROGRAM

Definition

Signetics is recognized as a manufacturer of reliable integrated circuits. Signetics realized long ago the need for a comprehensive reliability program to provide timely data representative of the entire Signetics product line. Thus the establishment of a Systematic and Uniform Reliability Evaluation program, known as SURE, which provides this data in a manner unique to the industry. Furthermore, this program is provided at no cost to customers.

The SURE Program is a Signetics in-house Qualification Test Program which has been in existence since 1963. The SURE Program is designed to monitor the continuing uniformity of all Signetics products and to demonstrate via periodic qualifications that Signetics products meet or exceed the stringent long-term reliability requirements of their intended applications.

The SURE Program is reviewed and modified annually to incorporate appropriate changes in military microelectronic test programs, products and demonstrated product capabilities, and market requirements. The

1978 SUREIII/883B Reliability Program contains minor changes to the 1975 SURE II/883A Program, most significant of which is the inclusion of recent changes in military microelectronic test programs (i.e., inclusion of MIL-SD-883B, Method 5005.4 and MIL-M-3851OD). The SURE III/883B Program continues to incorporate additional environmental tests to fulfill the need for special reliability assurance of plastic products.

Section 3 Operational Amplifiers

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Section 3 — Operational Amplifiers

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OPERATIONAL AMPLIFIERS—SYMBOLS AND DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} (-V_{CC})

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Bandwidth

The frequency at which the gain is down 3dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

Average Input Offset Current Temperature Coefficient (TC_{I_{OS}})

The change in input offset current divided by the change to ambient temperature producing it.

Average Input Offset Voltage Temperature Coefficient (TCV_{OS})

The change in input offset voltage divided by the change in ambient temperature producing it.

Common Mode Input Resistance

The resistance looking into both inputs, with inputs tied together.

Common Mode Rejection Ratio (CMRR)

The ratio of the change of input offset voltage to the input common mode voltage change producing it.

Full Power Bandwidth

The maximum frequency at which the full sinewave output might be obtained.

Input Bias Current (I_B)

The average of the two input currents at zero output voltage. In some cases, the input current is measured for either input independently.

Input Capacitance

The capacitance looking into either input terminal with the other grounded.

Input Current

The current into an input terminal.

Input Noise Voltage

The square root of the mean square narrow-band noise voltage referred to the input.

Input Offset Current

The difference in the currents into the two input terminals with the output at zero volts.

Input Offset Voltage

That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

Input Resistance

The resistance looking into either input terminal with the other grounded.

Input Voltage Range

The range of voltages on the input terminals for which the amplifier operates within specifications. In some cases, the input offset specifications apply over the input voltage range.

Large-Signal Voltage Gain

The ratio of the maximum output voltage swing to the change in input voltage required to drive the output to this voltage.

Output Resistance

The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

Output Short-Circuit Current

The maximum output current available from the amplifier with the output shorted to ground or to either supply.

Output Voltage Swing

The peak output swing, referred to zero, that can be obtained.

Power Consumption

The dc power required to operate the amplifier with the output at zero and with the output at zero and with no load current.

Power Supply Rejection Ratio

The ratio of the change in input offset voltage to the change in supply voltages producing it.

Rise Time

The time required for an output voltage step to change from 10% to 90% of its final value.

Slew Rate

The maximum rate of change of output voltage under large signal condition.

Supply Current

The current required from the power supply to operate the amplifier with no load and the output at zero.

Temperature Stability of Voltage Gain

The maximum variation of the voltage gain over the specified temperature range.

NOTE

Refer to Section 3 of the 1979 Analog Applications Manual for an in depth explanation of Operational Amplifiers and their applications

OPERATIONAL AMPLIFIERS—SYMBOLS AND DEFINITIONS

MC1458 DUAL OPERATIONAL AMPLIFIER

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
MOTOROLA FAIRCHILD RAYTHEON N.S.C. T.I.	.8	Slew Rate	10 to 60	NE/SE { 5530 5538	Yes		
			V/μ sec	NE { 5532 5532A 5533 5533A	Yes Yes Yes Yes		
	14	Full power out	30 to 300	NE/SE { 5530 5538	Yes Yes		
			kHz	NE { 5532 5532A 5533 5533A	Yes Yes		
	45	Noise	4, 5	NE { 5532 5532A 5533 5533A	Yes Yes		
			nv/√Hz				
	6	Offset voltage	4	NE { 5532 5532A 5533 5533A	Yes Yes		
			mv				
	500	Bias current	60 to 150	NE/SE { 5530 5538	Yes Yes		
			na				
	1	Gain bandwidth	1.5 ↓ 15	NE/SE { 5530 5538	Yes Yes		
			MHz	NE { 5533 5533A 5532 5532A	Yes Yes		
	2,000	Maximum loading	600	NE { 5533 5533A 5532 5532A	Yes Yes		
			OHM				

OPERATIONAL AMPLIFIERS—SYMBOLS AND DEFINITIONS

μa741 SINGLE OPERATIONAL AMPLIFIER

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
MOTOROLA FAIRCHILD RAYTHEON N.S.C. T.I.	0.5	Slew rate	10 to 600	NE/SE { 530 538 5534 5534A	Yes Yes Yes Yes	Yes Yes	*Not pin for pin replacement.
			V/μ sec	NE 5539*			
	10	Full power out	300 to 350,000	NE/SE { 530 538 5534 5534A	Yes Yes Yes Yes	Yes Yes	
			kHz	NE 5539*			
	45	Noise	4, 5	NE/SE { 5534 5534A	Yes Yes	Yes Yes	
			nv/√Hz				
	5	Offset voltage	4	NE/SE { 5534 5534A	Yes Yes	Yes Yes	
			mv				
	500	Bias current	60 to 150	NE/SE { 530 538	Yes Yes		
			na				
	1	Gain bandwidth	1.5 ↓ 1200	NE/SE { 530 538 5534 5534A	Yes Yes Yes Yes	Yes Yes	
			MHz	NE 5539*			
2,000	Maximum loading	600	NE/SE { 5534 5534A	Yes Yes	Yes Yes		
		OHM					

3

HIGH PERFORMANCE JFET INPUT OP AMPS

LF355/356

DESCRIPTION

The LF355 and LF356 operational amplifiers employ well matched, high voltage JFET input structures on the same monolithic chip as bipolar devices. These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time and low noise.

COMMON FEATURES (TYPICAL)

- Low input bias current 50pA
- Low input offset current 10pA
- High input impedance $10^{12}\Omega$
- Low input offset voltage 3mV
- Low V_{OS} temperature drift $5\mu V/^{\circ}C$
- Low input noise current $0.01pA/\sqrt{Hz}$

APPLICATIONS

- Precision high speed integrators
- Fast A/D, D/A converters
- High impedance buffers
- Wideband, low noise, low drift amplifier

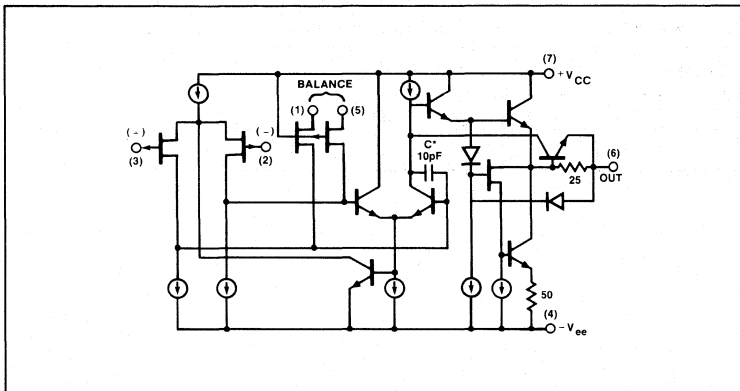
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	± 18	V
Power dissipation	500	mW
Operating temperature range	0 to 170	$^{\circ}C$
T_j (Max)	100	$^{\circ}C$
Input voltage range ¹	± 20	V
Output short circuit duration	Continuous	
Storage temperature range	-65 to +150	$^{\circ}C$
Lead temperature (soldering 10 sec.)	300	$^{\circ}C$

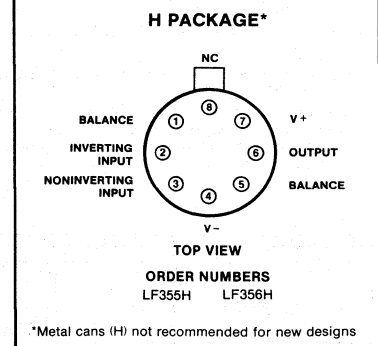
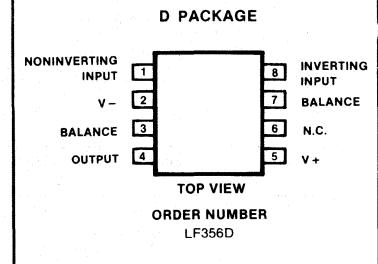
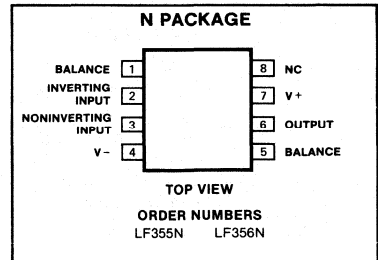
NOTE

1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

EQUIVALENT SCHEMATIC



PIN CONFIGURATION



3

HIGH PERFORMANCE JFET INPUT OP AMPS

LF355/356

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LF355/356			UNIT
		Min	Typ	Max	
V_{os}	Input offset voltage		3	10 13	mV mV
$\Delta V_{os}/\Delta T$	Avg. TC of input offset voltage		5		$\mu\text{V}/^\circ\text{C}$
$\Delta\text{TC}/\Delta V_{os}$	Change in average TC ² with V_{os} adjust		0.5		$\mu\text{V}/^\circ\text{C}$ per mV
I_{os}	Input offset current ^{1,3}		3	50 2	pA nA
I_B	Input bias current ^{1,3}		30	200 8	pA nA
R_{IN}	Input resistance				Ω
A_{VOL}	Large signal voltage gain				V/mV
			25	10 ¹² 200	V/mV
V_o	Output voltage swing		± 12 ± 10	± 13 ± 12	V V
V_{CM}	Input common mode Voltage range		± 10	+15.1 -12	V V V
CMRR	Common-mode rejection ratio		80	100	dB
PSRR	Supply volt. rej. ratio ⁴		80	100	dB

NOTES

- These specifications apply for $V_s = \pm 15\text{V}$ and $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$. V_{os} , I_B and I_{os} are measured at $V_{CM} = 0$.
- The Temperature Coefficient of the adjusted input offset voltage changes only a small amount ($0.5\mu\text{V}/^\circ\text{C}$ typically) for each mV of adjustment from its original unadjusted value. Common mode rejection and open loop voltage gain are also unaffected by offset adjustment.
- The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d . $T_J = T_A + \theta_{JA} P_d$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
- Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_s = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	LF355			LF356			UNIT
	Min	Typ	Max	Min	Typ	Max	
Supply current		2	4		5	10	mA

HIGH PERFORMANCE JFET INPUT OP AMPS

LF355/356

3

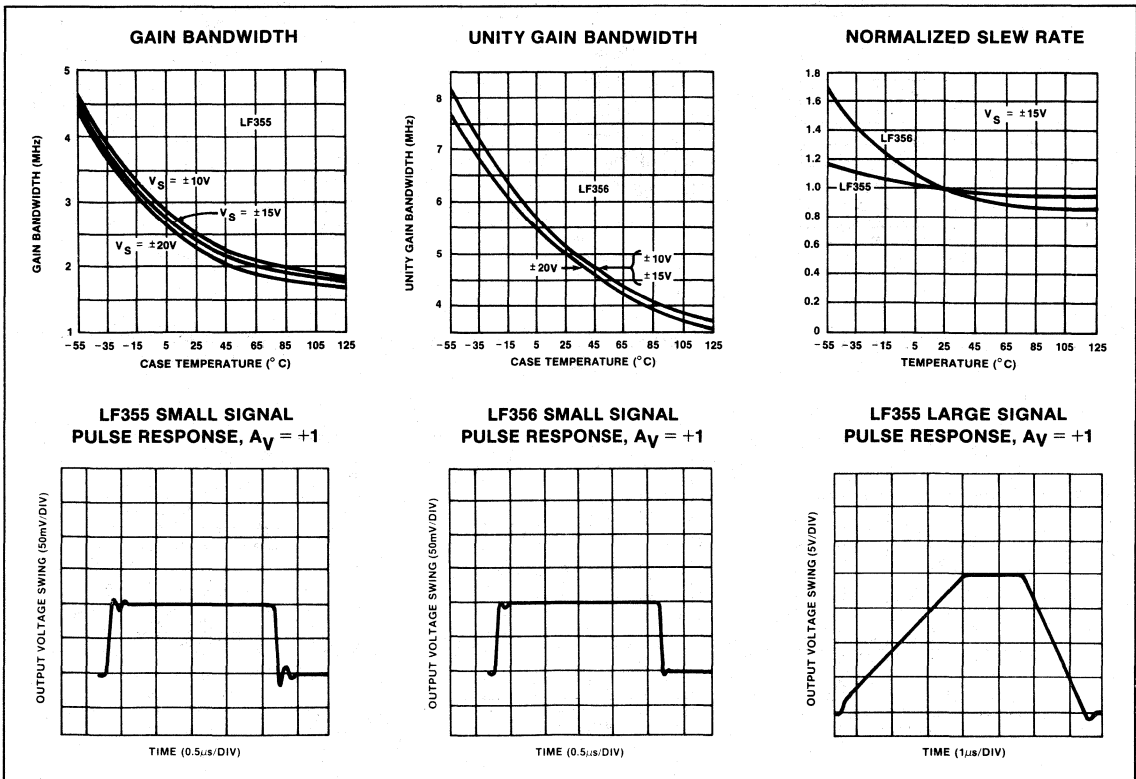
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.¹

PARAMETER	TEST CONDITIONS	LF355			LF356			UNIT
		Min	Typ	Max	Min	Typ	Max	
SR Slew rate	$A_V = 1$		5			12		$\text{V}/\mu\text{s}$
GBW Gain bandwidth product			2.5			5		MHz
t_s Settling time ¹ to 0.01%			4			1.5		μs
e_n Equiv. input noise volt.	$R_s = 100\Omega$ $f = 100\text{Hz}$ $f = 1000\text{Hz}$		25 20			15 12		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$
i_n Equiv. input noise current	$f = 100\text{Hz}$ $f = 1000\text{Hz}$		0.01 0.01			0.01 0.01		$\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$
C_{IN} Input capacitance			3			3		pF

NOTE

1. Settling time is defined here, for a unity gain inverter connection using 2k Ω resistors for the LF355/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter.

TYPICAL AC PERFORMANCE CHARACTERISTICS

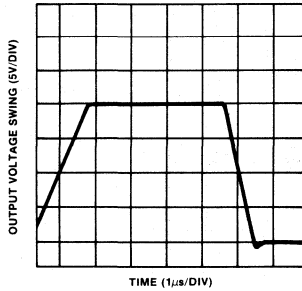


HIGH PERFORMANCE JFET INPUT OP AMPS

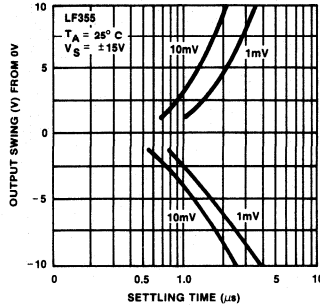
LF355/356

TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

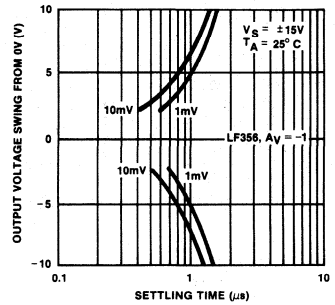
LF356 LARGE SIGNAL PULSE RESPONSE, $A_v = +1$



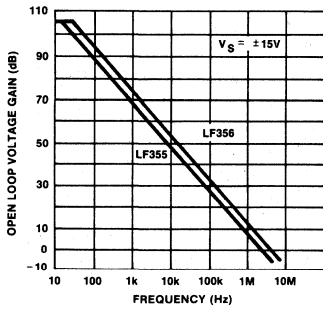
INVERTER SETTLING TIME



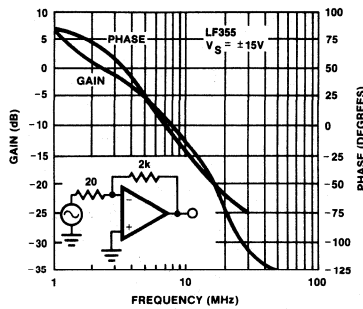
INVERTER SETTLING TIME



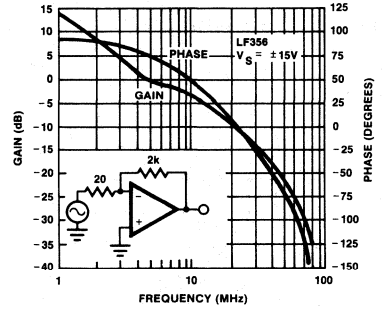
OPEN LOOP FREQUENCY RESPONSE



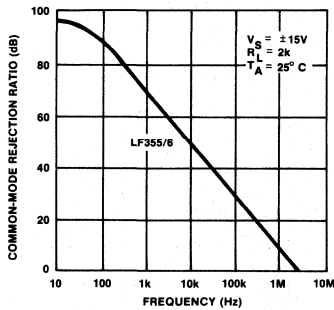
BODE PLOT



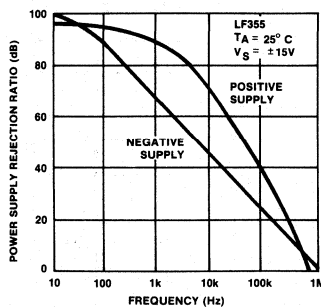
BODE PLOT



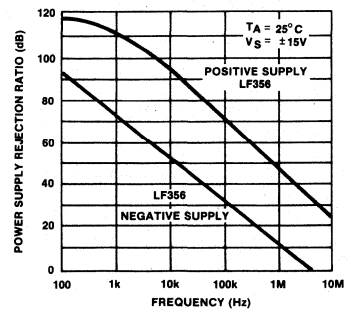
COMMON-MODE REJECTION RATIO



POWER SUPPLY REJECTION RATIO



POWER SUPPLY REJECTION RATIO

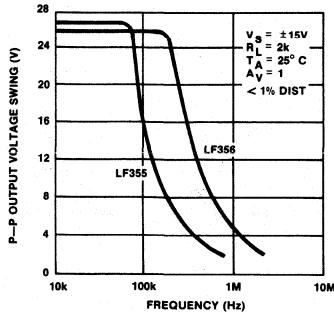


HIGH PERFORMANCE JFET INPUT OP AMPS

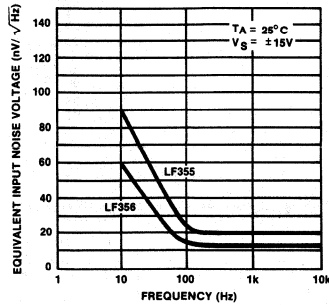
LF355/356

TYPICAL AC PERFORMANCE CHARACTERISTICS (Cont'd)

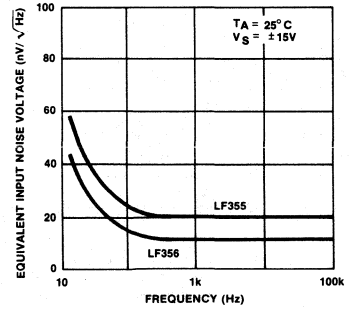
UNDISTORTED OUTPUT VOLTAGE SWING



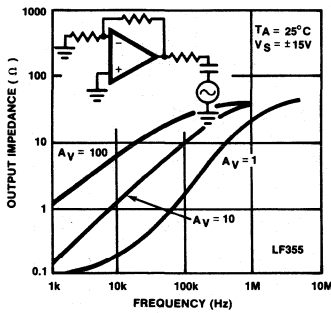
EQUIVALENT INPUT NOISE VOLTAGE



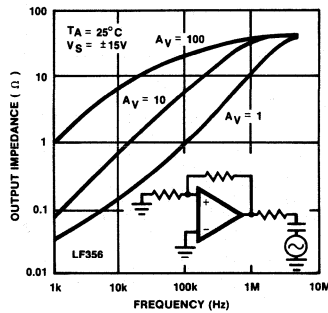
EQUIVALENT INPUT NOISE VOLTAGE (EXPANDED SCALE)



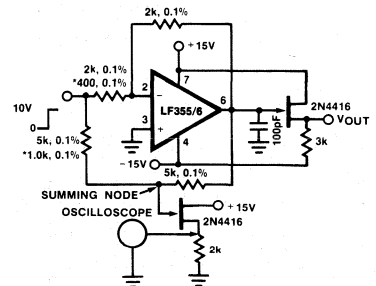
OUTPUT IMPEDANCE



OUTPUT IMPEDANCE



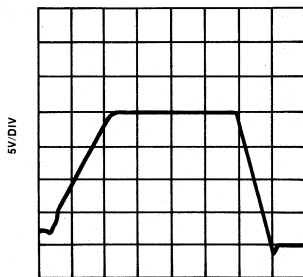
SETTLING TIME TEST CIRCUIT



- Settling time is tested with the LF355/6 connected as unity gain inverter,
- FET used to isolate the probe capacitance
- Output = 10V step

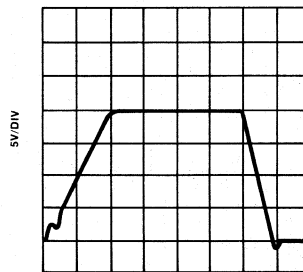
LARGE SIGNAL INVERTER OUTPUT, V_{OUT} (FROM SETTLING TIME CIRCUIT)

LF355



2μs/DIV

LF356



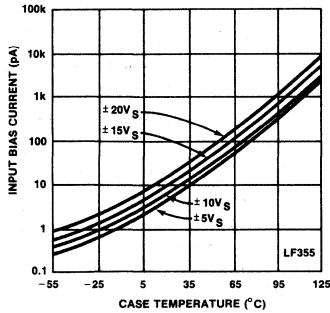
1μs/DIV

HIGH PERFORMANCE JFET INPUT OP AMPS

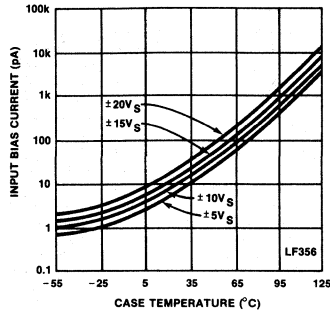
LF355/356

TYPICAL DC PERFORMANCE CHARACTERISTICS

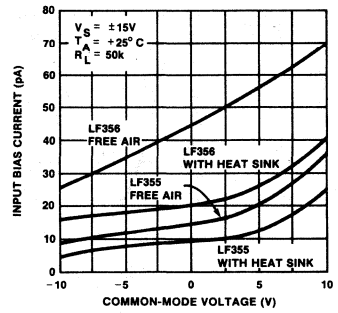
INPUT BIAS CURRENT



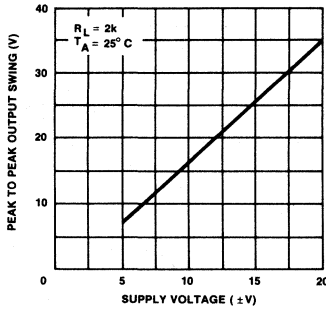
INPUT BIAS CURRENT



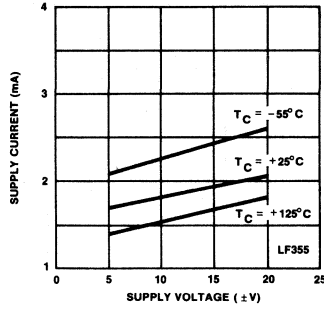
INPUT BIAS CURRENT



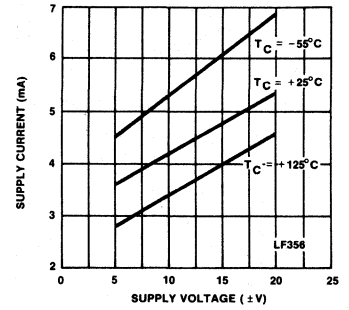
VOLTAGE SWING



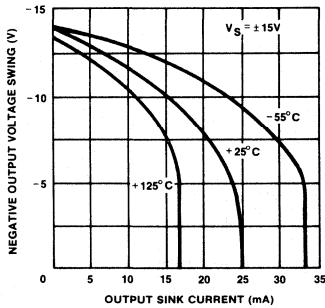
SUPPLY CURRENT



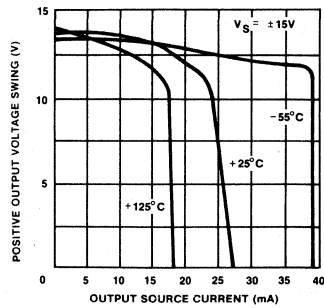
SUPPLY CURRENT



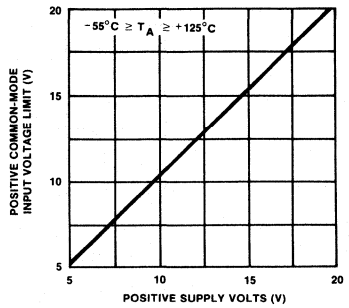
NEGATIVE CURRENT LIMIT



POSITIVE CURRENT LIMIT



POSITIVE COMMON-MODE INPUT VOLTAGE LIMIT

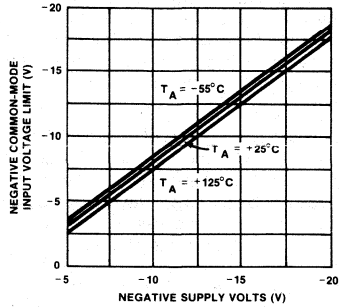


HIGH PERFORMANCE JFET INPUT OP AMPS

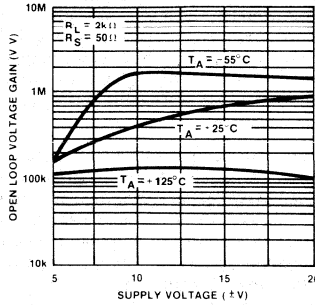
LF355/356

TYPICAL DC PERFORMANCE CHARACTERISTICS (Cont'd)

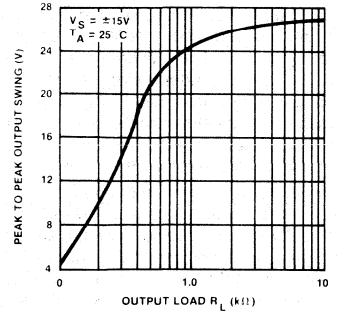
NEGATIVE COMMON-MODE INPUT VOLTAGE LIMIT



OPEN LOOP VOLTAGE GAIN



OUTPUT VOLTAGE SWING



3

HIGH PERFORMANCE JFET INPUT OP AMPS

LF355/356

APPLICATIONS

The LF355 and LF356 are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit. Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs ex-

ceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

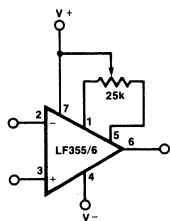
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore

essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

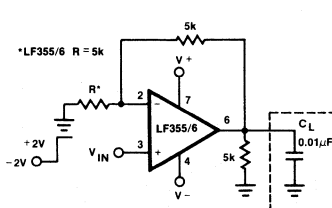
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

TYPICAL CIRCUIT CONNECTIONS

V_{OS} ADJUSTMENT

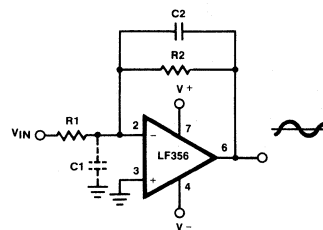
- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V+
- For potentiometers with temperature coefficient of 100ppm/°C or less the additional drift with adjust is $\approx 0.5\mu\text{V}/^\circ\text{C/mV}$ of adjustment
- Typical overall drift: $5\mu\text{V}/^\circ\text{C} \pm (0.5\mu\text{V}/^\circ\text{C/mV}$ of adj.)

DRIVING CAPACITIVE LOADS



Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_L \text{ max} \leq 0.01\mu\text{F}$.
Overshoot $\leq 20\%$
Setting time (ts) $\geq 5\mu\text{s}$

TYPICAL APPLICATIONS

WIDE BW LOW NOISE,
LOW DRIFT AMPLIFIER

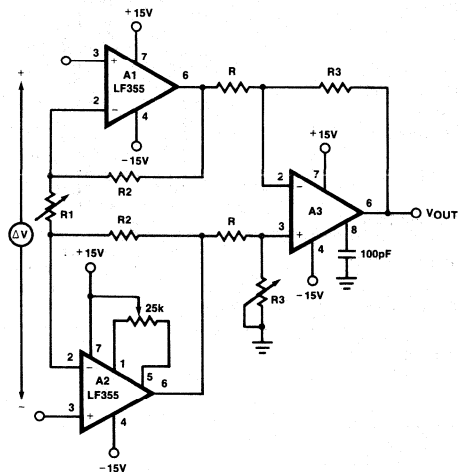
- Power BW: $f_{\text{max}} = \frac{S_r}{2\pi/p} \approx 240\text{kHz}$
- Parasitic input capacitance $C1 \approx (3\text{pF}$ for LF355 and LF356, plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add $C2$ such that: $R2C2 \approx R1C1$.

HIGH PERFORMANCE JFET INPUT OP AMPS

LF355/356

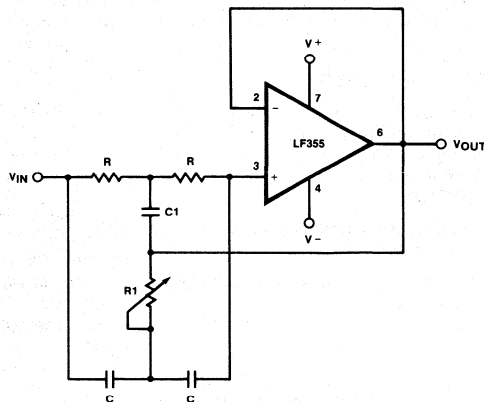
TYPICAL APPLICATIONS (Cont'd)

HIGH IMPEDANCE, LOW DRIFT INSTRUMENTATION AMPLIFIER



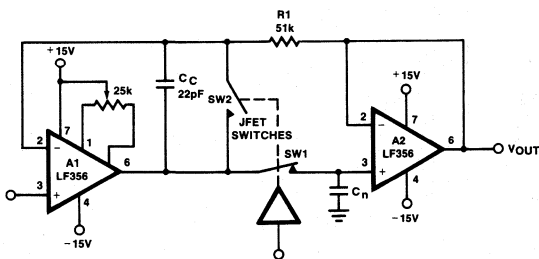
- $V_{OUT} = \frac{R3}{R} \left[\frac{2R2}{R1} + 1 \right] \Delta V, V^- +2V \leq V_{IN} \text{ Common-Mode} \leq V^+$
- System Vos adjusted via A2 Vos adjust
- Trim R3 to boost up CMRR to 120dB.

HIGH Q NOTCH FILTER



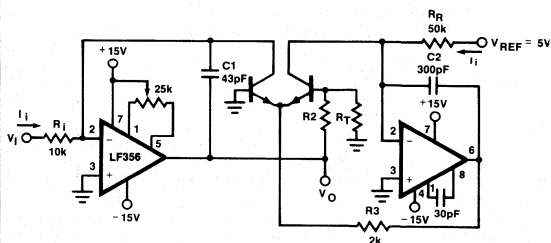
- $2R1 = R = 10M\Omega$
- $2C = C1 = 300pF$
- Capacitors should be matched to obtain high Q
- $f_{NOTCH} = 120Hz, \text{ notch} = 55dB, Q > 180$
- Use LF355 for Δ Low I_b
- Δ Low supply current

HIGH ACCURACY SAMPLE AND HOLD



- By closing the loop through A2 the V_{OUT} accuracy will be determined uniquely by A1. No Vos adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added on propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold.
- R1, C_c : additional compensation
- Use LF356 for Δ Fast settling time
- Δ Low Vos

FAST LOGARITHMIC CONVERTER



$$|V_{OUT}| = \left[1 + \frac{R2}{R} \right] \frac{kT}{q} \ln V_i \left[\frac{R_r}{V_{REF} R_i} \right] = \log V_i \frac{1}{R_i I_R}$$

$R2 = 15.71, R1 = 1k, 0.3\%/^{\circ}C$ (for temperature compensation)

- Dynamic range: $100\mu A \leq I_i \leq 1mA$ (5 decades, $|V_o| = 1V/\text{decades}$)
- Transient response: $3\mu s$ for $\Delta =$ decades
- $C1, C2, R2, R3$: added dynamic compensation
- Vos adjust the LF356 to minimize quiescent error
- R_r : Tel Labs type Q81 + $0.3\%/^{\circ}C$.

GENERAL PURPOSE SINGLE SUPPLY OP AMP**LM124/224/324/SA534****DESCRIPTION**

The LM124/SA534 series consists of four independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages.

UNIQUE FEATURES

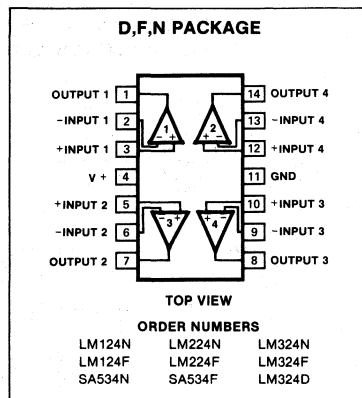
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain cross frequency is temperature compensated.

The input bias current is also temperature compensated.

FEATURES

- Internally frequency compensated for unity gain
- Large dc voltage gain—(100dB)
- Wide bandwidth (unity gain)—1MHz (temperature compensated)
- Wide power supply range
Single supply—(3Vdc to 30Vdc) or dual supplies—(± 1.5 Vdc to ± 15 Vdc)
- Very low supply current drain—essentially independent of supply voltage (1mW/op amp at +5Vdc)
- Low input biasing current—(45nA dc temperature compensated)
- Low input offset voltage—(2mVdc) and offset current—(5nA dc)
- Differential input voltage range equal to the power supply voltage
- Large output voltage—(0Vdc to $V+ - 1.5$ Vdc swing)
- LM124 MII std 883A,B,C available

PIN CONFIGURATION**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	RATING	UNIT	
V+	Supply voltage	32 or ± 16	Vdc
	Differential input voltage	32	Vdc
	Input voltage	-0.3 to +32	Vdc
	Power dissipation ¹		
	N package	570	mW
	F package	900	mW
	Output short-circuit to GND		
	1 amplifier ²	Continuous	
	V+ < 15Vdc and T _A = 25°C		
	Input current (V _{IN} < -0.3V) ³	50	mA
	Operating temperature range		
	LM324	0 to +70	°C
	LM224	-25 to +85	°C
	SA534	-40 to +85	°C
	LM124	-55 to +125	°C
	Storage temperature range	-65 to +150	°C
	Lead temperature (soldering, 10sec)	300	°C

NOTES

1. For operating at high temperatures, all devices must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. LM 124/224 can be derated based on a +150°C maximum junction temperature.
2. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V+. At values of supply voltage in excess of +15Vdc continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the input lines.

GENERAL PURPOSE SINGLE SUPPLY OP AMP

LM124/224/324/SA534

DC ELECTRICAL CHARACTERISTICS $V_+ = 5V$, $T_A = 25^\circ C$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LM124/LM224			LM324/SA534			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage ¹	$R_S = 0\Omega$ $R_S = 0\Omega$, over temp.		± 2	± 5 ± 7		± 2	± 7 ± 9	mV mV
V_{OS} Drift	$R_S = 0\Omega$		7			7		$\mu V / ^\circ C$
I_{BIAS} Input current ²	$I_{IN}(+)$ or $I_{IN}(-)$ $I_{IN}(+)$ or $I_{IN}(-)$, over temp.		45 40	150 300		45 40	250 500	nA nA
I_{OS} Offset current	$I_{IN}(+) - I_{IN}(-)$ $I_{IN}(+) - I_{IN}(-)$, over temp.		± 3	± 30 ± 100		± 5	± 50 ± 150	nA nA
I_{OS} Drift			10			10		$\mu A / ^\circ C$
V_{CM} Common mode voltage range ³	$V_+ = 30V$ $V_+ = 30V$, over temp.	0 0		$V_+ - 1.5$ $V_+ - 2$	0 0		$V_+ - 1.5$ $V_+ - 2$	V V
$CMRR$ Common mode rejection ratio		70	85		65	70		dB
V_{OUT} Output voltage swing	$R_L = 2k\Omega$, $V_+ = +30V$, over temp.	26			26			V
V_{OH}	$R_L \leq 10k\Omega$, over temp.	27	28		27	28		V
V_{OL}	$R_L \leq 10k\Omega$, $V_+ = 5V$, over temp.		5	20		5	20	mV
I_{CC} Supply current	$R_L = \infty$, $V_{CC} = 30V$, over temp. $R_L = \infty$, on all op amps, over temp.		1.5 0.7	3 1.2		1.5 0.7	3 1.2	mA
A_{VOL} Large signal voltage gain	$V_+ = +15V$ (for large V_O swing), $R_L \geq 2k\Omega$ $V_+ = +15V$ (for large V_O swing), $R_L \geq 2k\Omega$, over temp.	50 25	100		25 15	100		V/mV V/mV
Amplifier-to-amplifier coupling ⁵	$f = 1kHz$ to $20kHz$, input referred		-120			-120		dB
PSRR	$R_S \leq 0\Omega$	65	100		65	100		dB
Output current Source	$V_{IN+} = +1Vdc$, $V_{IN-} = 0Vdc$, $V_+ = 15Vdc$	20	40		20	40		mA
Sink	$V_{IN+} = +1Vdc$, $V_{IN-} = 0Vdc$, $V_+ = 15Vdc$, over temp.	10	20		10	20		mA
	$V_{IN-} = +1Vdc$, $V_{IN+} = 0Vdc$, $V_+ = 15Vdc$	10	20		10	20		mA
	$V_{IN-} = +1Vdc$, $V_{IN+} = 0Vdc$, $V_+ = 15Vdc$, over temp.	5	8		5	8		mA
	$V_{IN+} = 0Vdc$, $V_{IN-} = +1Vdc$, $V_O = 200mV$	12	50		12	50		μA
I_{SC} Short circuit current ⁴			40	60		40	60	mA
Differential input voltage ⁶				V_+			V_+	V

NOTES

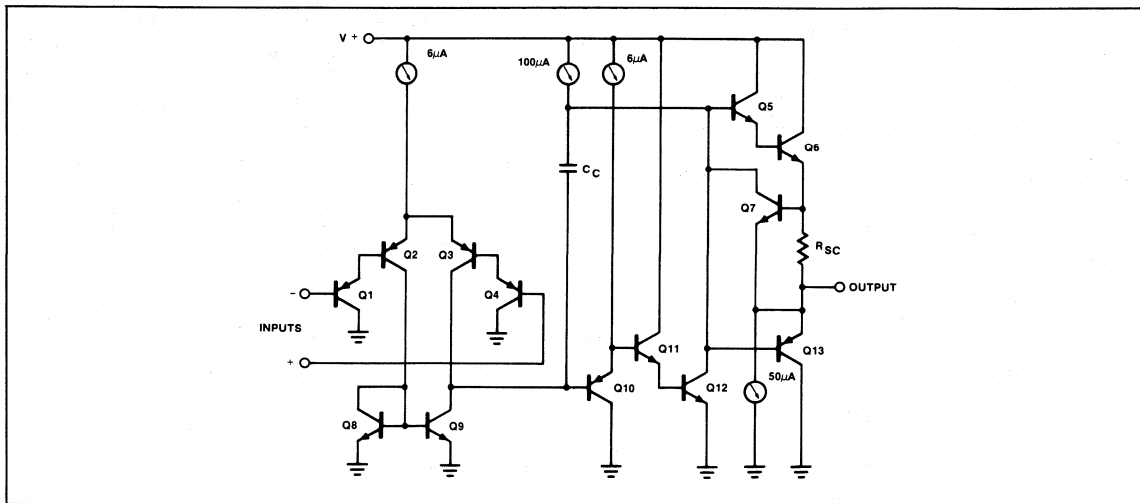
- $V_O = 1.4Vdc$, $R_S = 0\Omega$ with V_+ from 5V to 30V and over full input common mode range (0Vdc to $V_+ - 1.5V$).
- The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_+ - 1.5$, but either or both inputs can go to +32V without damage.
- Short circuits from the output to V_+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the

- magnitude of V_+ . At values of supply voltage in excess of +15Vdc continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
- Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.
 - The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_+ - 1.5V$, but either or both inputs can go to +32Vdc without damage.

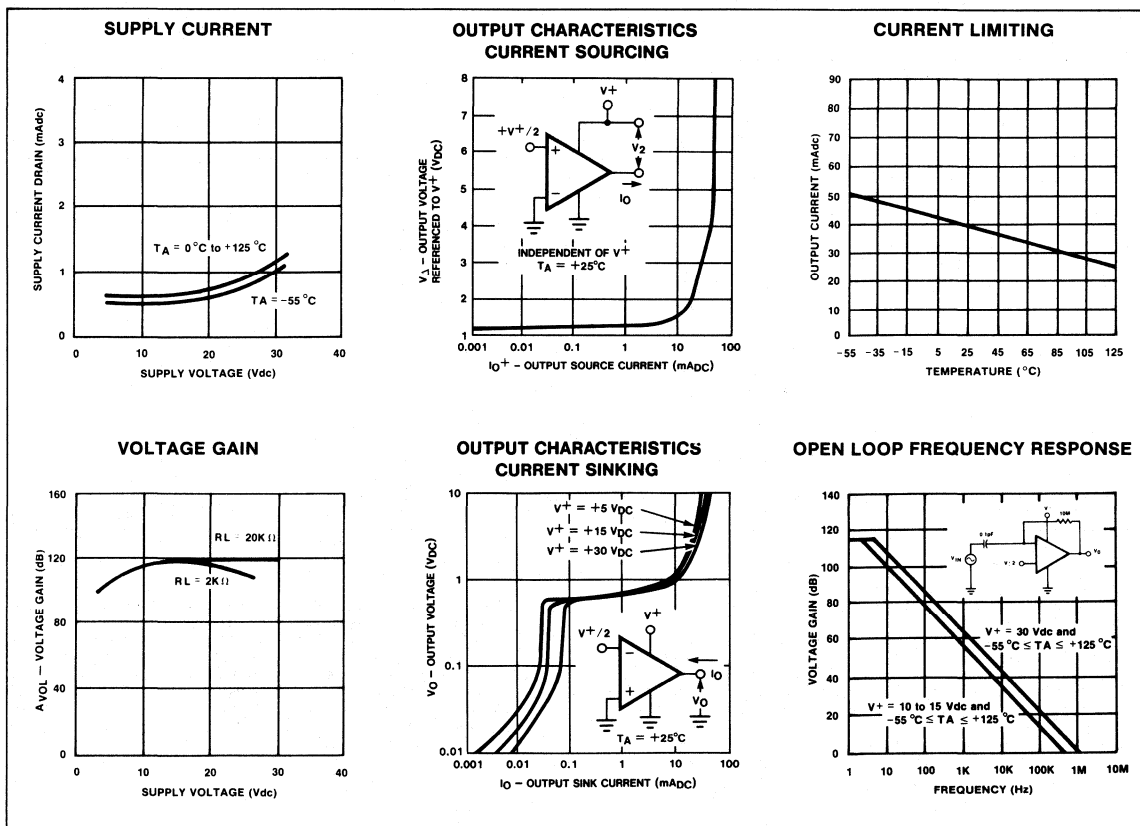
GENERAL PURPOSE SINGLE SUPPLY OP AMP

LM124/224/324/SA534

EQUIVALENT SCHEMATIC



TYPICAL PERFORMANCE CHARACTERISTICS

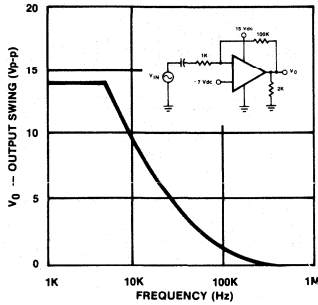


GENERAL PURPOSE SINGLE SUPPLY OP AMP

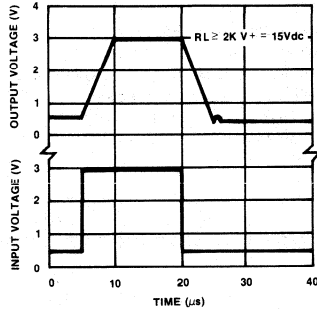
LM124/224/324/SA534

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

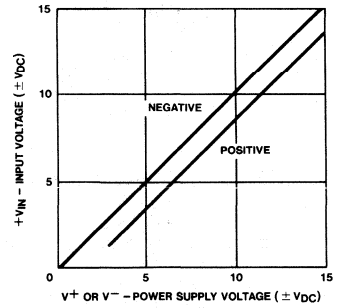
LARGE SIGNAL FREQUENCY RESPONSE



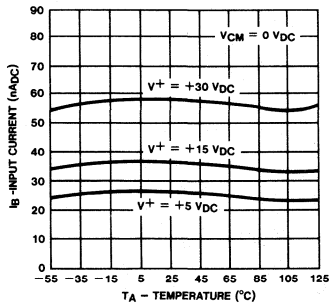
VOLTAGE FOLLOWER PULSE RESPONSE



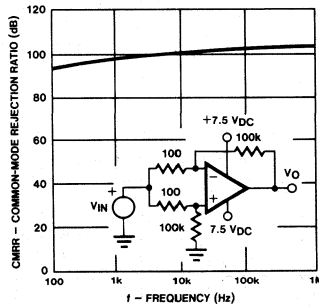
INPUT VOLTAGE RANGE



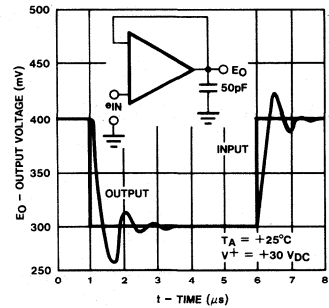
INPUT CURRENT



COMMON MODE REJECTION RATIO



VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



3

HIGH PERFORMANCE AMPLIFIER

LM301A

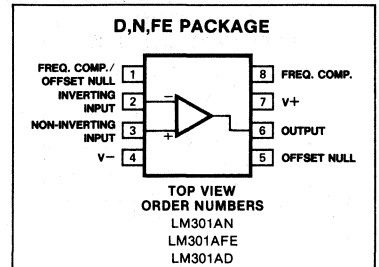
DESCRIPTION

The LM301A is a high performance operational amplifier featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

FEATURES

- Short circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch up
- LM101, LM101A, LH2101, LH2101A
MIL std 883A,B,C available
- LM101A, LH2101A MIL-STD-38510
(JAN) available

PIN CONFIGURATIONS



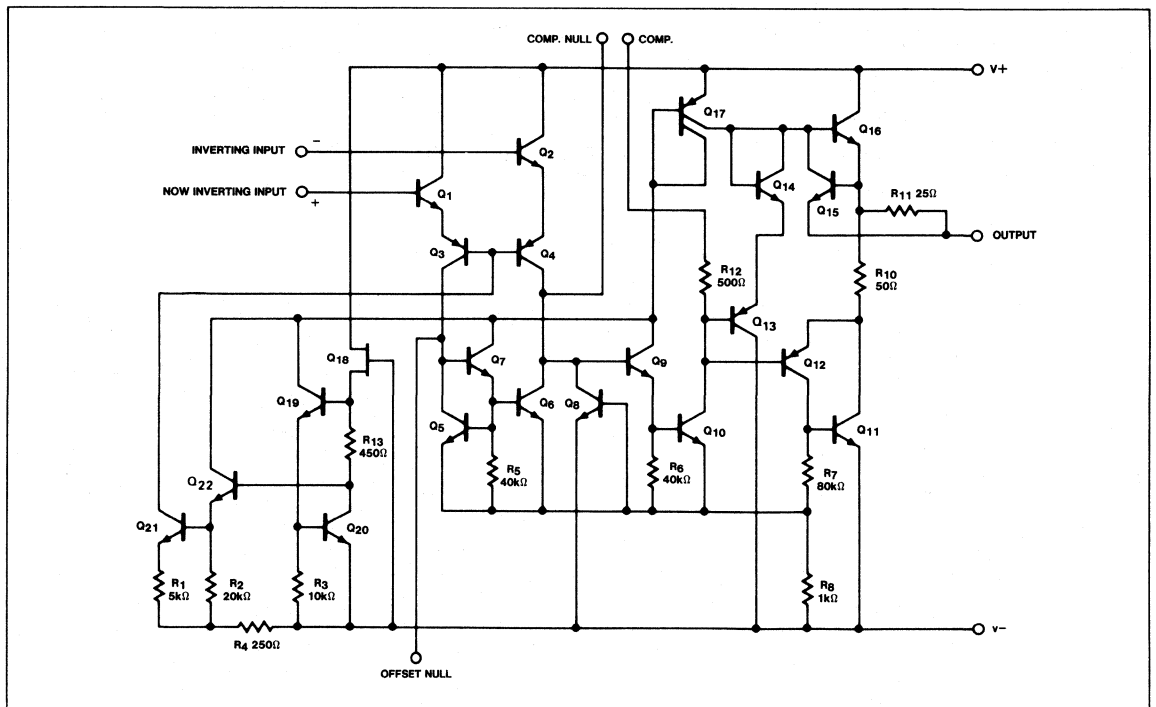
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage LM301A	± 18	V
Power dissipation	500	mW
Differential input voltage	± 30	V
Input voltage ¹	± 15	V
Output short circuit duration	Indefinite	
Operating temperature range LM301A	0 to +70	$^{\circ}\text{C}$
Storage temperature range	-65 to +150	$^{\circ}\text{C}$
Lead temperature (soldering 60sec)	300	$^{\circ}\text{C}$

NOTES

1. For supply voltages less than $\pm 15\text{V}$, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC



HIGH PERFORMANCE AMPLIFIER

LM301A

3

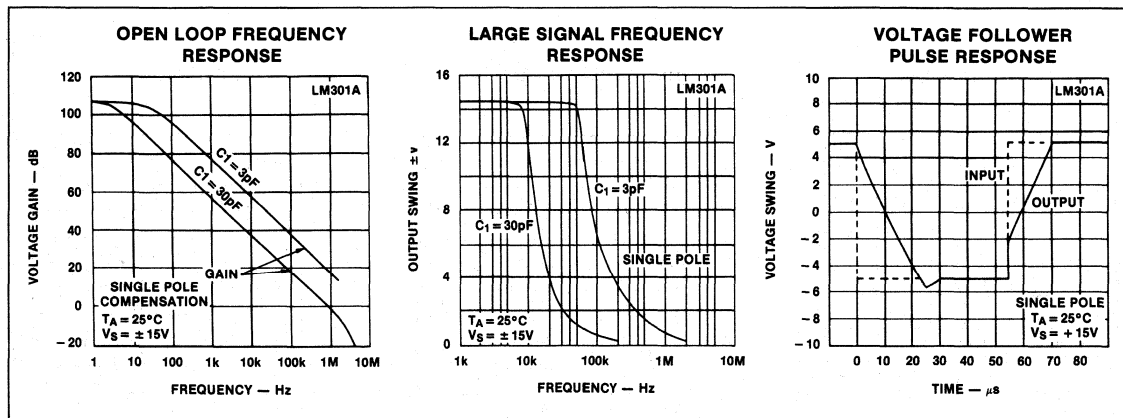
DC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A < 70^{\circ}\text{C}$, $\pm 5\text{V} \leq V_S \leq \pm 15\text{V}$ and $C_1 = 30\text{pF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS} Input Offset Voltage	$T_A = 25^{\circ}\text{C}$, $R_S < 50\text{k}\Omega$		2.0	7.5	mV
I_{OS} Input Offset Current	$T_A = 25^{\circ}\text{C}$		3	50	nA
I_{BIAS} Input Bias Current	$T_A = 25^{\circ}\text{C}$		70	250	nA
I_{OS} Input Resistance	$T_A = 25^{\circ}\text{C}$	0.5	2		$\text{M}\Omega$
I_{CC} Supply Current	$T_A = 25^{\circ}\text{C}$, $V_S = \pm 15\text{V}$		1.8	3.0	mA
A_{VOL} Large Signal Voltage Gain	$T_A = 25^{\circ}\text{C}$, $V_S = \pm 15\text{V}$ $V_{OUT} = \pm 10\text{V}$; $R_L > 2\text{k}\Omega$	25	160		V/mV
V_{OS} Input Offset Voltage	$R_S < 50\text{k}\Omega$			10	mV
V_{OS} Average Temperature Coefficient of Input Drift Offset Voltage			6.0	30	$\mu\text{V}/^{\circ}\text{C}$
I_{OS} Input Offset Current				70	nA
I_{OS} Average Temperature Coefficient of Input Offset Current	$25^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$ $0^{\circ}\text{C} < T_A < 25^{\circ}\text{C}$		0.01 0.02	0.3 0.6	$\text{nA}/^{\circ}\text{C}$ $\text{nA}/^{\circ}\text{C}$
I_{BIAS} Input Bias Current				300	nA
A_{VOL} Large Signal Voltage Gain	$V_S = \pm 15\text{V}$, $V_{OUT} = \pm 10\text{V}$ $R_L > 2\text{k}\Omega$	15			V/mV
V_{OUT} Output Voltage Swing	$V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$	± 12 ± 10	± 14 ± 13		V V
V_{IN} Input Voltage Range	$V_S = \pm 15\text{V}$	± 12			V
C_{MRR} Common Mode Rejection Ratio	$R_S < 50\text{k}\Omega$	70	90		dB
$PSRR$ Supply Voltage Rejection Ratio	$R_S < 50\text{k}\Omega$	70	96		dB

***NOTE**

Unless otherwise specified, all specifications for LM301A are $\pm 5\text{V} \leq V_S \leq \pm 15\text{V}$.

TYPICAL PERFORMANCE CHARACTERISTICS

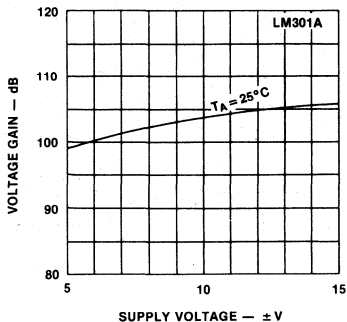


HIGH PERFORMANCE AMPLIFIER

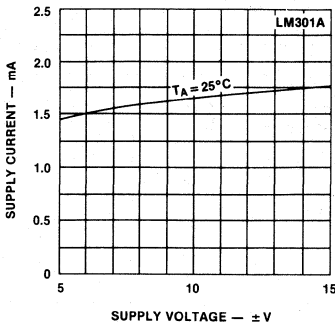
LM301A

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

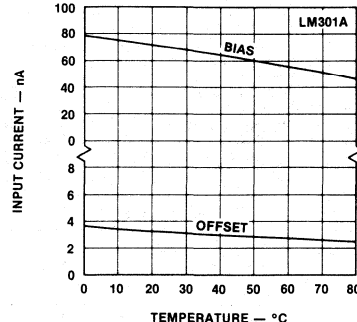
VOLTAGE GAIN



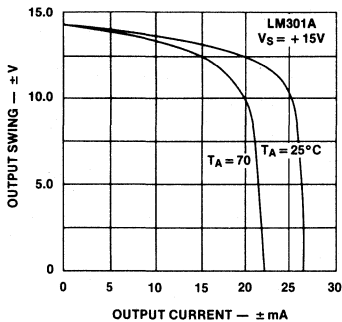
SUPPLY CURRENT



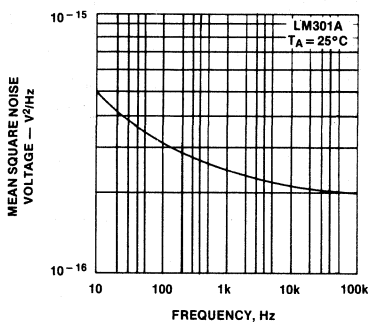
INPUT CURRENT



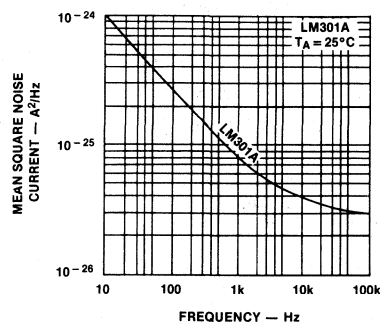
CURRENT LIMITING



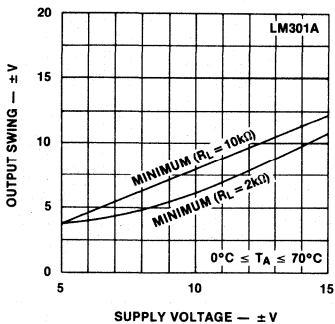
INPUT NOISE VOLTAGE



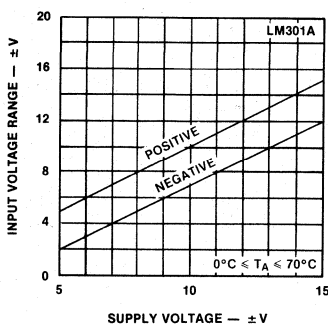
INPUT NOISE CURRENT



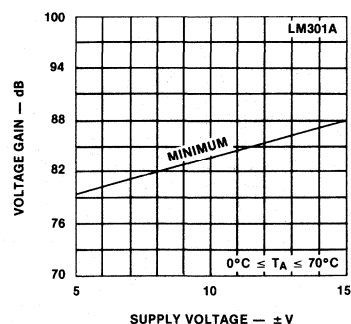
OUTPUT SWING



INPUT VOLTAGE RANGE



VOLTAGE GAIN

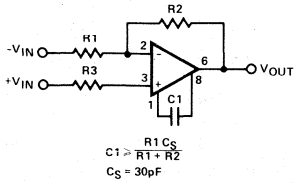


HIGH PERFORMANCE AMPLIFIER

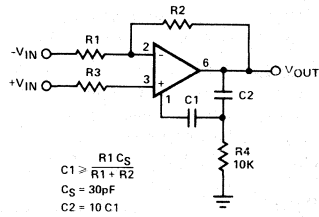
LM301A

COMPENSATION CIRCUITS

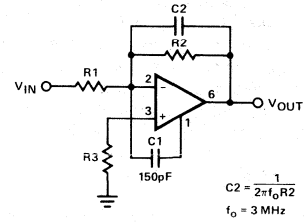
SINGLE POLE COMPENSATION



TWO POLE COMPENSATION



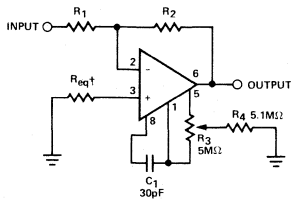
FEED FORWARD COMPENSATION



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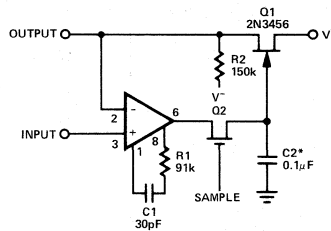
TYPICAL APPLICATIONS

INVERTING AMPLIFIER WITH BALANCING CIRCUIT



*May be zero or equal to parallel combination of $R1$ and $R2$ for minimum offset.

LOW DRIFT SAMPLE AND HOLD



*Polycarbonate Dielectric Capacitor

OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

LM13600/13600A

DESCRIPTION

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers are provided which are specifically designed to complement the dynamic range of the amplifiers.

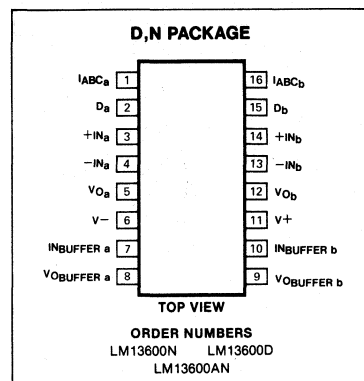
FEATURES

- gm adjustable over 6 decades
- Excellent gm linearity
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedance buffers
- High output signal to noise ratio
- Wide supply range $\pm 2V$ to $\pm 22V$.

APPLICATIONS

- Current controlled amplifiers
- Current controlled impedances
- Current controlled filters
- Current controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

PIN DESCRIPTION

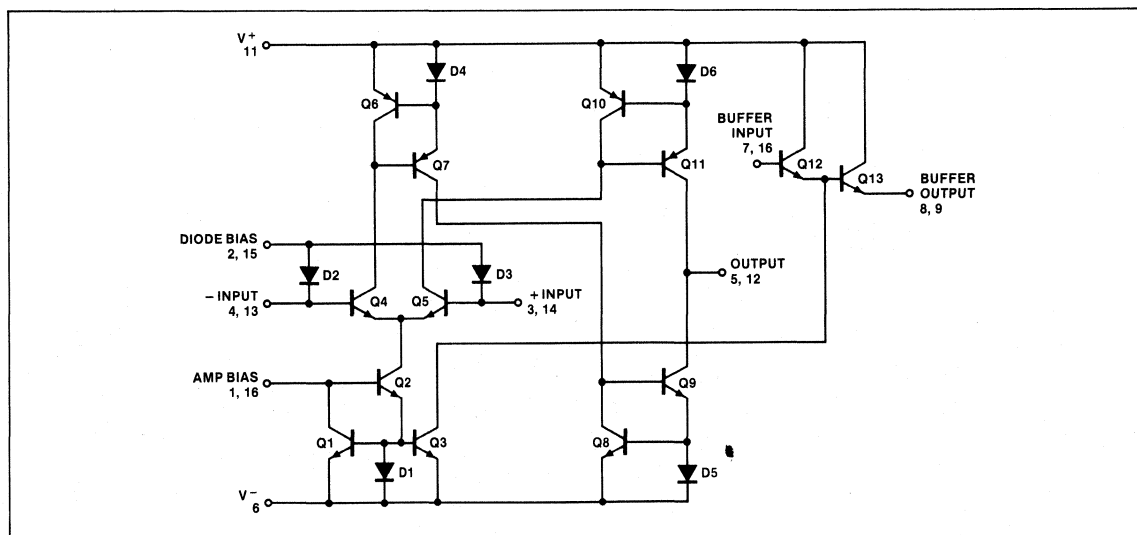


NOTE
See Signetics NE5517 for typical circuit applications information.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage ¹		
LM13600	36 V _{DC} or ± 18	V
LM13600A	44 V _{DC} or ± 22	V
Power dissipation ² T _A = 25°C		
LM13600N, LM13600AN	570	mW
Differential input voltage	± 5	V
Diode bias current (I _D)	2	mA
Amplifier bias current (I _{ABC})	2	mA
Output short circuit duration	Indefinite	
Buffer output current ³	20	mA
Operating temperature range		
LM13600N, LM13600AN	0°C to +70	°C
DC input voltage	+V _S to -V _S	
Storage temperature range	-65°C to +150	°C
Lead temperature (Soldering, 10 Seconds)	300	°C

BLOCK DIAGRAM



OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

LM13600/13600A

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LM13600			LM13600A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (V_{OS})	Over specified temperature range $I_{ABC} = 5\mu A$		0.4	5		0.4	2	mV
			0.3	5		0.3	5	mV
							2	mV
V_{OS} including diodes	Diode Bias Current (I_D) = 500 μA		0.5	5		0.5	2	mV
Input offset change	$5\mu A \leq I_{ABC} \leq 500\mu A$		0.1			0.1	3	mV
Input offset current			0.1	0.6		0.1	0.6	μA
input bias current	Over specified temperature range		0.4	5		0.4	5	μA
			1	8		1	7	μA
Forward Transconductance (gm)	Over specified temperature range	6700	9600	13000	7700	9600	12000	μmho
		5400			4000			μmho
gm tracking			0.3			0.3		dB
Peak output current	$R_L = 0, I_{ABC} = 5\mu A$ $R_L = 0, I_{ABC} = 500\mu A$ $R_L = 0, \text{Over specified temp range}$		5		3	5	7	μA
		350	500	650	350	500	650	μA
		300			300			μA
Peak output voltage positive negative	$R_L = \infty, 5\mu A \leq I_{ABC} \leq 500\mu A$	+12	+14.2		+12	+14.2		V
	$R_L = \infty, 5\mu A \leq I_{ABC} \leq 500\mu A$	-12	-14.4		-12	-14.4		V
Supply current	$I_{ABC} = 500\mu A, \text{Both channels}$		2.6			2.6		mA
V_{OS} sensitivity positive negative	$\Delta V_{OS}/\Delta V+$ $\Delta V_{OS}/\Delta V-$		20	150		20	150	$\mu V/V$
			20	150		20	150	$\mu V/V$
CMRR		80	110		80	110		dB
Common mode range		± 12	± 13.5		± 12	± 13.5		V
Crosstalk	Referred to input ⁵ 20 Hz < f < 20 KHz		100			100		dB
Diff. input current	$I_{ABC} = 0, \text{Input} = \pm 4V$		0.02	100		0.02	10	nA
Leakage current	$I_{ABC} = 0$ (Refer to test circuit)		0.2	100		0.2	5	nA
Input resistance		10	26		10	26		K Ω
Open loop bandwidth			2			2		MHz
Slew rate	Unity gain compensated		50			50		V/ μ Sec
Buff. input current	5		0.4	5		0.4	5	μA
Peak buffer output voltage	5	10			10			V

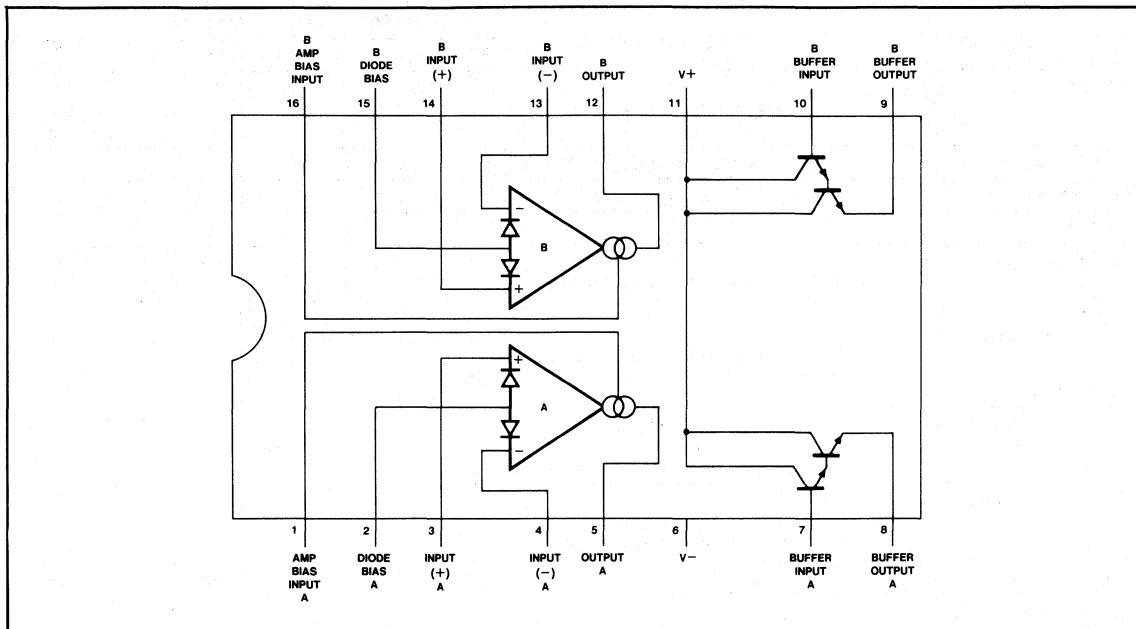
NOTES

- For selections to a supply voltage above $\pm 22V$, contact factory.
- For operating at high temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in still air.
- Buffer output current should be limited so as to not exceed package dissipation.
- These specifications apply for $V_S = \pm 15V, T_A = 25^\circ C$, amplifier bias current (I_{ABC}) = 500 μA , pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
- These specifications apply for $V_S = \pm 15V, I_{ABC} = 500\mu A, R_{OUT} = 5\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIERS

LM13600/13600A

CONNECTION DIAGRAM



HIGH PERFORMANCE OPERATIONAL AMPLIFIER

MC1456/1556

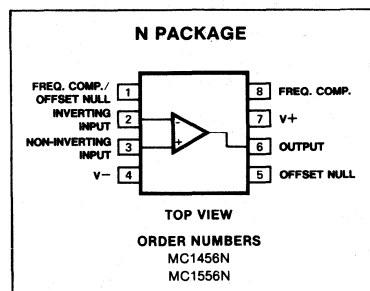
DESCRIPTION

The MC1456/1556 is an internally compensated precision monolithic operational amplifier featuring extremely low offset and bias currents and offset null capability. The MC1456/1556 is short circuit protected and its high common mode and differential input voltage range provides exceptional performance when used as an integrator, summing amplifier, and voltage follower.

FEATURES

- Low input bias current—15nA maximum
- Low input offset current—2.0nA maximum
- Low input offset voltage—4.0mV maximum
- High slew rate—2.5V/μs typical
- Large power bandwidth—40kHz typical
- Low power consumption—45mW maximum
- Offset voltage null capability
- Output short circuit protection
- Input over-voltage protection
- MIL-STD-883A,B,C available

PIN CONFIGURATION

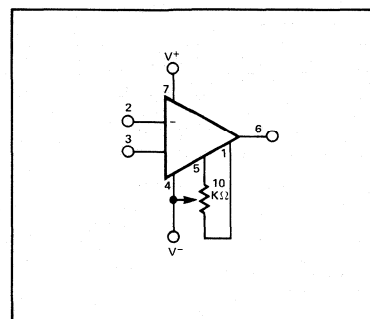


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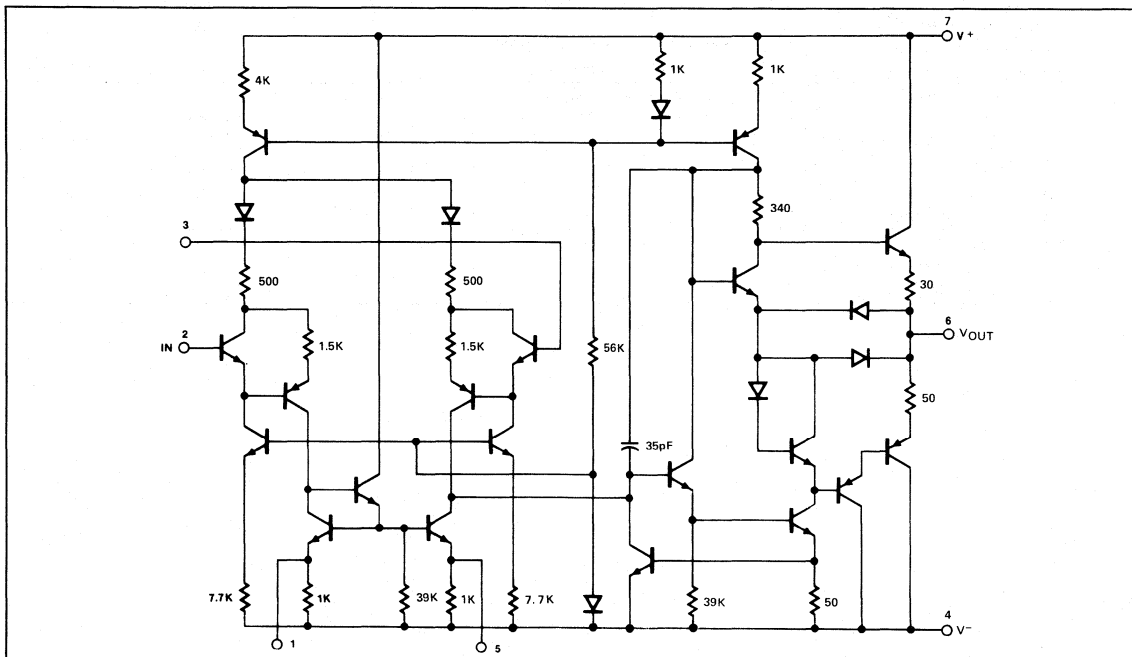
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage MC1556	±22	V
MC1456	±18	V
Differential input voltage	± V _{CC}	V
Common mode input voltage	± V _{CC}	V
Load current	20	mA
Output short circuit duration	Continuous	
Power dissipation	680	mW
Derate above T _A = 25°C	4.6.	mW/°C
Operating temperature range MC1556	-55 to +125	°C
MC1456	0 to +70	°C
Storage temperature range	-65 to +150	°C

OFFSET ADJUST CIRCUIT



EQUIVALENT SCHEMATIC



HIGH PERFORMANCE OPERATIONAL AMPLIFIER

MC1456/1556

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified

PARAMETER	TEST CONDITIONS	MC1556			MC1456			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	Over temperature		2.0	4.0 6.0		5.0	10.0 14.0	mVdc mVdc
I_{OS} Offset current	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $25^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ $-55^\circ\text{C} \leq T_A \leq 25^\circ\text{C}$		1.0	2.0 3.0 5.0		5.0	10.0 14	nA nA nA nA
I_{BIAS} Input current	Over temperature		8.0	15 30		15.0	30.0 40	nA nA
V_{CM} Common mode voltage range	$R_S \leq 10\text{k}\Omega$, $T_A = 25^\circ\text{C}$, $f = 100\text{Hz}$	± 12	± 13		± 11	± 12		V
CMRR Common mode rejection ratio	$f = 20\text{Hz}$	80	110		70	110		dB
Z_{IN} Common mode input impedance			250			250		M Ω
V_{OUT} Output voltage swing	$R_L = 2\text{k}\Omega$	± 12	± 13		± 11	± 12		V
I_{CC} Supply current			1.0	1.5		1.3	3.0	mA
P_D DC quiescent power dissipation ($V_O = 0$)			30	45		40	90	mW
PSRR Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$		50	100		75	200	$\mu\text{V}/\text{V}$
Large signal voltage gain	$R_L \leq 2\text{k}\Omega$, $V_{OUT} = \pm 10\text{V}$, $T_A = 25^\circ\text{C}$ Over temperature	100 40	200		70 40	100		V/mV V/mV

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

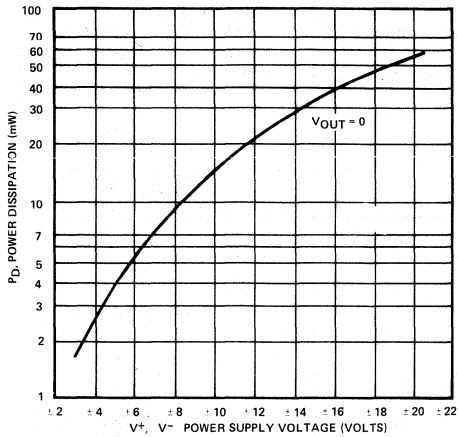
PARAMETER	TEST CONDITIONS	MC1556			MC1456			UNIT
		Min	Typ	Max	Min	Typ	Max	
C_p Differential input impedance	Open loop $f = 20\text{Hz}$		6.0			6.0		pF
r_p Parallel input capacitance			5			3		M Ω
e_n Parallel input resistance	$A_v = 100$, $R_S = 10\text{k}\Omega$, $f = 1.0\text{kHz}$, $BW = 1.0\text{kHz}$		45			45		$\text{nV}/\sqrt{\text{Hz}}$
BW_p Equivalent input noise voltage	$A_v = 1$, $R_L = 2\text{k}\Omega$, $\text{THD} \leq 5\%$ $V_{OUT} = \pm 10\text{V}$		40 70			40 70		kHz degrees
Phase margin (open loop, unity gain)			18			18		dB
Gain margin			2.5			2.5		V/ μsec
S_R Slew rate (unity gain)								
Z_{OUT} Output impedance	$f = 20\text{Hz}$		1.0	2.0		1.0	2.5	k Ω
BW Unity gain crossover frequency (open loop)			1.0			1.0		MHz

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

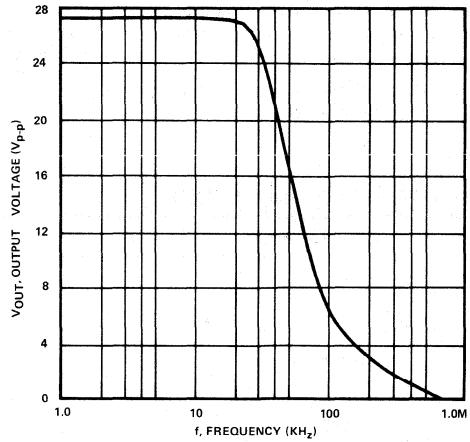
MC1456/1556

TYPICAL PERFORMANCE CHARACTERISTICS

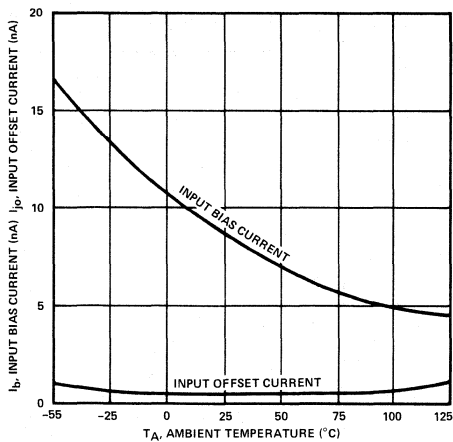
POWER DISSIPATION vs POWER SUPPLY VOLTAGE



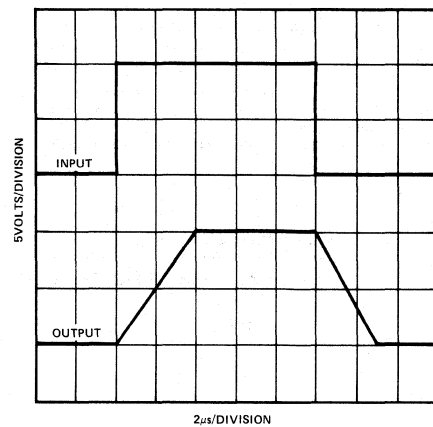
POWER BANDWIDTH



TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs TEMPERATURE FOR MC1556



VOLTAGE FOLLOWER PULSE RESPONSE



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GENERAL PURPOSE OPERATIONAL AMPLIFIER

MC/SA1458/MC1558

DESCRIPTION

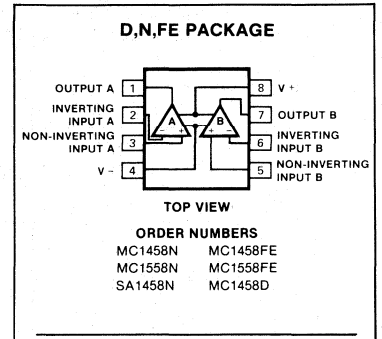
The MC1458 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The MC1458 is short-circuit protected and allows for nulling of offset voltage.

The MC1458/SA1458/MC1558 consists of a pair of 741 operational amplifiers on a single chip.

FEATURES

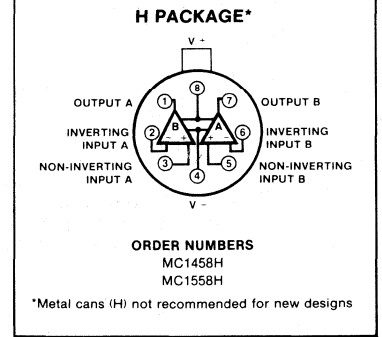
- Internal frequency compensation
- Short circuit protection
- Excellent temperature stability
- High input voltage range
- No latch-up
- 1558/1458 are 2 "op amps" in space of one 741 package
- MC1558 MIL-STD-883A,B,C available

PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

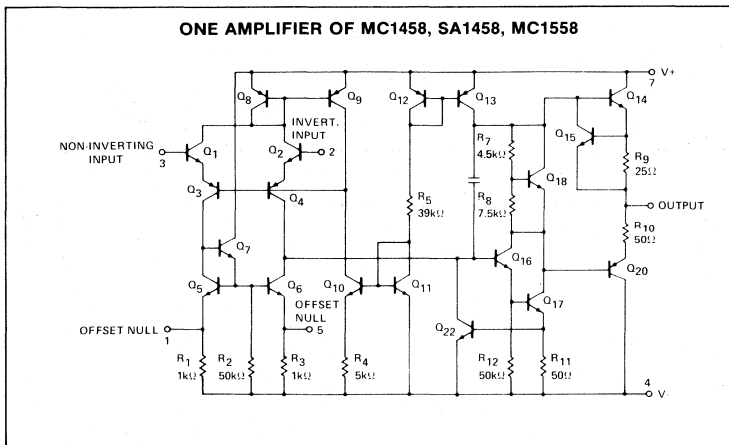
PARAMETER	RATING	UNIT
Supply voltage		
MC1458	±18	V
SA1458	±18	V
MC1558	±22	V
Internal power dissipation		
N package	500	mW
H package ¹	800	mW
F,FE package	1000	mW
Differential input voltage	±30	V
Input voltage ²	±15	V
Output short-circuit duration	Continuous	
Operating temperature range		
MC1458	0 to +70	°C
SA1458	-40 to +85	°C
MC1558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 60sec)	300	°C



NOTES

1. Ratings based on thermal resistances, junction to ambient, of 240°C/W, 150°C/W, 110°C/W for N, H, F and FE packages respectively, and a maximum junction temperature of 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC



GENERAL PURPOSE OPERATIONAL AMPLIFIER

MC/SA1458/MC1558

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MC1558			UNIT
		Min	Typ	Max	
V_{OS} Offset voltage	$R_S = 10\text{k}\Omega$ $R_S = 10\text{k}\Omega$, over temp.		1.0	5.0 6.0	mV mV
I_{OS} Offset current	Over temp.		20	200 500	nA nA
I_{BIAS} Input bias current	Over temp.		80	500 1500	nA nA
V_{OUT} Output voltage swing	$R_L = 10\text{k}\Omega$, over temp. $R_L = 2\text{k}\Omega$, over temp.	± 12 ± 10	± 14 ± 13		V V
A_{VOL} Large signal voltage gain	$R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$ $R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$, over temp.	50 20	100		V/mV V/mV
Offset voltage adjustment range			± 30		mV
PSRR Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$		30	150	$\mu\text{V}/\text{V}$
CMRR Common mode rejection ratio		70	90		dB
I_{CC} Supply current			2.3	5.0	mA
V_{IN} Input voltage range		± 12	± 13		V
P_d Power consumption			70	150	mW
R_{OUT} Channel separation			120		dB
I_{SC} Output resistance			75		Ω
			25		mA

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DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MC1458			SA1458			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	$R_S = 10\text{k}\Omega$ $R_S = 10\text{k}\Omega$, over temp.		2.0	6.0 7.5		2.0	6.0 7.5	mV mV
I_{OS} Offset current	Over temp.		20	200 300		20	200 500	nA nA
I_{BIAS} Input bias current	Over temp.		80	500 800		80	500 1500	nA nA
V_{OUT} Output voltage swing	$R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$, over temp.	± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13		V V
A_{VOL} Large signal voltage gain	$R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$ $R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$, over temp.	25 15	200		20 15	200		V/mV V/mV
Offset voltage adjustment range			± 30			± 30		mV
PSRR Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$		30	150		30	150	$\mu\text{V}/\text{V}$
CMRR Common mode rejection ratio		70	90		70	90		dB
I_{CC} Supply current			2.3	5.6		2.3	5.6	mA
V_{IN} Input voltage range		± 12	± 13		± 12	± 13		V
R_{IN} Input resistance								$M\Omega$
P_d Power consumption			70	170		70	170	mW
R_{OUT} Channel separation			120			120		dB
I_{SC} Output short-circuit current			25			25		mA

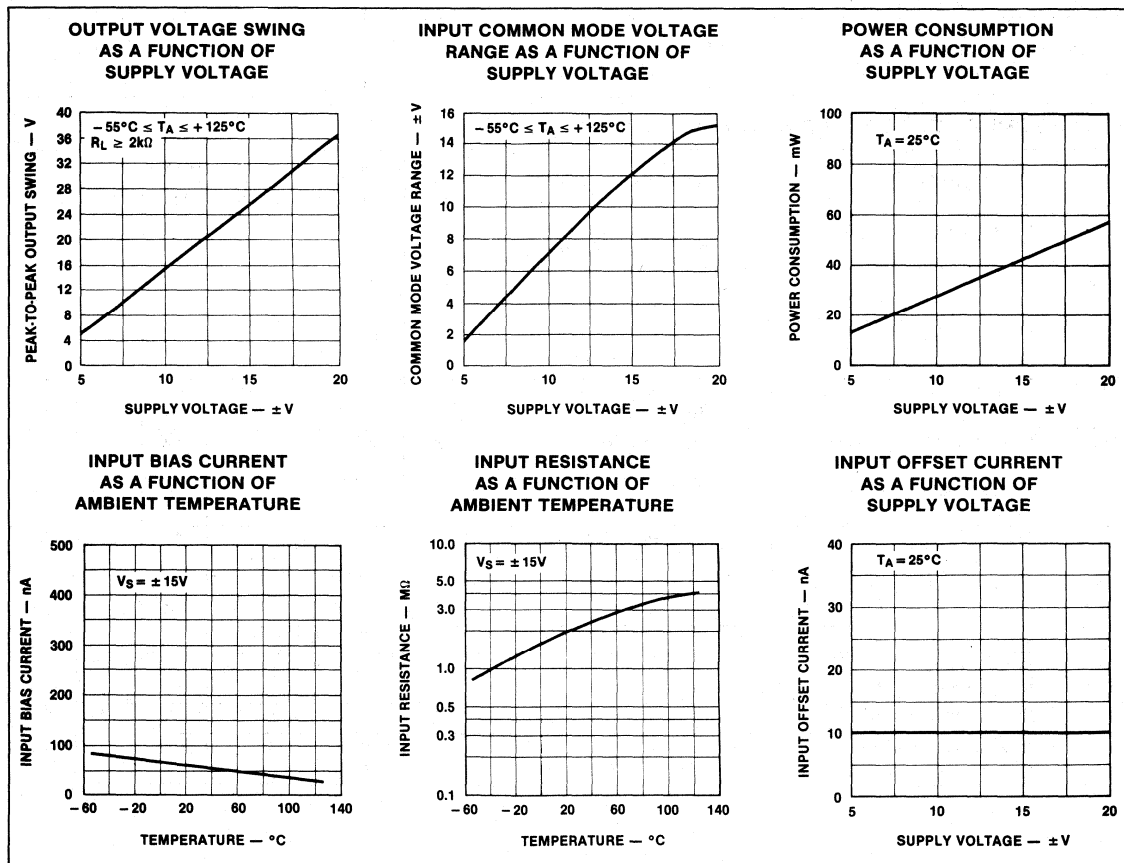
GENERAL PURPOSE OPERATIONAL AMPLIFIER

MC/SA1458/MC1558

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	MC1458, SA1458, MC1558			UNIT
		Min	Typ	Max	
Parallel input resistance	Open loop, $f = 20\text{Hz}$	0.3			$M\Omega$
Common mode input impedance	$f = 20\text{Hz}$		200		$M\Omega$
Equivalent input noise voltage	$A_V = 100$, $R_S = 10k\Omega$, $B_W = 1.0\text{kHz}$, $f = 1.0\text{kHz}$		45		$nV \sqrt{\text{Hz}}$
Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, $\text{THD} \leq 5\%$, $V_{\text{OUT}} = 20\text{Vp-p}$		14		kHz
Phase margin			65		degrees
Gain margin			11		dB
Unity gain crossover frequency	Open loop		1.0		MHz
Transient response unity gain	$V_{\text{IN}} = 20\text{mV}$, $R_L = 2k\Omega$, $C_L \leq 100\text{pF}$				
Rise time			0.3		μs
Overshoot			5.0		%
Slew rate	$C \leq 100\text{pF}$, $R_L \geq 2k$, $V_{\text{IN}} = \pm 10\text{V}$		0.8		$V/\mu\text{s}$

TYPICAL PERFORMANCE CHARACTERISTICS



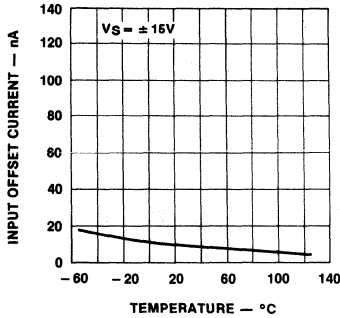
GENERAL PURPOSE OPERATIONAL AMPLIFIER

MC/SA1458/MC1558

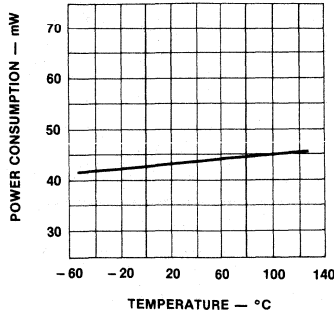
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

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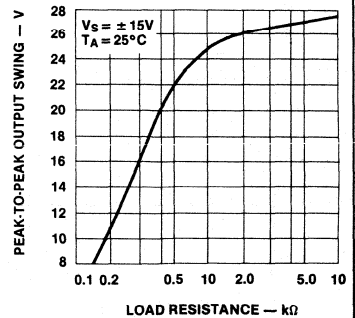
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



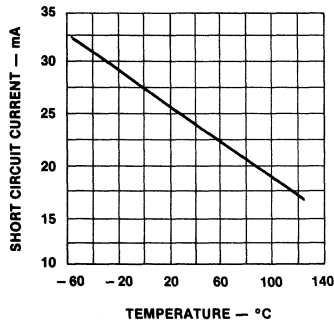
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



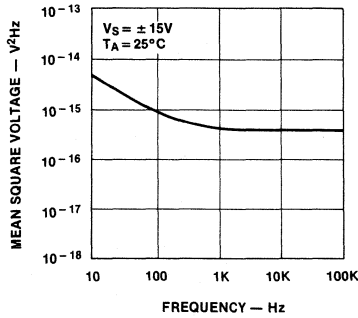
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



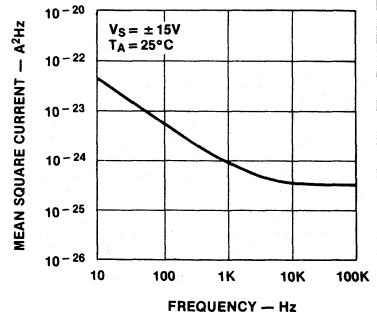
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



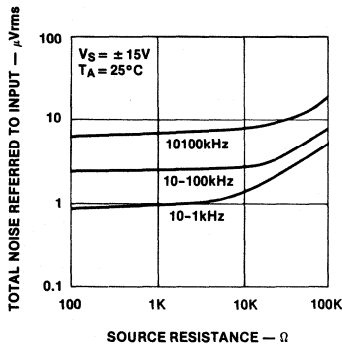
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



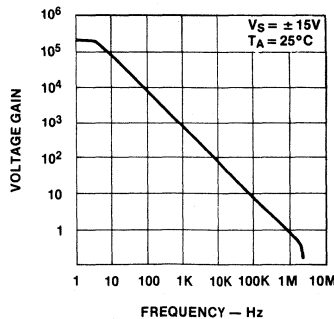
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



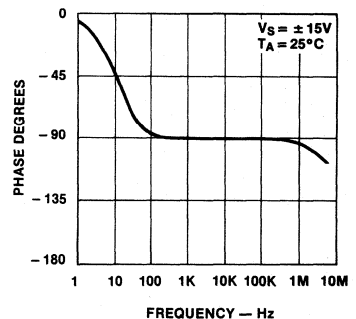
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

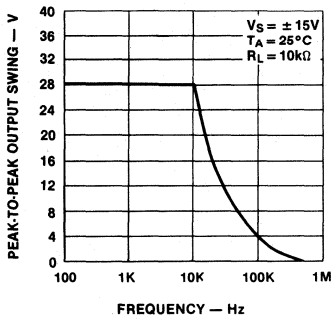


GENERAL PURPOSE OPERATIONAL AMPLIFIER

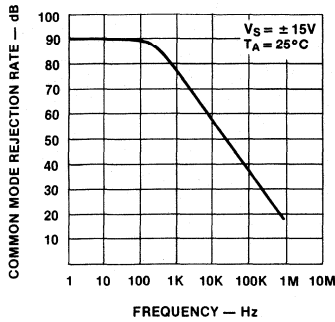
MC/SA1458/MC1558

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

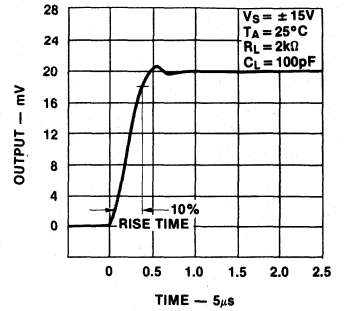
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



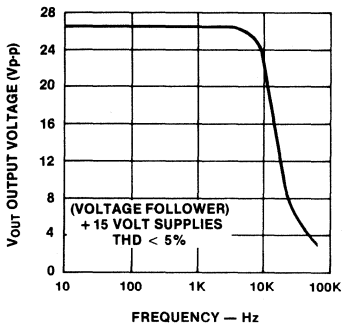
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH (Large Signal Swing vs Frequency)



QUAD LOW POWER OPERATIONAL AMPLIFIERS

MC3303/3403/3503

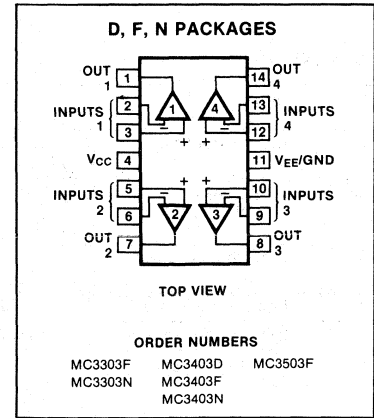
DESCRIPTION

The MC3403 is a quad operational amplifier with true differential inputs. The device has electrical characteristics similar to the popular μ A741. However, the MC3403 has several distinct advantages over standard operational amplifier types in single supply applications. The MC3403 can operate at supply voltages as low as 3.0V or as high as 36V. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications. The output voltage range also includes the negative power supply voltage.

FEATURES

- Short circuit protected outputs
- Class AB output stage for minimal cross-over distortion
- True differential input stage
- Single supply operation: 3.0 to 36V
- Split supply operation: ± 1.5 to ± 18 V
- Low input bias currents: 500nA max
- Four amplifiers per package
- Internally compensated

PIN CONFIGURATION



3

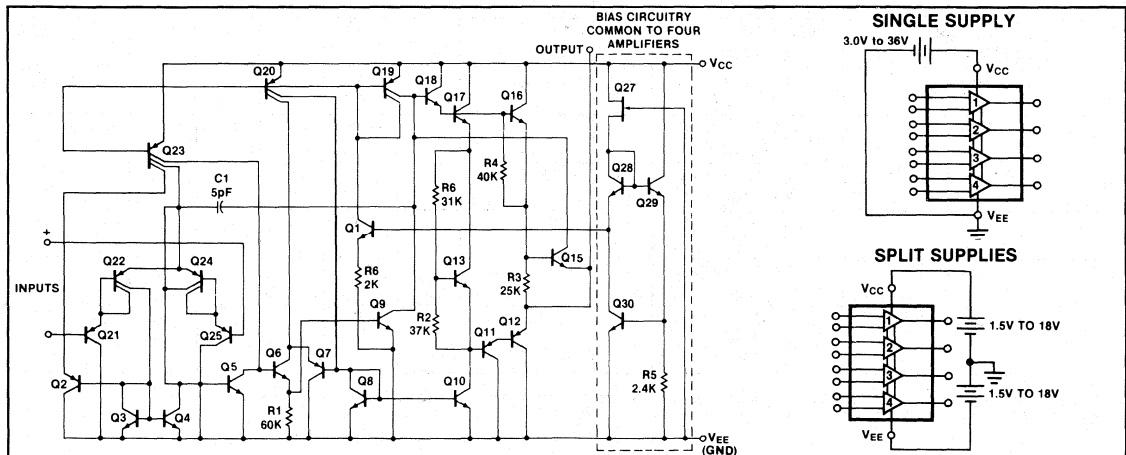
ABSOLUTE MAXIMUM RATINGS

SYMBOL AND PARAMETER	RATING	UNIT
Power supply voltages		
V_{CC} Single supply	36	Vdc
V_{CC} Split supplies	+ 18	Vdc
V_{EE}	- 18	Vdc
V_{IDR} Input differential voltage range ⁽¹⁾	± 36	Vdc
V_{ICR} Input common mode voltage range ^(1,2)	± 18	Vdc
Storage temperature range		
Ceramic package	- 65 to + 150	$^{\circ}$ C
Plastic package	- 55 to + 125	$^{\circ}$ C
Operating ambient temperature range		
MC3503	- 55 to + 125	$^{\circ}$ C
MC3403	0 to + 70	$^{\circ}$ C
MC3303	- 40 to + 85	$^{\circ}$ C
Junction temperature		
Ceramic package	175	$^{\circ}$ C
Plastic package	150	$^{\circ}$ C

NOTES

1. Split power supplies.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

CIRCUIT SCHEMATIC (1/4 Shown)



QUAD LOW POWER OPERATIONAL AMPLIFIERS

MC3303/3403/3503

ELECTRICAL CHARACTERISTICS ($V_{CC} = +15V$, $V_{EE} = -15V$ for MC3503, MC3403; $V_{CC} = +14V$, $V_{EE} = GND$ for MC3303.
 $T_A = 25^\circ C$ unless otherwise noted)

SYMBOL AND PARAMETER	TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO} Input offset voltage	$T_A = T_{HIGH}$ to $T_{LOW}^{(1)}$	—	2.0	5.0	—	2.0	10	—	2.0	8.0	mV
		—	—	6.0	—	—	12	—	—	10	
I_{IO} Input offset current	$T_A = T_{HIGH}$ to T_{LOW}	—	10	50	—	10	50	—	30	75	nA
		—	—	200	—	—	200	—	—	250	
A_{VOL} Large signal open-loop voltage gain	$V_O = \pm 10V$, $R_L = 2.0k\Omega$ $T_A = T_{HIGH}$ to T_{LOW}	50	200	—	20	200	—	20	200	—	V/mV
		25	300	—	15	—	—	15	—	—	
I_{IB} Input bias current	$T_A = T_{HIGH}$ to T_{LOW}	—	-30	-500	—	-30	-500	—	-30	-500	nA
		—	-40	-1200	—	—	-800	—	—	-1000	
z_o Output impedance	$f = 20Hz$	—	75	—	—	75	—	—	75	—	Ω
z_i Input impedance	$f = 20Hz$	0.3	1.0	—	0.3	1.0	—	0.3	1.0	—	M Ω
V_{OR} Output voltage range	$R_L = 10k\Omega$ $R_L = 2.0k\Omega$ $R_L = 2.0k\Omega$, $T_A = T_{HIGH}$ to T_{LOW}	± 12 ± 10 ± 10	± 13.5 ± 13 —	— — —	± 12 ± 10 ± 10	± 13.5 ± 13 —	— — —	+12 +10 +10	+12.5 +12 —	— — —	V
V_{ICR} Input common mode voltage range		+13V - V_{EE}	+13.5V - V_{EE}	—	+13V - V_{EE}	+13.5V - V_{EE}	—	+12V - V_{EE}	+12.5V - V_{EE}	—	V
CMRR Common mode rejection ratio	$R_S \leq 10k\Omega$	70	90	—	70	90	—	70	90	—	dB
I_{CC}, I_{EE} Power supply current ($V_O = 0$)	$R_L = \infty$	—	2.5	4.0	—	2.5	7.0	—	2.5	7.0	mA
$I_{OS\pm}$ Individual output short circuit current ⁽²⁾		± 10	± 30	± 45	± 10	± 20	± 45	± 10	± 30	± 45	mA
PSRR+ Positive power supply rejection ratio		—	30	150	—	30	150	—	30	150	$\mu V/V$
PSRR- Negative power supply rejection ratio		—	30	150	—	30	150	—	—	—	$\mu V/V$
$\Delta I_{IO}/\Delta T$ Average temperature coefficient of input offset current	$T_A = T_{HIGH}$ to T_{LOW}	—	50	—	—	50	—	—	50	—	pA/ $^\circ C$
$\Delta V_{IO}/\Delta T$ Average temperature coefficient of input offset voltage	$T_A = T_{HIGH}$ to T_{LOW}	—	10	—	—	10	—	—	10	—	$\mu V/^\circ C$
BW_P Power bandwidth	$A_V = 1$, $R_L = 2.0k\Omega$, $V_O = 20V(p-p)$ THD = 5%	—	9.0	—	—	9.0	—	—	9.0	—	kHz
BW Small signal bandwidth	$A_V = 1$, $R_L = 10k\Omega$, $V_O = 50mV$	—	1.0	—	—	1.0	—	—	1.0	—	MHz
SR Slew rate	$A_V = 1$, $V_i = -10V$ to $+10V$	—	0.6	—	—	0.6	—	—	0.6	—	V/ μs
t_{TLH} Rise time	$A_V = 1$, $R_L = 10k\Omega$, $V_O = 50mV$	—	0.35	—	—	0.35	—	—	0.35	—	μs
t_{THL} Fall time	$A_V = 1$, $R_L = 10k\Omega$, $V_O = 50mV$	—	0.35	—	—	0.35	—	—	0.35	—	μs
OS Overshoot	$A_V = 1$, $R_L = 10k\Omega$, $V_O = 50mV$	—	20	—	—	20	—	—	20	—	%
ϕ_m Phase margin	$A_V = 1$, $R_L = 2.0k\Omega$, $C_L = 200pF$	—	50	—	—	50	—	—	50	—	$^\circ$
— Crossover distortion	$V_{IN} = 30mV(p-p)$, $V_{OUT} = 2.0V(p-p)$, $f = 10kHz$	—	1.0	—	—	1.0	—	—	1.0	—	%

NOTES

- $T_{HIGH} = 125^\circ C$ for MC3503, $70^\circ C$ for MC3403, $85^\circ C$ for MC3303. $T_{LOW} = -55^\circ C$ for MC3503, $0^\circ C$ for MC3403, $-40^\circ C$ for MC3303.
- Not to exceed maximum package power dissipation.

QUAD LOW POWER OPERATIONAL AMPLIFIERS

MC3303/3403/3503

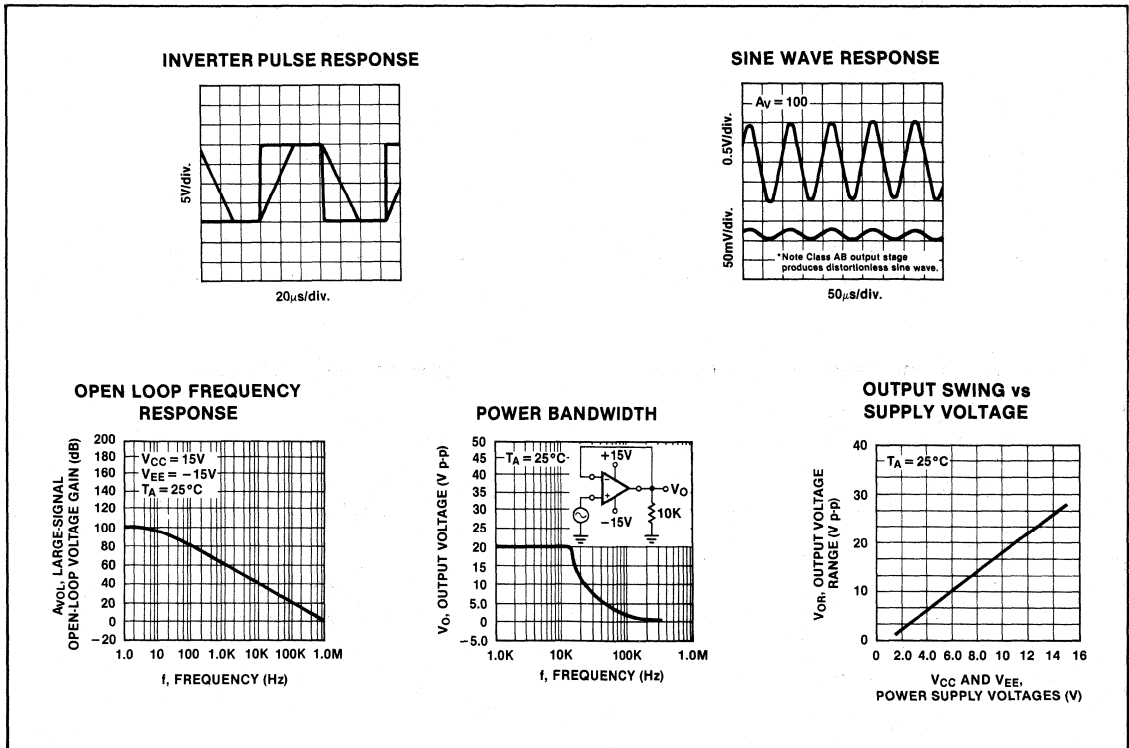
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V$, $V_E = GND$, $T_A = 25^\circ C$ unless otherwise noted.)

SYMBOL AND PARAMETER	TEST CONDITIONS	MC3503			MC3403			MC3303			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IO} Input offset voltage		—	2.0	5.0	—	2.0	10	—	—	10	mV
I_{IO} Input offset current		—	30	50	—	30	50	—	—	75	nA
I_{IB} Input bias current		—	-200	-500	—	-200	-500	—	—	-500	nA
A_{VOL} Large signal open-loop voltage gain	$R_L = 2.0k\Omega$	10	200	—	10	200	—	10	200	—	V/mV
PSRR Power supply rejection ratio		—	—	150	—	—	150	—	—	150	$\mu V/V$
V_{OR} Output voltage range ⁽³⁾	$R_L = 10k\Omega$, $V_{CC} = 5.0V$, $R_L = 10k\Omega$, $5.0V \leq V_{CC} \leq 30V$	3.3	3.5	—	3.3	3.5	—	3.3	3.5	—	Vp-p
I_{CC} Power supply current		—	2.5	4.0	—	2.5	7.0	—	2.5	7.0	mA
— Channel separation	$f = 1.0kHz$ to $20kHz$ (input referenced)	—	-120	—	—	-120	—	—	-120	—	dB

NOTE
3. Output will swing to ground.

3

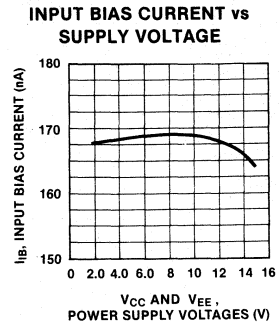
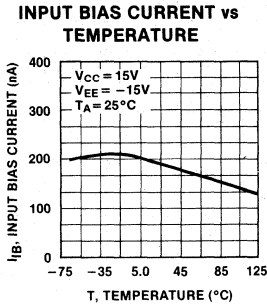
TYPICAL PERFORMANCE CURVES



QUAD LOW POWER OPERATIONAL AMPLIFIERS

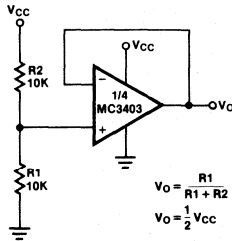
MC3303/3403/3503

TYPICAL PERFORMANCE CURVES (Continued)

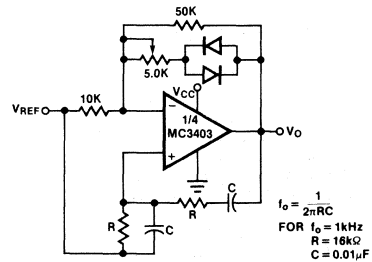


APPLICATIONS

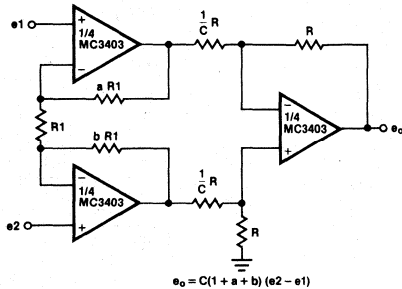
VOLTAGE REFERENCE



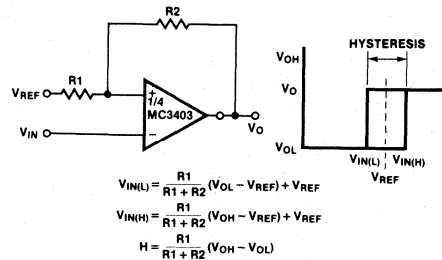
WEIN BRIDGE OSCILLATOR



HIGH IMPEDANCE DIFFERENTIAL AMPLIFIER



COMPARATOR WITH HYSTERESIS



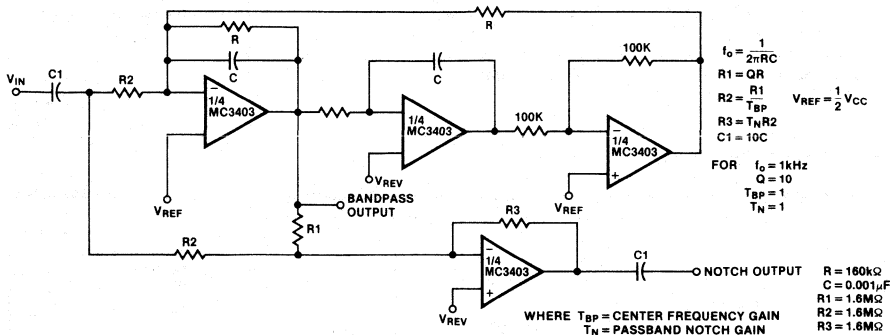
QUAD LOW POWER OPERATIONAL AMPLIFIERS

MC3303/3403/3503

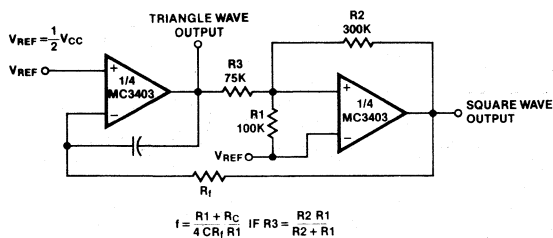
APPLICATIONS (Continued)

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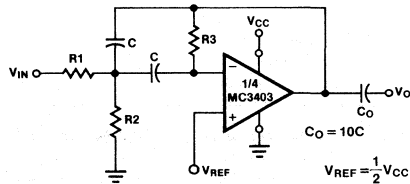
BI-QUAD FILTER



FUNCTION GENERATOR



MULTIPLE FEEDBACK BANDPASS FILTER



GIVEN f_o = CENTER FREQUENCY
 $A(f_o)$ = GAIN AT CENTER FREQUENCY

CHOOSE VALUE f_o, C

THEN:

$R3 = \frac{Q}{\pi f_o C}$

$R1 = \frac{R3}{2 A(f_o)}$

$R2 = \frac{R1 R5}{4Q^2 R1 - R5}$

FOR LESS THAN 10% ERROR FROM OPERATIONAL AMPLIFIER

$Q_o f_o < 0.1$ WHERE f_o AND BW ARE EXPRESSED IN HZ.
 BW

IF SOURCE IMPEDANCE VARIES, FILTER MAY BE PRECEDED WITH VOLTAGE FOLLOWER BUFFER TO STABILIZE FILTER PARAMETERS.

HIGH SLEW RATE OPERATIONAL AMPLIFIER

NE/SE530/5530

DESCRIPTION

The 530/5530 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated, the SE530/5530 guarantee slew rates of $25V/\mu s$ with 2mV maximum offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers such as the 741, 747, 1458, 4558 and LF356 types.

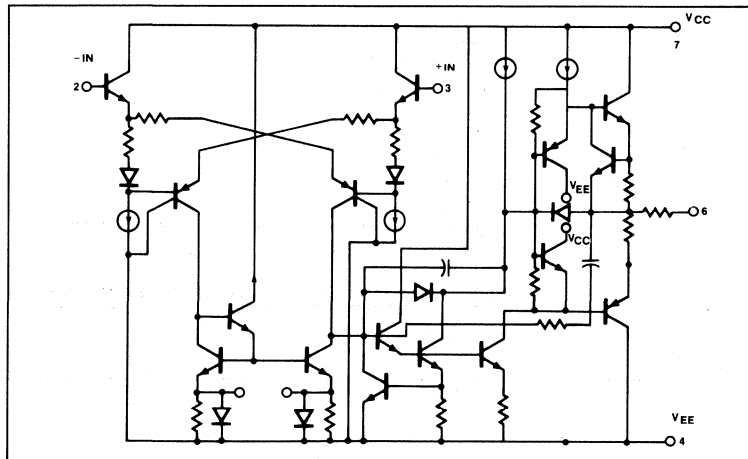
FEATURES

- Gain bandwidth product—3MHz
- $35V/\mu s$ slew rate (Gain = -1)
- Internal frequency compensation
- Low input offset voltage 2mV max
- Low input bias current—60nA max
- Short circuit protection
- Offset null capability
- Large common mode and differential voltage ranges

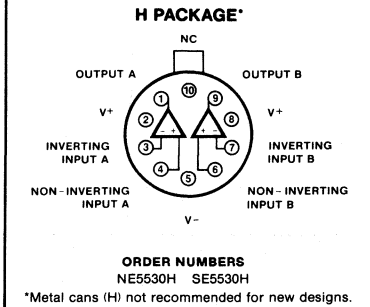
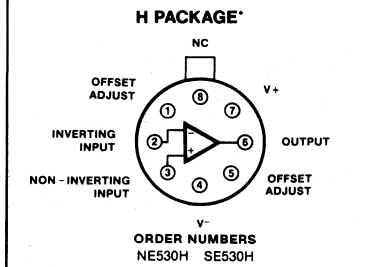
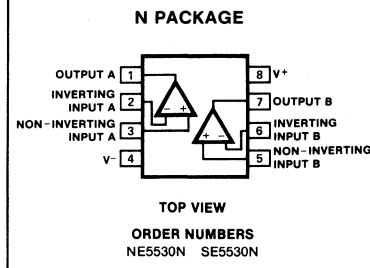
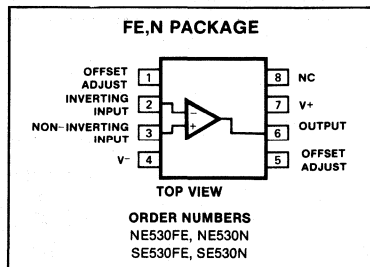
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE530/5530	± 22	V
NE530/5530	± 18	V
Internal power dissipation		
N Package	500	mW
H Package	800	mW
FE Package	1000	mW
Differential input voltage	± 30	V
Input voltage	± 15	V
Operating temperature range		
SE530/5530	-55 to +125	$^{\circ}C$
NE530/5530	0 to +70	$^{\circ}C$
Storage temperature range	-65 to +150	$^{\circ}C$
Lead temperature range	300	$^{\circ}C$
Output short circuit	Indefinite	

EQUIVALENT SCHEMATIC EACH AMPLIFIER



PIN CONFIGURATIONS



HIGH SLEW RATE OPERATIONAL AMPLIFIER

NE/SE530/5530

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$ unless otherwise specified.¹

PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$R_s \leq 10\text{k}\Omega$ Over temperature		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
Temperature coefficient of input offset voltage			3	15		6		$\mu\text{V}/^\circ\text{C}$
Input offset current	Over temperature		5	20 40		15	40 80	nA nA
Input bias current	Over temperature		45	80 200		65	150 200	nA nA
Input resistance		3	10		1	6		M Ω
Input voltage range		± 12	± 13		± 12	± 13		V
Large signal voltage gain	$R_L \geq 2\text{k}\Omega$, $V_0 = \pm 10\text{V}$ Over temperature	50 25	200		50 25	200		V/mV V/mV
Output voltage swing	$R_L \geq 10\text{k}\Omega$ $R_L \geq 2\text{k}\Omega$	± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13		V V V
Output short circuit current			25			25		mA
Output resistance			100			100		Ω
Supply current	Each amplifier Over temperature		2.0 2.2	3.0 3.6		2.0 2.2	3.0	mA mA
Common mode rejection ratio	$R_s \leq 10\text{k}\Omega$ Over temperature	70	90		70	90		dB
Power supply rejection ratio	$R_s \leq 10\text{k}\Omega$ Over temperature		30	150		30	150	$\mu\text{V}/\text{V}$

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient Response Small signal rise time Small signal overshoot Settling time	TO 0.1% (10V step)		.06 13 0.9			.06 13 0.9		μs % μs
Slew rate Unity gain inverting Unity gain non-inverting	$\pm 15\text{V}$ supply, $V_0 = \pm 10\text{V}$, $R_L \geq 2\text{k}\Omega$	25 18	35 25		20 12	35 25		V/ μs V/ μs
Power bandwidth	5% THD, $V_0 = \pm 10\text{V}$, $R_L \geq 2\text{k}\Omega$	360	500		280	500		kHz
Small signal bandwidth	Open loop		3			3		MHz
Channel separation			120			120		dB

NOTE

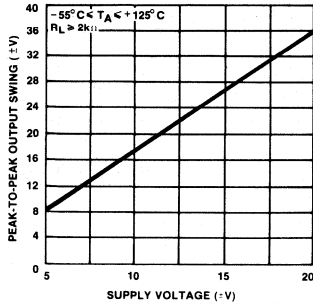
1. Operating temperature range for the SE530/5530 is -55°C to $+125^\circ\text{C}$.
Operating temperature range for the NE530/5530 is 0°C to $+70^\circ\text{C}$.

HIGH SLEW RATE OPERATIONAL AMPLIFIER

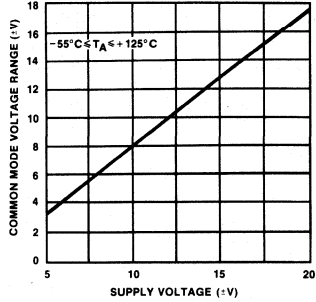
NE/SE530/5530

TYPICAL PERFORMANCE CHARACTERISTICS

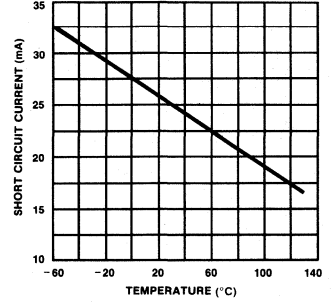
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



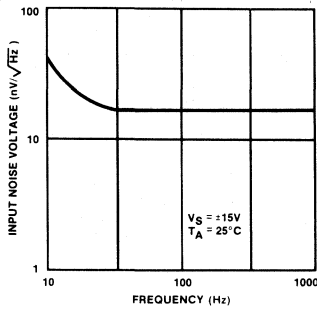
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



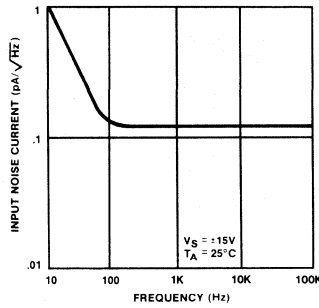
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



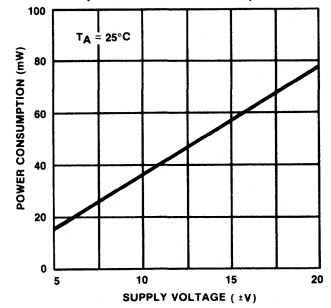
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



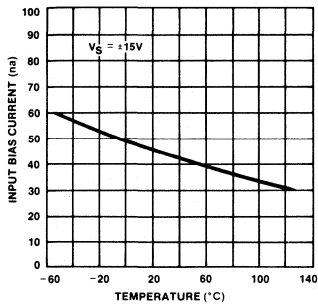
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



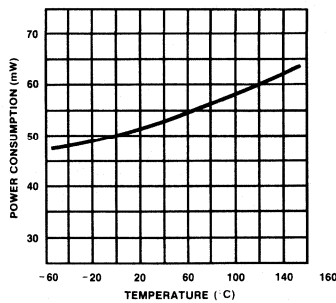
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE (EACH AMPLIFIER)



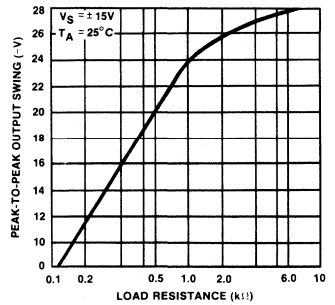
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE (EACH AMPLIFIER)



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



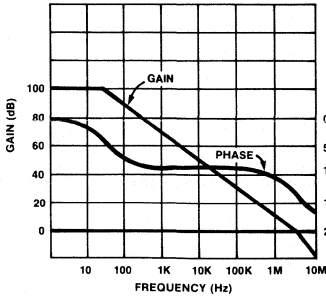
HIGH SLEW RATE OPERATIONAL AMPLIFIER

NE/SE530/5530

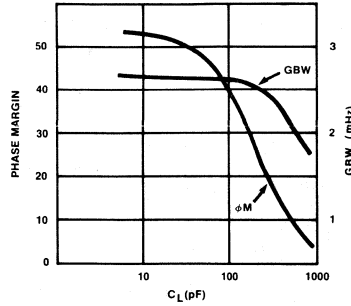
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

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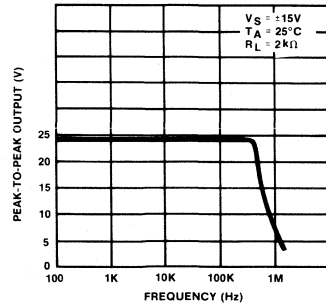
NE530 OPEN-LOOP GAIN AND PHASE vs FREQUENCY



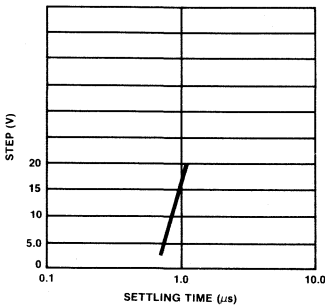
GAIN-BANDWIDTH PRODUCT AND PHASE MARGIN vs LOAD CAPACITANCE



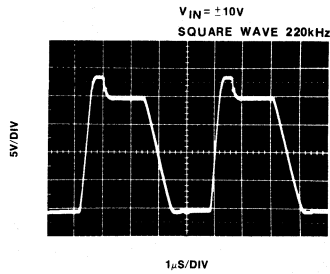
POWER BANDWIDTH



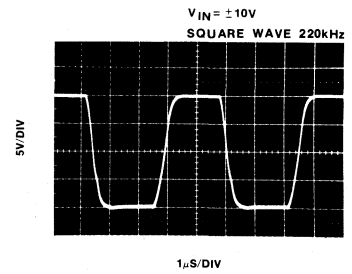
INPUT VOLTAGE STEP vs SETTLING TIME TO 10mV



SLEW RATE—VOLTAGE FOLLOWER

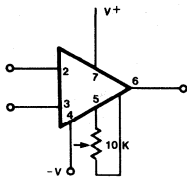


SLEW RATE (-1 AMPLIFIER)



TYPICAL CIRCUIT CONNECTION

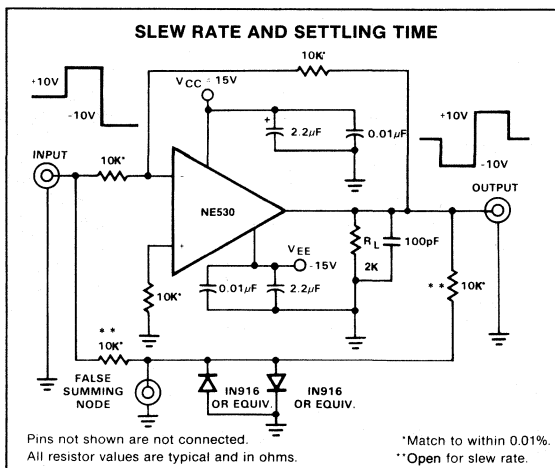
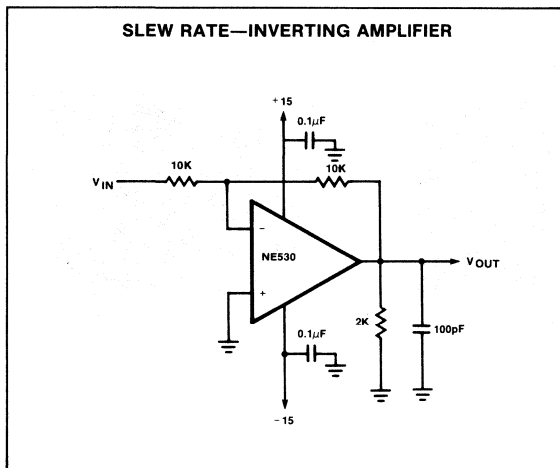
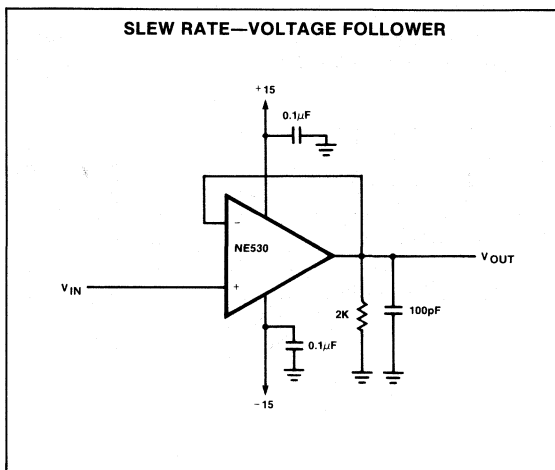
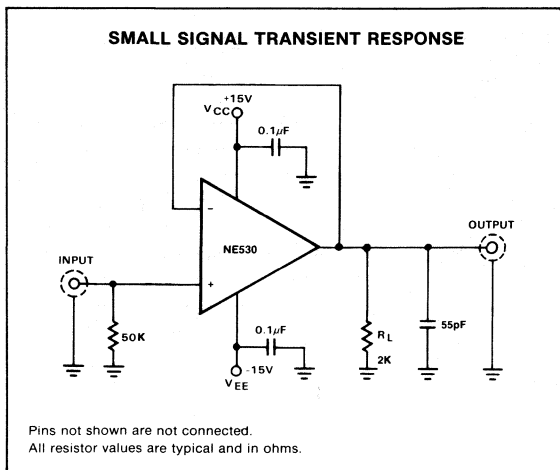
OFFSET ADJUST CIRCUIT



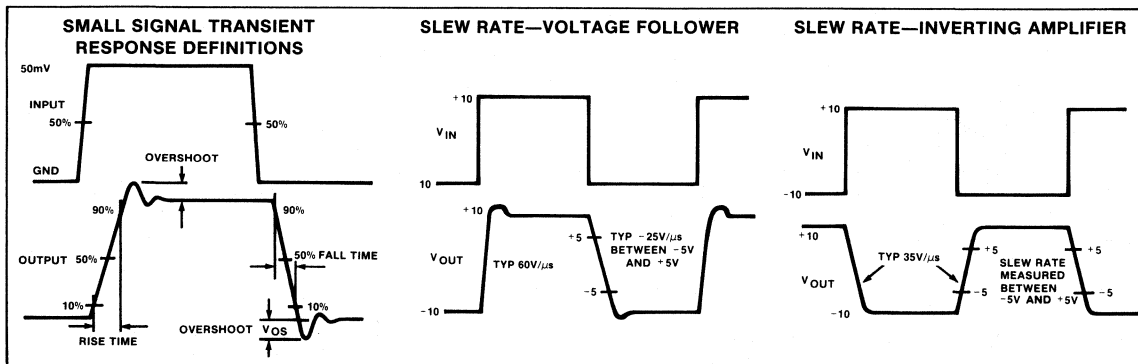
HIGH SLEW RATE OPERATIONAL AMPLIFIER

NE/SE530/5530

TEST LOAD CIRCUITS



VOLTAGE WAVEFORMS



HIGH SLEW RATE OPERATIONAL AMPLIFIER

NE/SE531

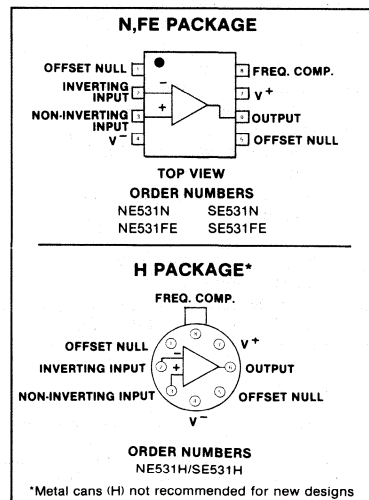
DESCRIPTION

The 531 is a fast slewing high performance operational amplifier which retains dc performance equal to the best general purpose types while providing far superior large signal ac performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier is compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

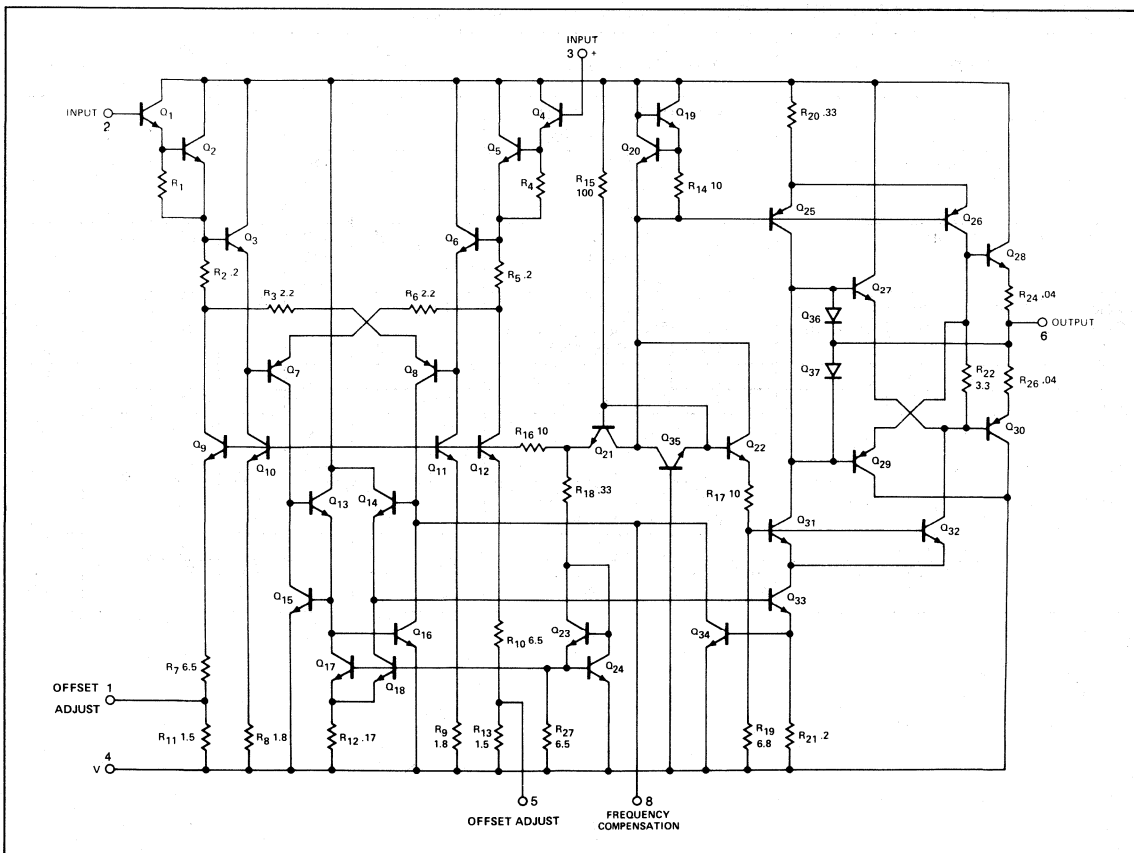
FEATURES

- 35V/ μ sec slew rate at unity gain
- Pin for pin replacement for μ A709, μ A748 or LM101
- Compensated with a single capacitor
- Same low drift offset null circuitry as μ A741
- Small signal bandwidth 1MHz
- Large signal bandwidth 500KHz
- True op amp dc characteristics make the 531 the ideal answer to all slew rate limited operational amplifier applications.

PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC



HIGH SLEW RATE OPERATIONAL AMPLIFIER

NE/SE531

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	±22	V
Internal power dissipation ¹	300	mW
Differential input voltage	±15	V
Common mode input voltage ²	±15	V
Voltage between offset null and V-	±0.5	V
Operating temperature range		
NE531	0 to +70	°C
SE531	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	300	°C
Output short circuit duration ³	indefinite	

NOTES

- Rating applies for case temperature to 125°C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
- For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or to +75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE531'			NE531			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	$R_S \leq 10k\Omega$, $T_A = 25^\circ C$ $R_S \leq 10k\Omega$, over temp		2.0	5.0 6.0		2.0	6.0 7.5	mV mV
I_{OS} Offset current	$T_A = 25^\circ C$ $T_A = HIGH$ $T_A = LOW$		30	200 200 500		50	200 200 300	nA nA nA
I_{BIAS} Input current	$T_A = 25^\circ C$ $T_A = HIGH$ $T_A = LOW$		300	500 500 1500		400	1500 1500 2000	nA nA nA
V_{CM} Common mode voltage range CMRR Common mode rejection ratio	$T_A = 25^\circ C$ $T_A = 25^\circ C$, $R_S \leq 10k\Omega$ Over temp $R_S \leq 10k\Omega$	±10			±10 70	100		V dB dB
R_{IN} Input resistance	$T_A = 25^\circ C$		20			20		M Ω
V_{OUT} Output voltage swing	$R_L \geq 10k\Omega$, over temp	±10	±13		±10	±13		V
I_{CC} Supply current	$T_A = 25^\circ C$ T_{MAX}			7.0 7.0			10 10	mA mA
P_D Power consumption	$T_A = 25^\circ C$			210			300	mW
PSRR Power supply rejection ratio	$R_S \leq 10k\Omega$, $T_A = 25^\circ C$ $R_S \leq 10k\Omega$, over temp		10	150		10	150	$\mu V/V$ $\mu V/V$
R_{OUT} Output resistance	$T_A = 25^\circ C$		75			75		Ω
A_{VOL} Large signal voltage gain	$T_A = 25^\circ C$, $R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$ $R_L \geq 10k\Omega$, $V_{OUT} = \pm 10V$, over temp	50 25	100		20 15	60		V/mV V/mV

NOTE

- Temperature range:
SE531 $-55^\circ C \leq T_A \leq 125^\circ C$
NE531 $0^\circ C \leq T_A \leq 70^\circ C$

HIGH SLEW RATE OPERATIONAL AMPLIFIER

NE/SE531

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

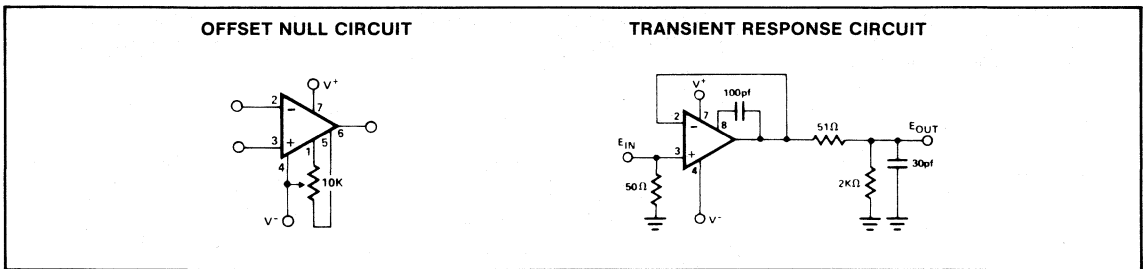
PARAMETER	TEST CONDITIONS	NE531			SE531			UNIT
		Min	Typ	Max	Min	Typ	Max	
Full power bandwidth			500			500		kHz
Settling time (1% (.01%))	$A_v = +1$, $V_{IN} = \pm 10\text{V}$		1.5 2.5			1.5 2.5		μs μs
Large signal overshoot	$A_v = +1$, $V_{IN} = \pm 10\text{V}$		2			2		%
Small signal overshoot	$A_v = +1$, $V_{IN} = 400\text{mV}$		5			5		%
Small signal risetime	$A_v = +1$, $V_{IN} = 400\text{mV}$		300			300		ns
Slew rate	$A_v = 100$		35			35		$\text{V}/\mu\text{s}$
	$A_v = 10$		35			35		$\text{V}/\mu\text{s}$
	$A_v = 1$ (noninverting)		30		20	30		$\text{V}/\mu\text{s}$
	$A_v = 1$ (inverting)		35		25	35		$\text{V}/\mu\text{s}$

3

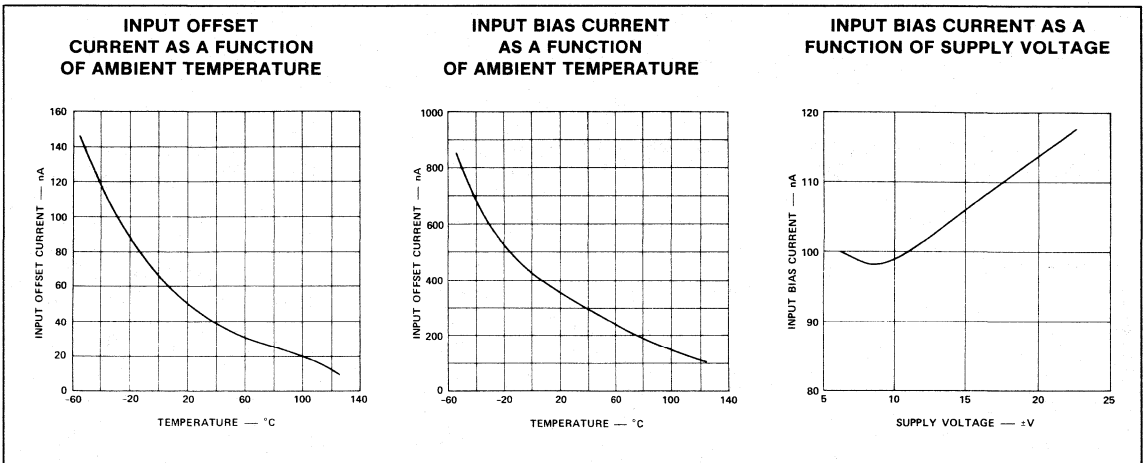
NOTE

1. All AC testing is performed in the transient response test circuit.

TEST LOAD CIRCUITS



TYPICAL PERFORMANCE CHARACTERISTICS $(V_S = \pm 15\text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise specified.)

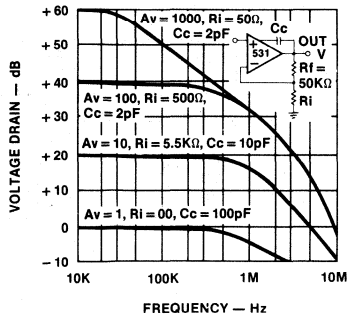


HIGH SLEW RATE OPERATIONAL AMPLIFIER

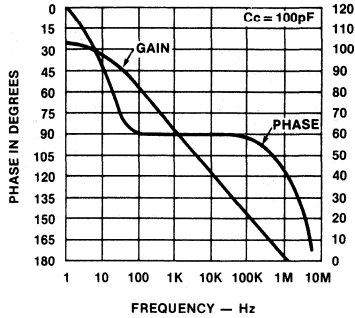
NE/SE531

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

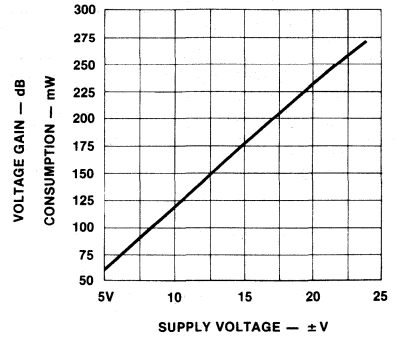
CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



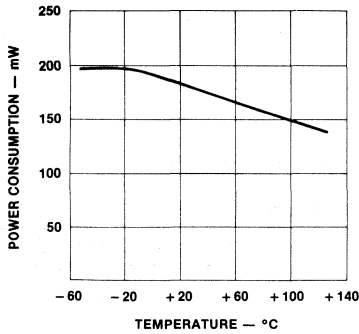
OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



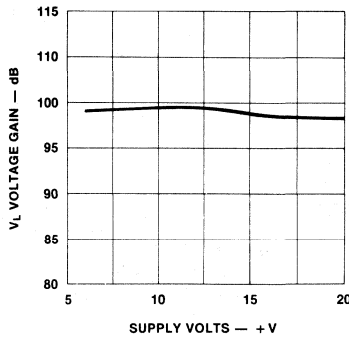
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



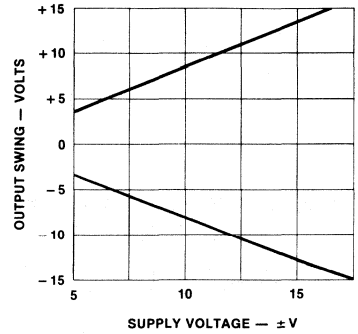
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



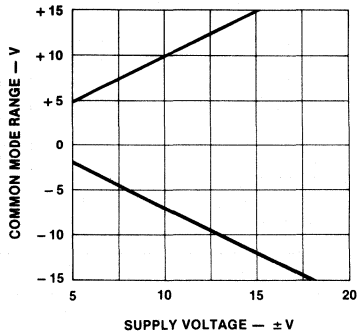
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



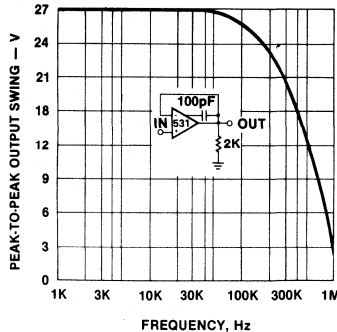
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



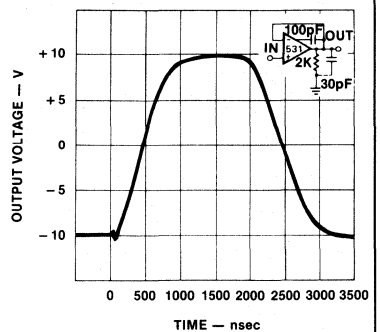
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE

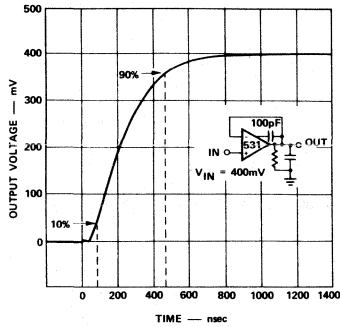


HIGH SLEW RATE OPERATIONAL AMPLIFIER

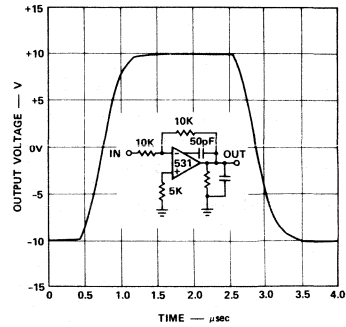
NE/SE531

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

**VOLTAGE FOLLOWER
TRANSIENT RESPONSE**



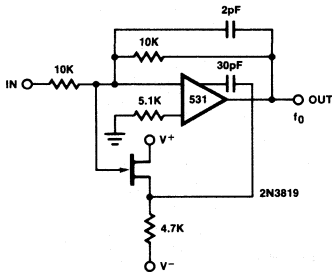
**UNITY GAIN INVERTING
AMPLIFIER LARGE SIGNAL
RESPONSE**



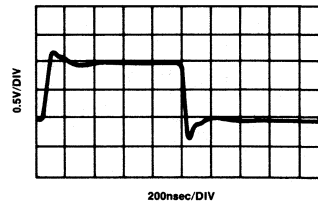
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TYPICAL APPLICATIONS

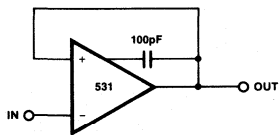
**HIGH SPEED INVERTER
(10MHz BANDWIDTH)**



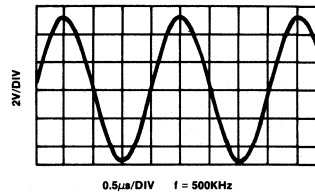
**PULSE RESPONSE
HIGH SPEED INVERTER**



FAST SETTLING VOLTAGE FOLLOWER



**LARGE SIGNAL RESPONSE
VOLTAGE FOLLOWER**

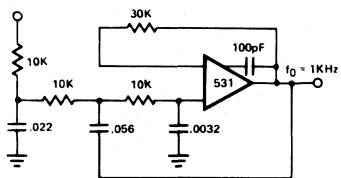


HIGH SLEW RATE OPERATIONAL AMPLIFIER

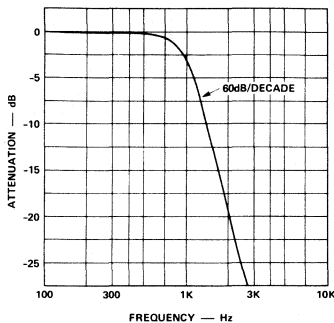
NE/SE531

TYPICAL APPLICATIONS (Cont'd)

POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*



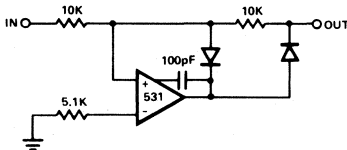
RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER



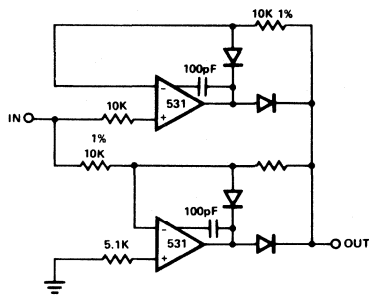
*Reference—EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokaw

PRECISION RECTIFIERS

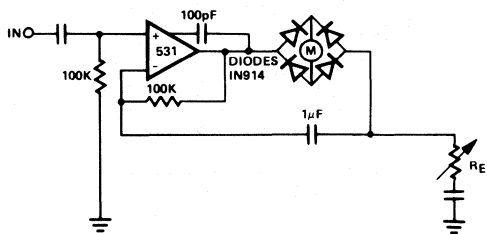
(a) HALF WAVE



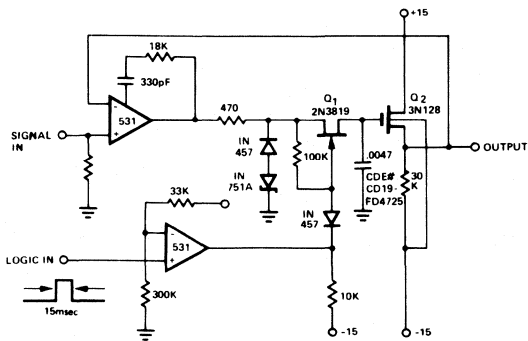
(b) FULL WAVE



AC MILLIVOLTMETER



SAMPLE AND HOLD



LOW POWER DUAL OPERATIONAL AMPLIFIERS NE/SA/SE532/LM158/258/358

DESCRIPTION

The 532/358 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

- Internally frequency compensated for unity gain
- Large dc voltage gain—(100dB)
- Wide bandwidth (unity gain)—1MHz (temperature compensated)
- Wide power supply range
single supply—(3Vdc to 30Vdc)
or dual supplies—(±1.5Vdc to ±15Vdc)
- Very low supply current drain (400 μ A)—essentially independent of supply voltage (1mW/op amp at +5Vdc)
- Low input biasing current—(45nA dc temperature compensated)
- Low input offset voltage—(2mVdc) and offset current—(5nA dc)

- Differential input voltage range equal to the power supply voltage
- Large output voltage—(0Vdc to V+—1.5Vdc swing)
- SE532 MIL-STD-883A,B,C available

UNIQUE FEATURES

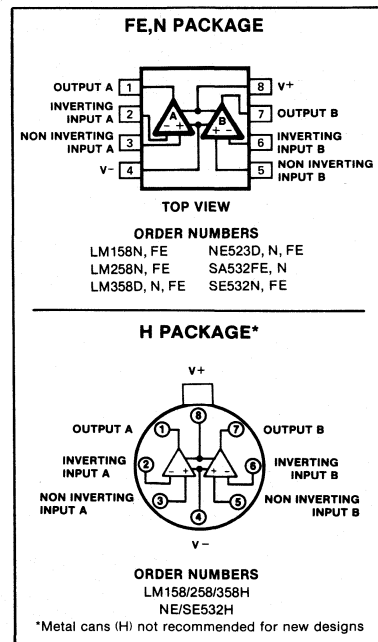
In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.



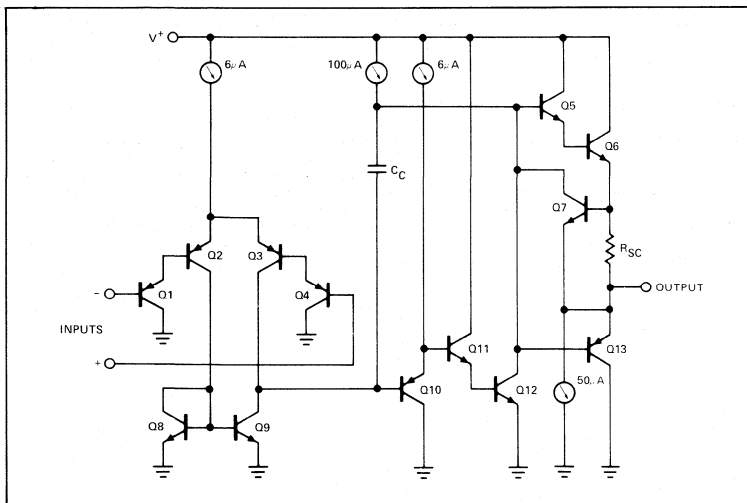
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V+	32 or ±16	Vdc
Differential input voltage	32	Vdc
Input voltage	-0.3 to +32	Vdc
Power dissipation ¹		
FE package	900	mW
H package	680	mW
N package	500	mW
Output short-circuit to GND ⁵ V+ < 15 Vdc and T _A = 25°C	Continuous	
Operating temperature range		
NE532/LM358	0 to +70	°C
LM258	-25 to +85	°C
SA532N	-40 to +85	°C
SE532/LM158	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

PIN CONFIGURATIONS



EQUIVALENT CIRCUIT



LOW POWER DUAL OPERATIONAL AMPLIFIERS NE/SA/SE532/LM158/258/358

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_+ = +5\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE532, LM158/258			NE/SA532/LM358			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage ¹	$R_S \leq 0\Omega$ $R_S \leq 0\Omega$, over temp.		± 2	± 5 ± 7		± 2	± 7 ± 9	mV mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7			7		$\mu\text{V}/^\circ\text{C}$
I_{OS} Offset current	$I_{IN(+)} - I_{IN(-)}$ Over temp.		± 3	± 30 ± 100		± 5	± 50 ± 150	nA nA
I_{OS} Drift			10			10		$\text{pA}/^\circ\text{C}$
I_{BIAS} Input current ²	$I_{IN(+)}$ or $I_{IN(-)}$ Over temp., $I_{IN(+)}$ or $I_{IN(-)}$		45 40	150 300		45 40	250 500	nA nA
V_{CM} Common mode voltage range ³	$V_+ = 30\text{V}$ Over temp., $V_+ = 30\text{V}$	0 0		$V_+ - 1.5$ $V_+ - 2.0$	0 0		$V_+ - 1.5$ $V_+ - 2.0$	V V
$CMRR$ Common mode rejection ratio		70	85		65	70		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \geq 2\text{k}\Omega$, $V_+ = 30\text{V}$, over temp	26			26			V
V_{OUT} Output voltage swing (V_{OL})	$R_L \geq 10\text{k}\Omega$, $V_+ = 30\text{V}$, over temp	27	28		27	28		V
	$R_L \leq 10\text{k}\Omega$, over temp.		5	20		5	20	mV
I_{CC} Supply current	$R_L = \infty$, $V_+ = 30\text{V}$ $R_L = \infty$ on all amplifiers, over temp		1.0 0.5	2.0 1.2		1.0 0.5	2.0 1.2	mA mA
A_{VOL} Large signal voltage Gain	$R_L \geq 2\text{k}\Omega$, $V_{OUT} \pm 10\text{V}$, $V_+ = 15\text{V}$ (for large V_O swing) Over temp.	50 25	100		25 15	100		V/mV V/mV
$PSRR$ Supply voltage rejection ratio	$R_S \leq 0\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling ⁴	$f = 1\text{kHz}$ to 20kHz (input referred)		-120			-120		dB
Output current Source	$V_{IN+} = +1\text{Vdc}$, $V_{IN-} = 0\text{Vdc}$, $V_+ = 15\text{Vdc}$	20	40		20	40		mA
Sink	$V_{IN+} = +1\text{Vdc}$, $V_{IN-} = 0\text{Vdc}$, $V_+ = 15\text{Vdc}$, over temp.	10	20		10	20		mA
	$V_{IN-} = +1\text{Vdc}$, $V_{IN+} = 0\text{Vdc}$, $V_+ = 15\text{Vdc}$	10	20		10	20		mA
	$V_{IN-} = +1\text{Vdc}$, $V_{IN+} = 0\text{Vdc}$, $V_+ = 15\text{Vdc}$, over temp.	5	8		5	8		mA
	$V_{IN+} = 0\text{V}$, $V_{IN-} = +1\text{Vdc}$, $V_O = 200\text{mV}$	12	50		12	50		μA
I_{SC} Short circuit current ⁵			40	60		40	60	mA
Differential input voltage ⁶				V_+			V_+	V

NOTES

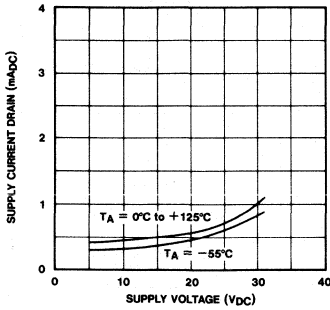
- $V_O \approx 1.4\text{V}$, $R_S = 0\Omega$ with V_+ from 5V to 30V ; and over the full input common-mode range (0V to $V_+ - 1.5\text{V}$).
- The direction of the input current is out of the IC due to the pnp input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V . The upper end of the common-mode voltage range is $V_+ - 1.5\text{V}$, but either or both inputs can go to $+32\text{V}$ without damage.
- Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance coupling increases at higher frequencies.
- Short circuits from the output to V_+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V_+ . At values of supply voltage in excess of $+15\text{Vdc}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction.
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V . The upper end of the common-mode voltage range is $V_+ - 1.5\text{V}$, but either or both inputs can go to $+32\text{Vdc}$ without damage.
- For operating at high temperatures, all devices must be derated based on a $+125^\circ\text{C}$ maximum junction temperature and a thermal resistance of $175^\circ\text{C}/\text{W}$ which applies for the device soldered in a printed circuit board, operating in a still air ambient.

LOW POWER DUAL OPERATIONAL AMPLIFIERS NE/SA/SE532/LM158/258/358

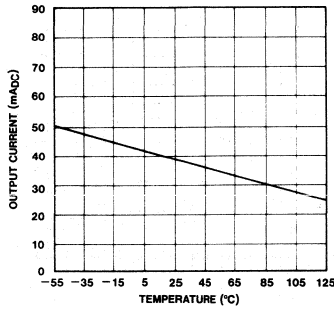
TYPICAL PERFORMANCE CHARACTERISTICS

3

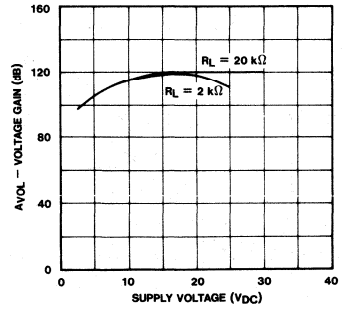
SUPPLY CURRENT



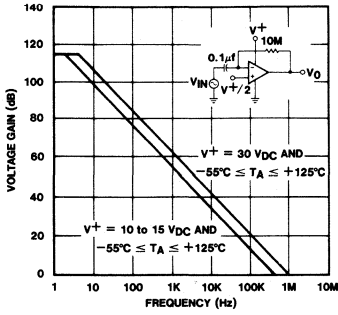
CURRENT LIMITING



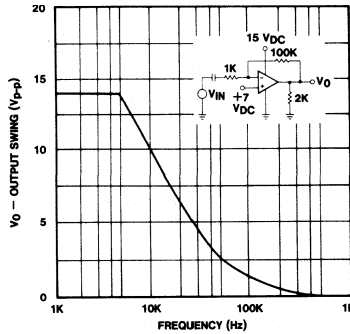
VOLTAGE GAIN



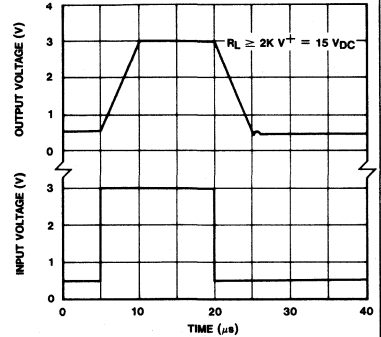
OPEN LOOP FREQUENCY RESPONSE



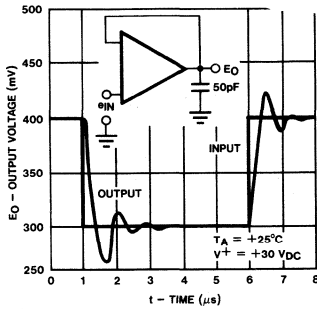
LARGE SIGNAL FREQUENCY RESPONSE



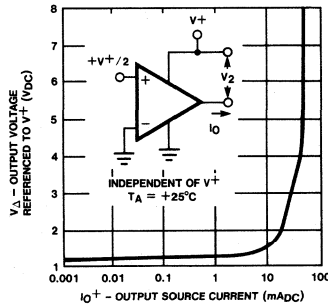
VOLTAGE FOLLOWER PULSE RESPONSE



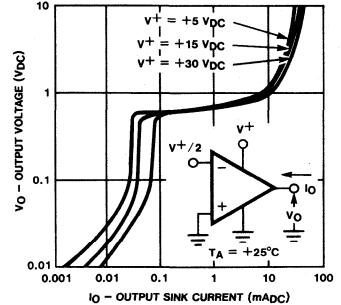
VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)



OUTPUT CHARACTERISTICS CURRENT SOURCING

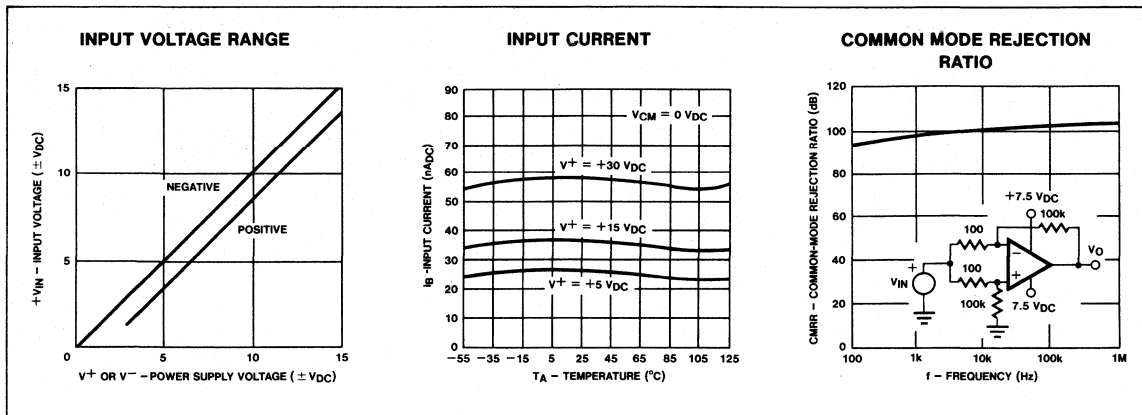


OUTPUT CHARACTERISTICS CURRENT SINKING



LOW POWER DUAL OPERATIONAL AMPLIFIERS NE/SA/SE532/LM158/258/358

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER

NE/SA/SE4558

DESCRIPTION

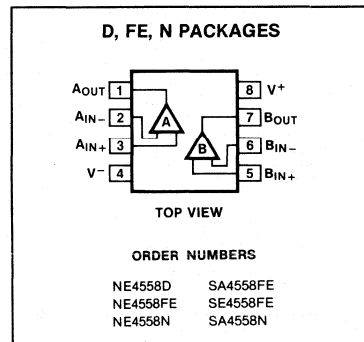
The 4558 is a dual operational amplifier internally compensated. The use of planar epitaxial process for silicon chip construction gives the IC unique performance characteristics.

Excellent channel separation allows the use of a dual device in a single amp application, providing the highest packaging density. The NE/SA/SE4558 is a pin for pin replacement for the RC/RM/RV4558.

FEATURES

- 2.5MHz unity gain bandwidth guaranteed
- Supply voltage $\pm 22V$ for SE4558 and $\pm 18V$ for NE4558
- Short circuit protection
- No frequency compensation required
- No latch-up
- Large common mode and differential voltage ranges
- Low power consumption

PIN CONFIGURATION



3

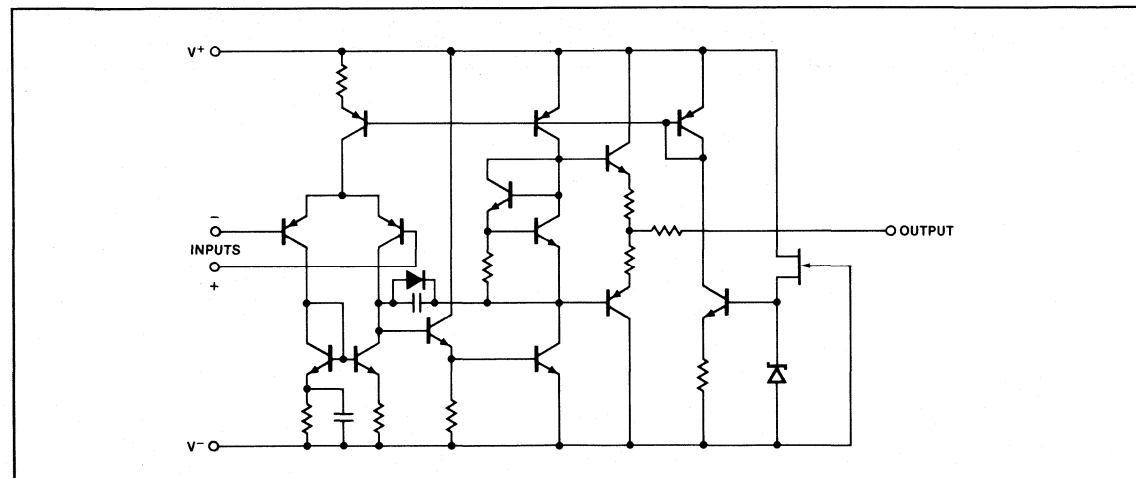
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE4558:	± 22	V
NE4558, SA4558:	± 18	V
Internal power dissipation (Note 1)	500	mW
Differential input voltage	± 30	V
Input voltage (Note 2)	± 15	V
Storage temperature range	- 65 to + 150	$^{\circ}C$
Operating temperature range		
SE4558:	- 55 to + 125	$^{\circ}C$
SA4558:	- 40 to + 85	$^{\circ}C$
NE4558:	0 to + 70	$^{\circ}C$
Lead temperature (soldering, 60s)	300	$^{\circ}C$
Output short circuit duration (Note 3)	Indefinite	

NOTES

1. Rating applies for case temperatures to + 125 $^{\circ}C$; derate linearly at 5.6 mW/ $^{\circ}C$ for ambient temperatures above + 75 $^{\circ}C$ for SE4558.
2. For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground on one amp only. Rating applies to + 125 $^{\circ}C$ case temperature or + 75 $^{\circ}C$ ambient temperature for NE4558 and to + 85 $^{\circ}C$ ambient temperature for SA4558.

EQUIVALENT SCHEMATIC



DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER

NE/SA/SE4558

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25^\circ C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE4558			NE/SA4558			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input offset current			50	200		30	200	nA
Input bias current			40	500		200	500	nA
Input resistance		0.3	1.0		0.3	1.0		M Ω
Large signal voltage gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	50,000	300,000		20,000	300,000		
Output voltage swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$	± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13		V
Input voltage range		± 12	± 13		± 12	± 13		V
Common mode rejection ratio	$R_S \leq 10k\Omega$	70	100		70	100		dB
Supply voltage rejection ratio	$R_S \leq 10k\Omega$		10	150		10	150	$\mu V/V$
Power consumption (all amplifiers)	$R_L = \infty$		100	170		100	170	mW
Transient response (unity gain)	$V_{IN} = 20mV$ $R_L = 2k\Omega$ $C_L \leq 100pF$							
Risettime			100			100		ns
Overshoot			15.0			15.0		%
Slew rate (unity gain)	$R_L \geq 2k\Omega$		1.0			1.0		V/ μs
Channel separation (gain = 100)	$f = 10kHz$ $R_S = 1k\Omega$		90			90		dB
Unity gain bandwidth (gain = 1)		2.5	3.0		2.0	3.0		MHz

The following specifications apply for $-55^\circ C \leq T_A \leq +125^\circ C$ for SE4558; $0^\circ C \leq T_A \leq +70^\circ C$ for NE4558; $-40^\circ C \leq T_A \leq +85^\circ C$ for SA4558

Input offset voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input offset current				500			300/500*	nA
Input bias current				1500			800/1500*	nA
Large signal voltage gain	$R_L \geq 2k\Omega$ $V_{OUT} = \pm 10V$	25,000			15,000			
Output voltage swing	$R_L \geq 2k\Omega$	± 10			± 10			V
Power consumption	$V_S = \pm 15V$ $T_A = HIGH$ $T_A = LOW$		90 120	150 200		90 120	150 200	mW

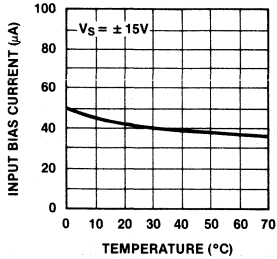
*SA4558

DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER

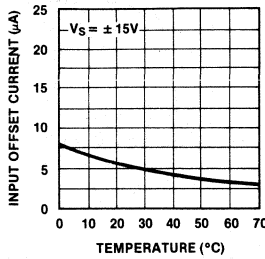
NE/SA/SE4558

TYPICAL PERFORMANCE CURVES

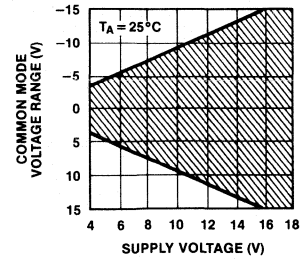
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



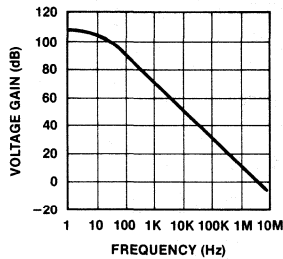
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



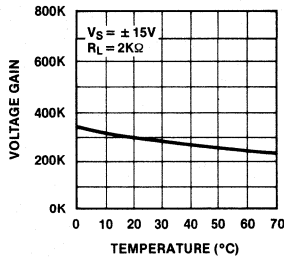
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



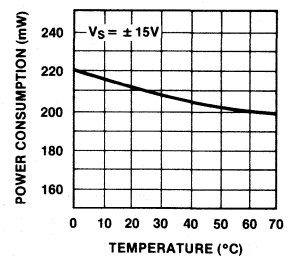
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



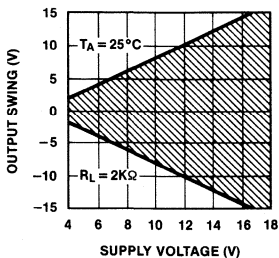
OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE



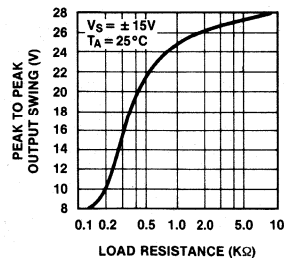
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



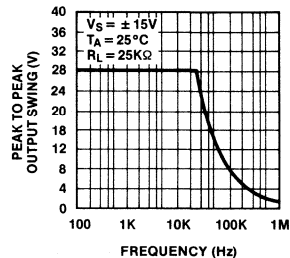
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



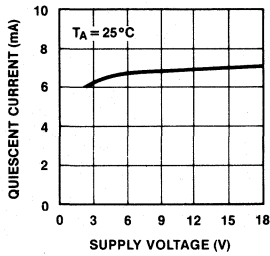
3

DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIER

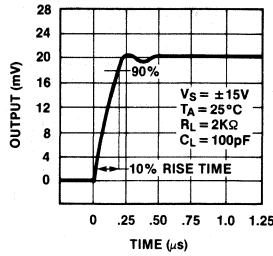
NE/SA/SE4558

TYPICAL PERFORMANCE CURVES (Continued)

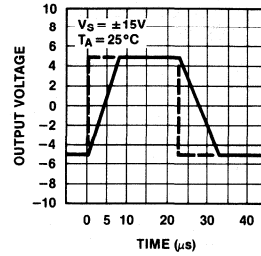
QUIESCENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



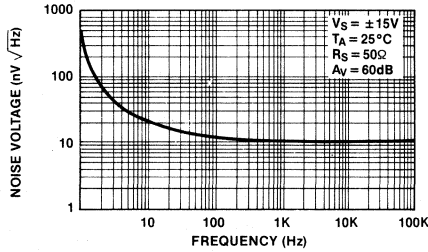
TRANSIENT RESPONSE



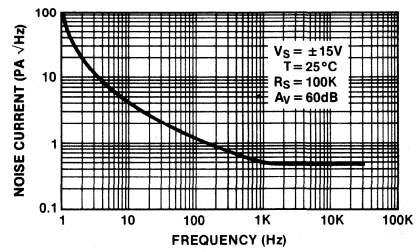
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



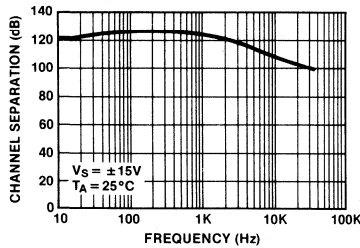
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



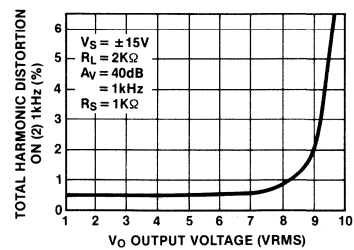
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



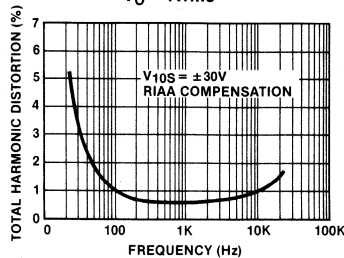
CHANNEL SEPARATION



TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE



DISTORTION vs FREQUENCY
 $V_O = 1\text{vrms}$



SINGLE OR DUAL HIGH SLEW RATE OP AMP

NE/SE535/5535

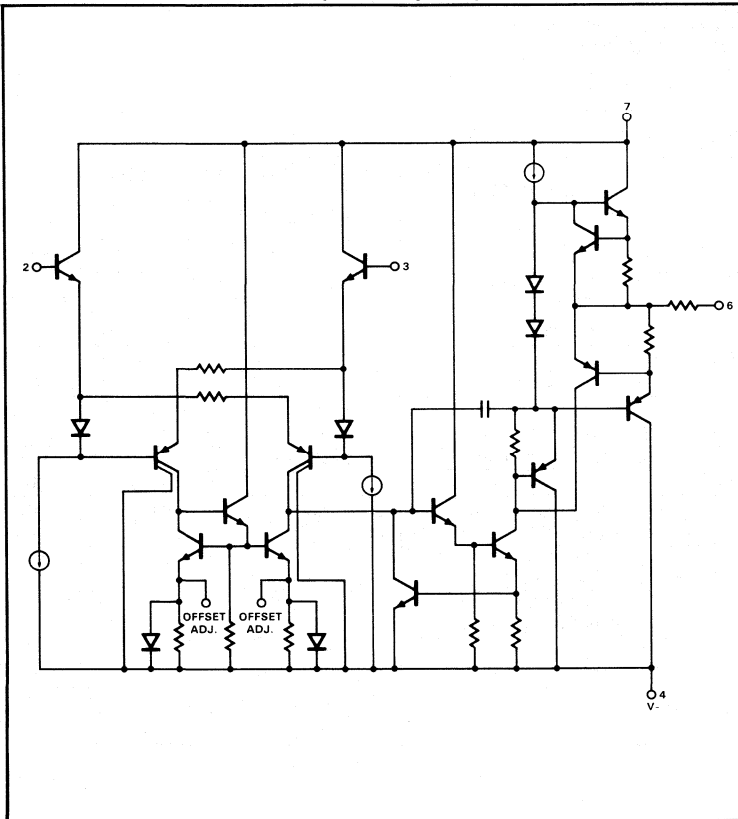
DESCRIPTION

The 535 and 5535 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. The 535 is a single device while the 5535 is a dual configuration. Internally compensated for unity gain, the SE535 and SE5535 feature a guaranteed unity gain slew rate of $10V/\mu s$ with 2mV maximum offset voltage. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 741, 747 and 1558.

FEATURES

- $15V/\mu s$ unity gain slew rate
 - Internal frequency compensation
 - Low input offset voltage—2mV
 - Low input bias current 80nA max
 - Short circuit protected
 - Offset null capability
 - Large common mode and differential voltage ranges
 - Pin compatibility
- | | | |
|-----------------|------------|-----------------|
| | 535 | 5535 |
| | 741 | 747,1558 |
| • Configuration | Single | Dual |

EQUIVALENT SCHEMATIC (One Amplifier)



PIN CONFIGURATIONS

FE, N PACKAGE

TOP VIEW

ORDER NUMBERS
SE535N, FE NE535N, FE

N PACKAGE

TOP VIEW

ORDER NUMBERS
SE5535N NE5535N

H PACKAGE*

ORDER NUMBERS
SE535H NE535H

H PACKAGE*

ORDER NUMBERS
SE5535H NE5535H

*Metal cans (H) not recommended for new designs



SINGLE OR DUAL HIGH SLEW RATE OP AMP

NE/SE535/5535

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SE535/ SE5535	NE535/ NE5535	UNIT
Supply voltage	±22	±18	V
Internal power dissipation ¹			
N Package	500	500	mW
H Package	800	800	mW
F Package	1000	1000	mW
Differential input voltage	±30	±30	V
Input voltage ²	±15	±15	V
Operating temperature range	-55 to +125	0 to +70	°C
Storage temperature range	-65 to +150	-65 to +150	°C
Lead temperature (solder, 60sec)	300	300	°C
Output short circuit ³	Indefinite	Indefinite	

NOTES

- Rating applies for thermal resistances junction to ambient of 240°C/W and 150°C/W for N and H packages, respectively. Maximum chip temperature is 150°C.
- For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

DC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V unless otherwise specified.*

PARAMETER	TEST CONDITIONS	SE535/SE5535			NE535/NE5535			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Input offset voltage	R _S ≤ 10kΩ R _S ≤ 10kΩ, over temp.		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
ΔV _{OS} Input offset voltage drift	R _S = 0Ω, over temp.		4.0			6.0		μV/°C
I _{OS} Input offset current	Over temp.		5	20 40		15	40 80	nA VnA
I _B Input current	Over temp.		45	80 200		65	150 200	nA nA
V _{CM} Common mode voltage range	R _S ≤ 10kΩ, over temp.	±12	±13		±12	±13		V
CMRR Common mode rejection ratio		70	90		70	90		dB
PSRR Power supply rejection	R _S ≤ 10kΩ, over temp.		30	150		30	150	μV/V
R _{IN} Input resistance		3	10		1	6		MΩ
A _{VOL} Large signal voltage gain	R _L ≥ 2kΩ, V _{OUT} = ±10V R _L ≥ 2kΩ, V _{OUT} = ±10V, over temp.	50	500		50	500		V/mV V/mV
V _{OUT} Output voltage	R _L ≥ 2kΩ, over temp. R _L ≥ 10kΩ, over temp.	±10 ±12	±13 ±14		±10 ±12	±13 ±14		V V
I _{CC} Supply current	Per amplifier Per amplifier, over temp.		1.8 2	2.8 3.3		1.8 2	2.8	mA mA
P _D Power dissipation	Per amplifier Per amplifier, over temp.		54 60	84 99		54 60	84	mW mW
I _{SC} Output short circuit current			25			25		mA
R _{OUT} Output resistance			100			100		Ω

*NOTE

Temperature range

SE types -55°C ≤ T_A ≤ 125°CNE types 0°C ≤ T_A ≤ 70°C

SINGLE OR DUAL HIGH SLEW RATE OP AMP

NE/SE535/5535

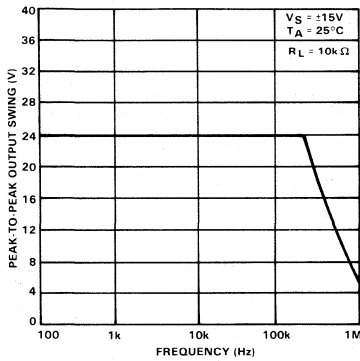
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE535/SE5535			NE535/NE5535			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain/bandwidth product			1			1		MHz
Transient response	To 0.1% $R_L \geq 10k\Omega$, unity gain, non-inverting		0.25			0.25		μs
Small signal rise time			6			6		%
Small signal overshoot			3			3		μs
Settling time			10	15		10	15	$\text{V}/\mu\text{s}$
Slew rate								

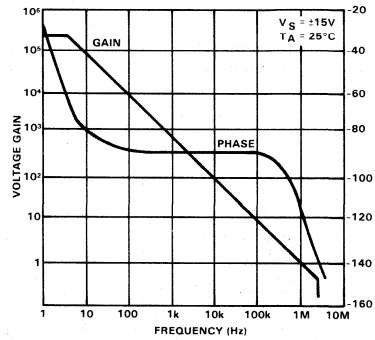
3

TYPICAL PERFORMANCE CHARACTERISTICS

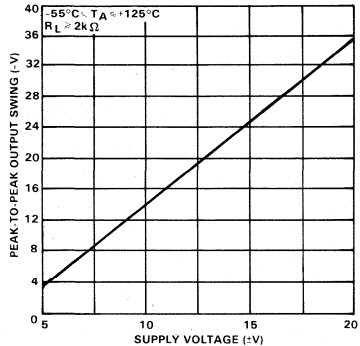
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



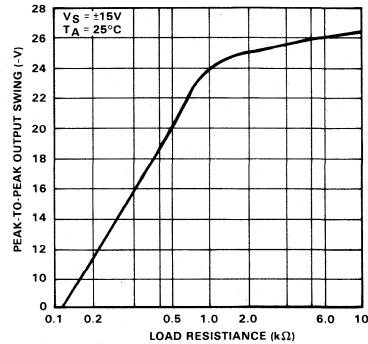
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

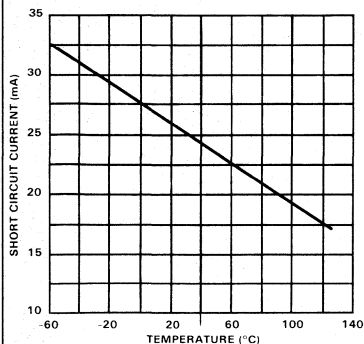


SINGLE OR DUAL HIGH SLEW RATE OP AMP

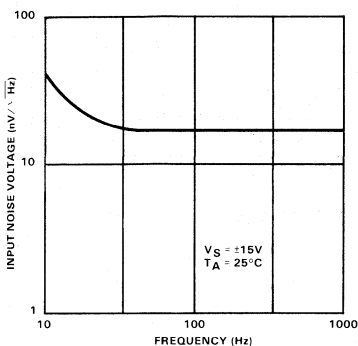
NE/SE535/535

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

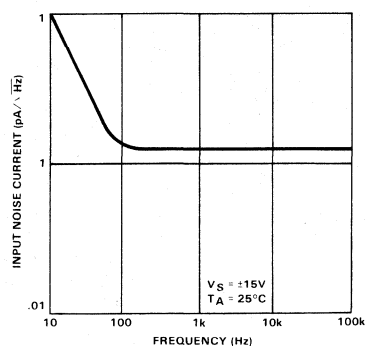
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



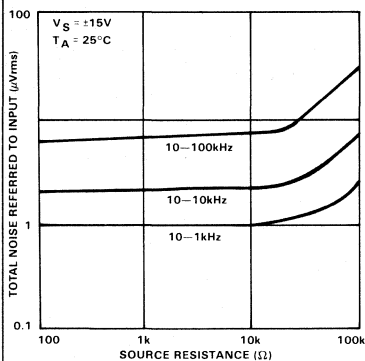
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



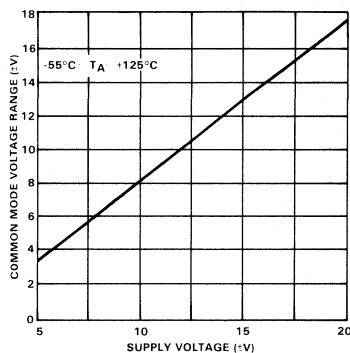
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



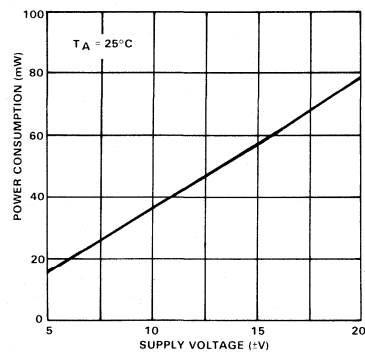
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



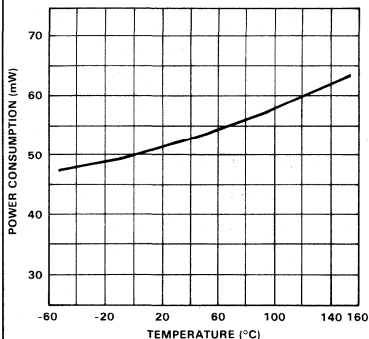
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



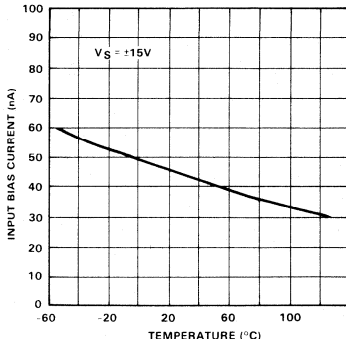
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



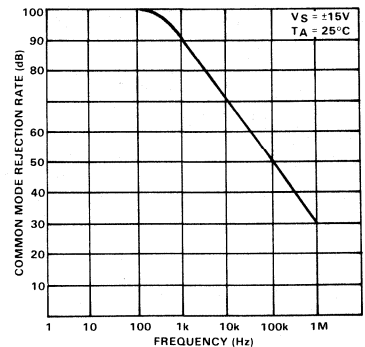
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

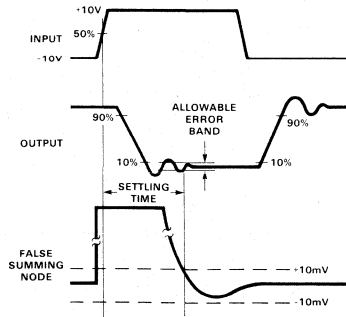


SINGLE OR DUAL HIGH SLEW RATE OP AMP

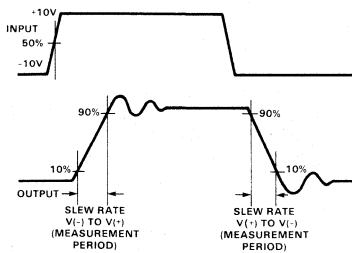
NE/SE535/5535

VOLTAGE WAVEFORMS

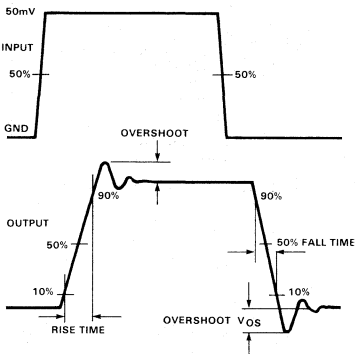
SETTLING TIME MEASUREMENT



SLEW RATE MEASUREMENT

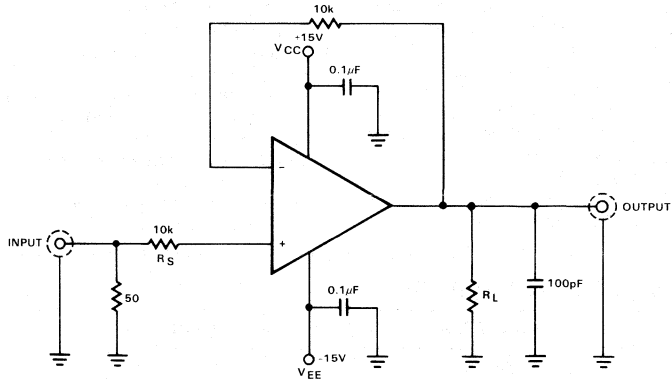


SMALL-SIGNAL TRANSIENT RESPONSE DEFINITIONS



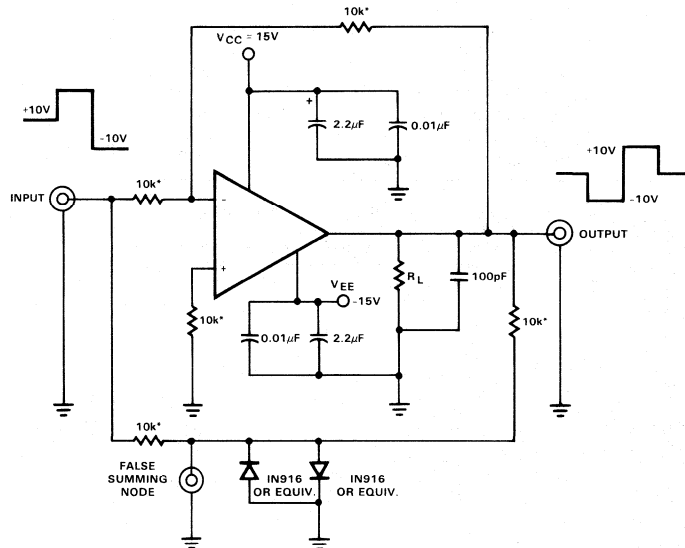
TEST CIRCUITS

SLEW RATE AND SMALL SIGNAL TRANSIENT RESPONSE



NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

SETTLING TIME



*Match to within 0.01%.
NOTE
Pins not shown are not connected.
All resistors values are typical and in ohms.

DUAL HIGH SLEW RATE OP AMPS

NE/SE538/5538

DESCRIPTION

The NE/SE538/5538 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated for gains of 5 or larger, the SE538/5538 offers guaranteed minimum slew rates of 40V/ μ s or larger. Featuring 2mV max input offset voltage, the 538 is a single amplifier while the 5538 is a dual amplifier. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A, 741, 747 and 1458.

FEATURES

- 2mV input offset voltage
- 80nA max input offset current
- Short circuit protected
- Offset null capability
- Large common mode and differential voltage ranges
- 60V/ μ s slew rate (gain of +5, -4 min)
- 6MHz gain bandwidth product (gain +5, -4 minimum)
- Internal frequency compensation (gain of +5, -4 minimum)
- Pin out: 538 same as 741 (single)
5538 same as 747, 1458 (dual)

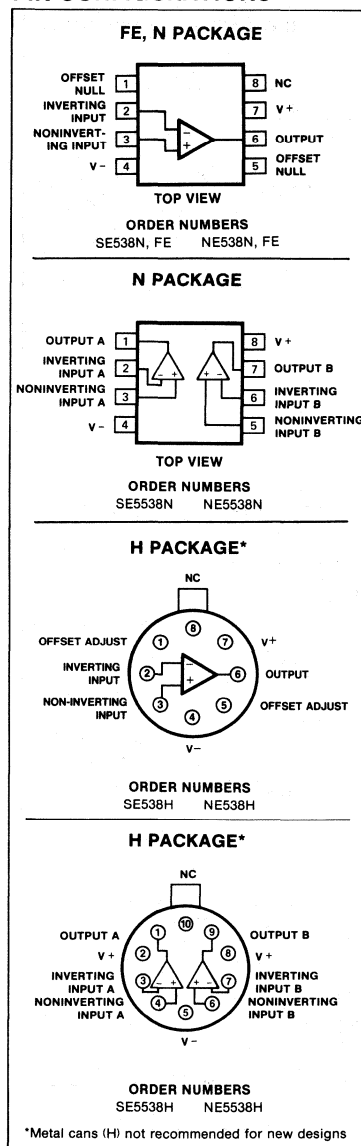
ABSOLUTE MAXIMUM RATINGS^{1,2,3}

PARAMETER	RATING	UNIT
V _{CC} Supply voltage		
SE military grade	± 22	V
NE commercial grade	± 18	V
P _D Internal power dissipation	1000	mW
P _D FE package		
Internal power dissipation ¹	500	mW
N package		
P _D Internal power dissipation ¹	800	mW
H package		
Differential input voltage	± 30	V
Input voltage ²	± 15	V
Operating temperature range		
SE military grade	-55 to +125	$^{\circ}$ C
NE commercial grade	0 to 70	$^{\circ}$ C
Output short circuit ³	indefinite	
Storage temperature range	-65 to +150	$^{\circ}$ C
Lead temperature (solder, 60sec.)	300	$^{\circ}$ C

NOTES

1. Rating applies for thermal resistances of 240 $^{\circ}$ C/W and 150 $^{\circ}$ C/W junction to ambient for N and H packages. Maximum chip temperature is 150 $^{\circ}$ C.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125 $^{\circ}$ C case temperature or 75 $^{\circ}$ C ambient temperature.

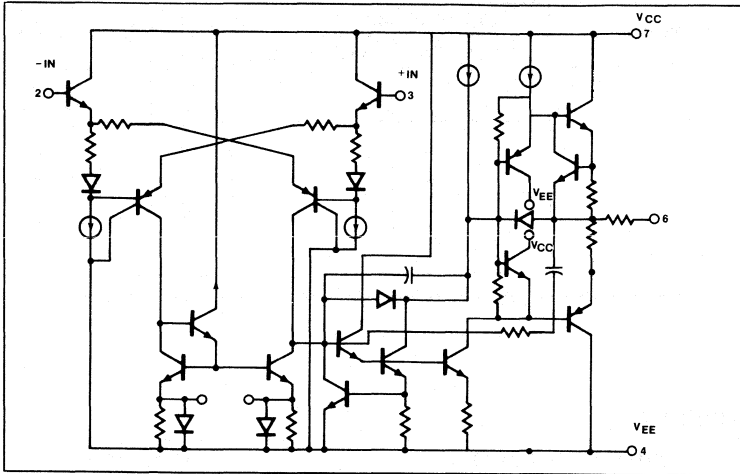
PIN CONFIGURATIONS



DUAL HIGH SLEW RATE OP AMPS

NE/SE538/5538

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



3

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE538/SE5538			NE538/NE5538			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{os} Input offset voltage	$R_S \leq 10\text{k}\Omega$ $R_S \leq 10\text{k}\Omega$, over temp.		0.7	4.0 5.0		2.0	6.0 7.0	mV mV
ΔV_{os} Input offset voltage drift	$R_S = 0\Omega$, over temp.		4.0			6.0		$\mu\text{V}/^\circ\text{C}$
I_{os} Input offset current	Over temp.		5	20 40		15	40 80	nA nA
I_b Input current	Over temp.		45	80 200		65	150 200	nA nA
V_{CM} Input common mode voltage range		± 12	± 13		± 12	± 13		V
CMRR Common mode rejection ratio	$R_S \leq 10\text{k}\Omega$, over temp.	70	90		70	90		dB
PSRR Power supply rejection	$R_S \leq 10\text{k}\Omega$, over temp.		30	150		30	150	$\mu\text{V}/\text{V}$
R_{IN} Input resistance		3	10		1	6		$\text{M}\Omega$
A_{VOL} Large signal voltage gain	$R_L \geq 2\text{k}\Omega$, $V_{OUT} = \pm 10\text{V}$ Over temp., $R_L \geq 2\text{k}\Omega$, $V_{OUT} = \pm 10\text{V}$	50 25	200		50 25	200		V/mV V/mV
V_{OUT} Output voltage	Over temp., $R_L \geq 2\text{k}\Omega$ Over temp., $R_L \geq 10\text{k}\Omega$	± 10 ± 12	± 13 ± 14		± 10 ± 12	± 13 ± 14		V V
I_{CC} Supply current	Per amplifier Over temp., per amplifier		2 2.2	3 3.6		2 2.2	3	mA mA
P_D Power dissipation	Per amplifier Over temp., per amplifier		60 66	90 108		60 66	90	mW mW
I_{SC} Output short circuit current			25			25		mA
R_{OUT} Output resistance			100			100		Ω

NOTE

Temperature Range
 SE Types $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$
 NE Types $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$

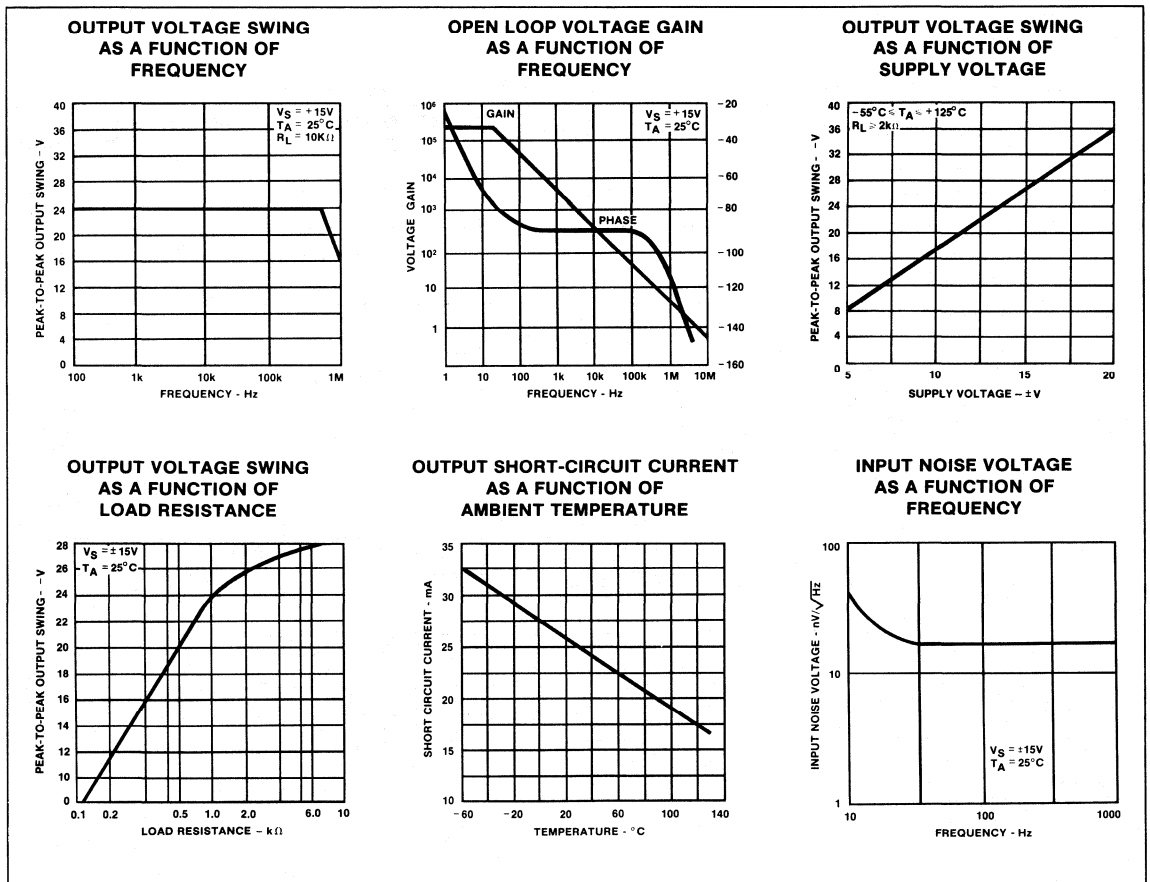
DUAL HIGH SLEW RATE OP AMPS

NE/SE538/5538

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE538/SE5538			SE538/NE5538			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product (Gain +5, -4 minimum)			6			6		MHz
Transient response Small signal rise time Small signal overshoot			0.25 6			0.25 6		μs %
Settling time	To 0.1%		1.2			1.2		μs
Slew rate	Minimum gain = 5 Noninverting $R_L \geq 2\text{k}\Omega$	40	60			60		$\text{V}/\mu\text{s}$

TYPICAL PERFORMANCE CHARACTERISTICS



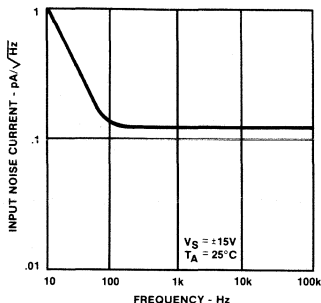
DUAL HIGH SLEW RATE OP AMPS

NE/SE538/538

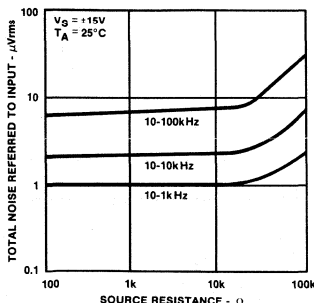
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

3

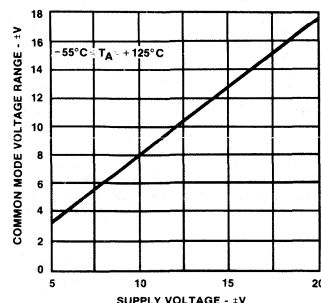
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



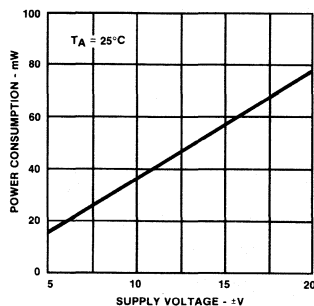
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



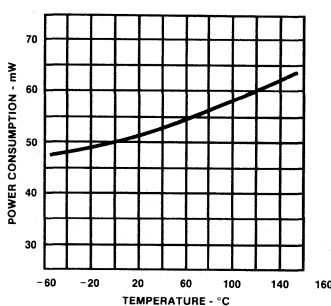
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



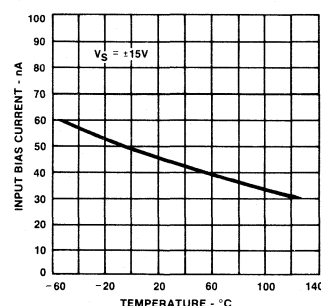
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



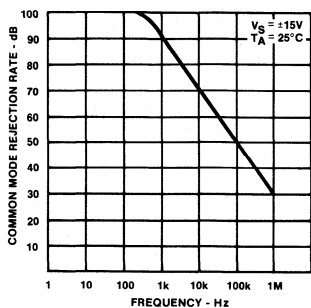
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



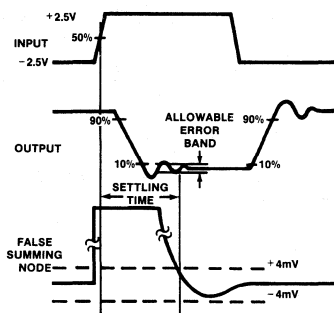
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



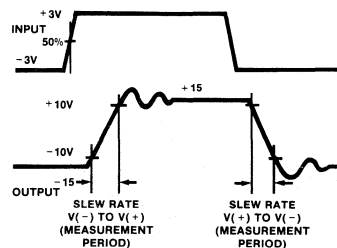
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SETTLING TIME MEASUREMENT WAVEFORMS



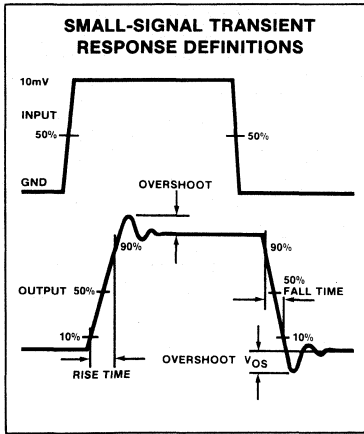
SLEW RATE MEASUREMENT V_{CC} = ±20V



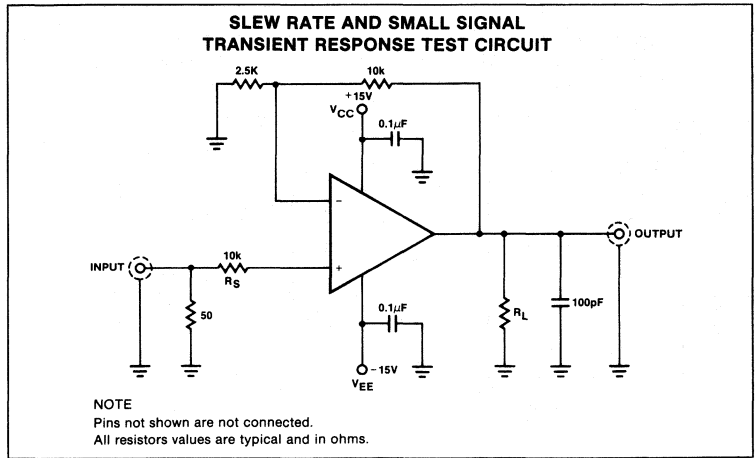
DUAL HIGH SLEW RATE OP AMPS

NE/SE538/5538

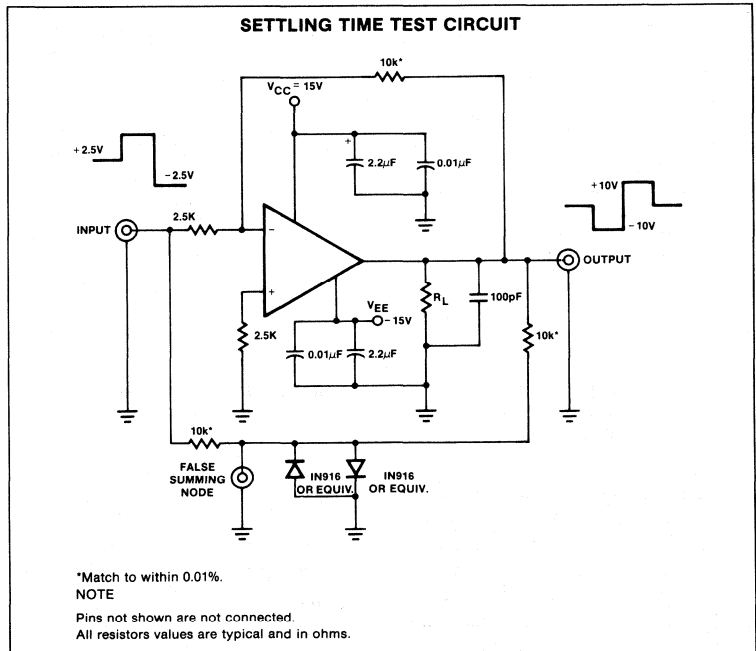
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



TEST LOAD CIRCUITS



TEST LOAD CIRCUITS (Cont'd)



DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER

NE/SE5512

DESCRIPTION

The 5512 series of high performance operational amplifier provides very good input characteristics. These amplifiers feature low input bias and voltage characteristics such as a 108 op amp with improved CMRR and a high differential input voltage limit achieved through the use of a bias cancellation and PNP input circuits with collector to emitter clamping. The output characteristics are like those of a 741 op amp with improved slew rate and drive capability yet have low supply quiescent current.

FEATURES

- Low input bias $< \pm 3nA$
- Low input offset current $< \pm 3nA$
- Low input offset voltage $< 1mV$
- Low V_{OS} temperature drift $4\mu V/^{\circ}C$
- Low input bias temperature drift $30pA/^{\circ}C$
- Low input voltage noise $25nV/\sqrt{Hz}$
- Low supply current $1.5mA/amp$
- High slew rate $1.0V/\mu s$
- High CMRR 100dB
- High input impedance $100M\Omega$
- High PSRR 110dB
- High differential input voltage limit
- No cross-over distortion
- Indefinite output short circuit protection
- Internally compensated for unity gain

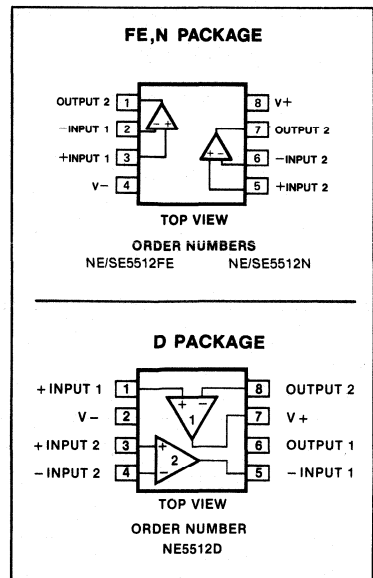
APPLICATIONS

- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Battery operation
- Instrumentation amplifiers

ABSOLUTE MAXIMUM RATINGS

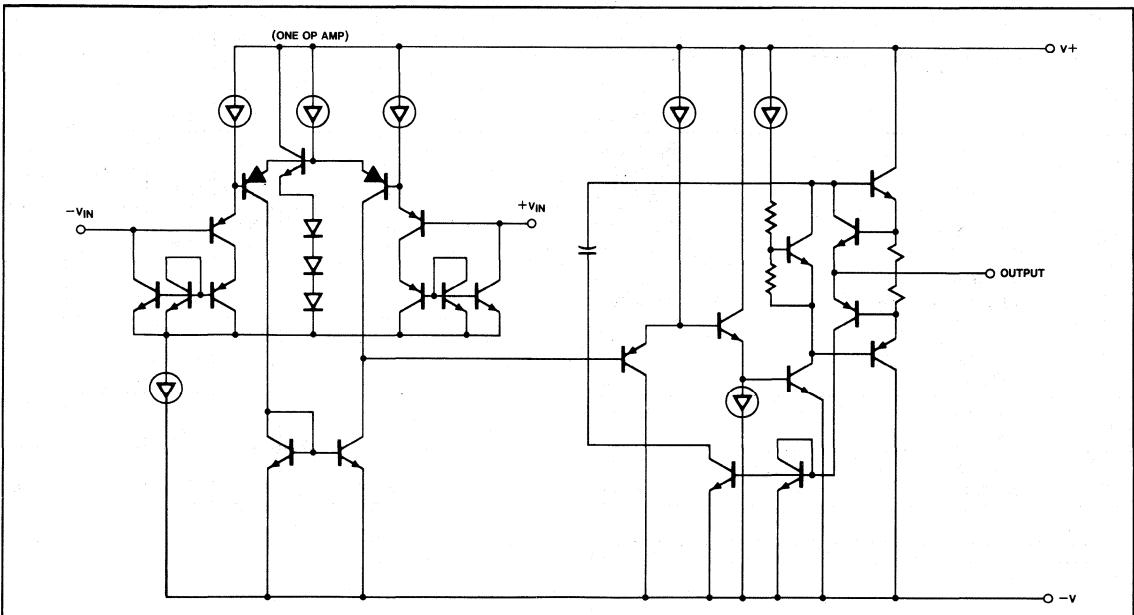
Parameter	Rating	Unit
V_{CC} Supply Voltage	± 16	V
V_D Power dissipation	500	mW
T_A Operating temperature range	NE5512	0 to 70 $^{\circ}C$
	SE5512	-55 to +125 $^{\circ}C$
T_{STG} Storage temperature range	-65 to +150	$^{\circ}C$
T_{SOLD} Lead temperature soldering	300	$^{\circ}C$

PIN CONFIGURATIONS



3

EQUIVALENT SCHEMATIC



DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER

NE/SE5512

ELECTRICAL PERFORMANCE CHARACTERISTICS $V_{CC} = \pm 15V$, F.R. = $-55^{\circ}C$ to $+125^{\circ}C$ (SE), $0^{\circ}C$ to $+70^{\circ}C$ (NE)

PARAMETER	TEST CONDITIONS	SE5512			NE5512			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage $R_S = 100\Omega$ $T_A = +25^{\circ}C$ $T_A = F.R.$		0.7 1	2 3		1 1.5	5 6	mV
I_{OS}	Input offset current $R_S = 100k\Omega$ $T_A = +25^{\circ}C$ $T_A = F.R.$		3 4	10 20		6 8	20 30	nA
I_B	Input bias current $R_S = 100k\Omega$ $T_A = +25^{\circ}C$ $T_A = F.R.$		3 4	10 20		6 8	20 30	nA
R_{IN}	Input resistance Differential $T_A = 25^{\circ}C$		100			100		$M\Omega$
V_{CM}	Input common mode range $T_A = 25^{\circ}C$ $T_A = F.R.$	± 13.5 ± 13	± 13.7 ± 13.2		± 13.5 ± 13	± 13.7 ± 13.2		V
CMRR	Input common-mode rejection ratio $V_{CC} = \pm 15V$ $V_{IN} = \pm 13.5V$ (RM) $T_A = 25^{\circ}C$ $V_{IN} = \pm 13V$ (F.R.) $T_A = F.R.$	70	100		70	100		dB
A_{VOL} GAIN	Large-signal voltage gain $R_L = 2k\Omega$ $T_A = 25^{\circ}C$ $V_O = \pm 10V$ $T_A = F.R.$	50 25	200		50 25	200		V/mV
S.R.	Slew rate $T_A = 25^{\circ}C$	0.6	1			1		V/ μs
GBW	Small-signal unity gain bandwidth $T_A = 25^{\circ}C$		3			3		MHz
θ_M	Phase margin $T_A = 25^{\circ}C$		45			45		Degree
V_{OUT}	Output voltage swing $R_L = 2k\Omega$ $T_A = 25^{\circ}C$ $T_A = F.R.$	± 13 ± 12.5	± 13.5 ± 13		± 13 ± 12.5	± 13.5 ± 13		V
V_{OUT}	Output voltage swing $R_L = 600\Omega^*$ $T_A = 25^{\circ}C$ $T_A = F.R.$	± 10 ± 8	± 11.5 ± 9		± 10 ± 8	± 11.5 ± 9		V
I_{CC}	Power supply current $R_L = \text{Open}$ $T_A = 25^{\circ}C$ $T_A = F.R.$		3.4 3.6	5 5.5		3.4 3.6	5 5.5	mA
PSRR	Power supply rejection ratio $T_A = 25^{\circ}C$ $T_A = F.R.$	80 80	110 100		80 80	110 100		dB
AA	Amplifier to amplifier coupling $f = 1kHz$ to $20kHz$ $T_A = 25^{\circ}C$		-120			-120		dB
HD	Total harmonic distortion $f = 10kHz$ $T_A = 25^{\circ}C$ $V_O = 7V_{RMS}$		0.01			0.01		%
V_{INN}	Input noise voltage $f = 1kHz$ $T_A = 25^{\circ}C$		30			30		nV/ \sqrt{Hz}
I_{INN}	Input noise current $f = 1kHz$ $T_A = 25^{\circ}C$.2			.2		pA/ \sqrt{Hz}

NOTE

* For operation at elevated temperature, N package must be derated based on a thermal resistance of $120^{\circ}/W$ junction to ambient. Thermal resistance of the FE package is $125^{\circ}/W$.

DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER

NE/SE5512

3

BRIDGE TRANSDUCER AMPLIFIER

In applications involving strain gauges, accelerometers and thermal sensors a bridge transducer is often used. Frequently the sensor elements are high resistance units requiring equally high bridge resistance for good sensitivity. This type of circuit then demands an amplifier with high input impedance, low bias current and low drift. The circuit shown represents a possible solution to these general requirements (Figure 1).

For $V_S = 10$ volts, the common mode voltage is approximately +5 volts, well within the common mode limits of the NE5512.

The sensitivity of the input stage is approximately

$$\frac{RF \cdot V_S}{2R}$$

to a change in transducer resistance ΔR . This gives a gain factor of ≈ 50 for $V_S = 10V$ and $R = 25k\Omega$. The second stage gain is $\times 100$ giving a total gain of ≈ 5000 .

Noise is minimized by shielding the transducer leads and taking special care to determine a good signal ground. Common mode noise rejection is particularly important making matched differential impedance critical. The NE5512 typically provides 100dB of common mode rejection and will considerably reduce this undesirable effect.

The following are sensitivity figures for the transducer circuits.

	$\frac{\Delta R}{R}$	$\frac{\Delta E_{out}}{E_{in}}$
leg 1	10%	-2.6V
	5%	-1.3V
leg 2	10%	+2.4
	5%	+1.2

Temperature compensation of the bridge element is accomplished by using low drift metal film resistors and also by providing a complimentary non-active sensor element to thermally track the offset in the active element.

High frequency roll-off provides attenuation of unwanted noise above the pass band of the transducer. The shunt capacitors across both stage feedback resistors are for this purpose.

CURRENT TO VOLTAGE CONVERTER

Taking advantage of the very low bias current and offset of the NE5512 is demonstrated in its adaptation to a current to voltage converter as shown below (Figure 2).

The lower limit of measuring accuracy is determined by I_B (inverting) which is typically 6nA. In order to attain a measurement accu-

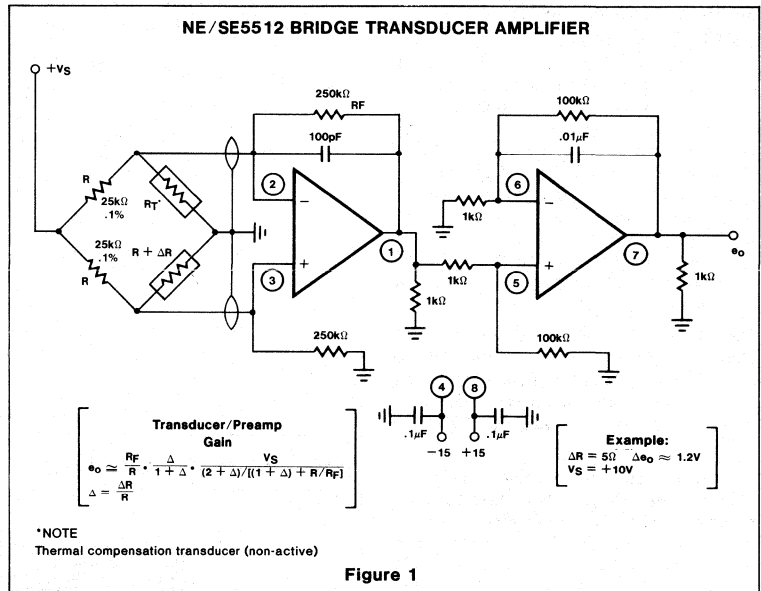


Figure 1

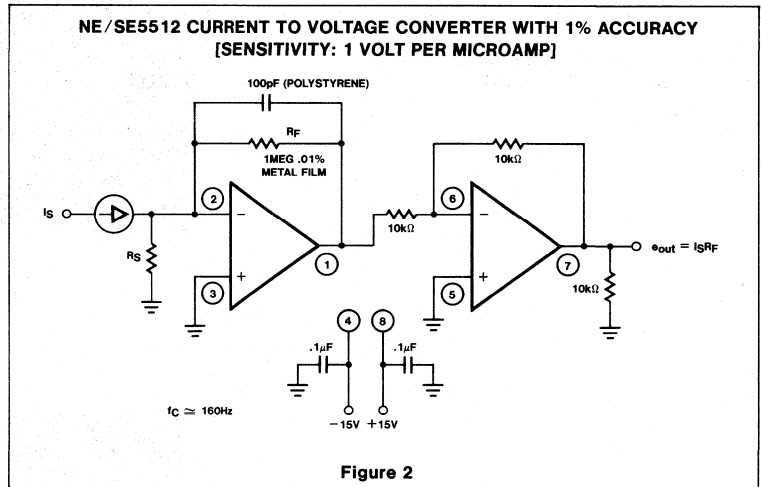


Figure 2

racy of 1% the following inequality must hold,

$$I_B \approx (.01) I_{Smin}$$

Where I_B = input bias current, I_{Smin} = minimum measured current. For $I_B = 6nA$ and $I_{Smin} = 1\mu A$,

$$6nA \approx (.01) 1\mu A = 10nA$$

and the inequality hold.

DC offset and current noise gain is determined by

$$\frac{R_F + R_S}{R_S}$$

which ≈ 1 for $R_S \gg R_F$.

The measured results for this circuit appear below ($V_{CC} = \pm 15$ volts).

INPUT CURRENT	OUTPUT VOLTAGE
1μA	1.008 Volts
5μA	5.00 Volts
10.00μA	10.00 Volts

DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER

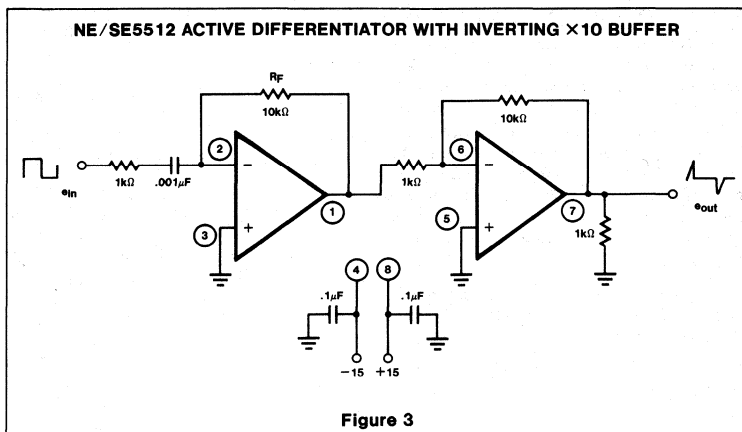
NE/SE5512

NE5512 OPERATIONAL DIFFERENTIATOR

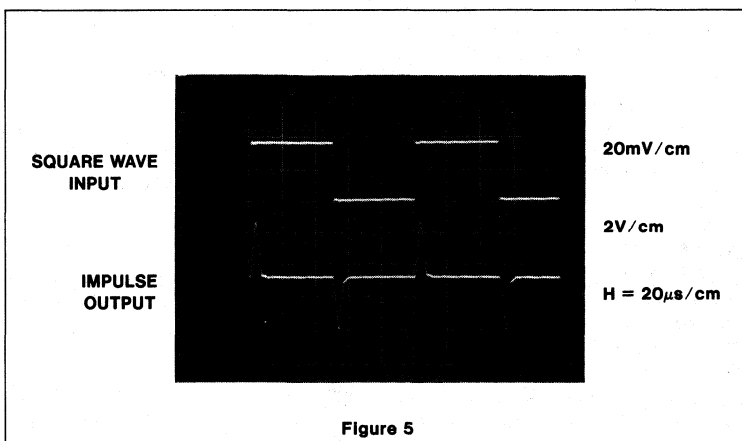
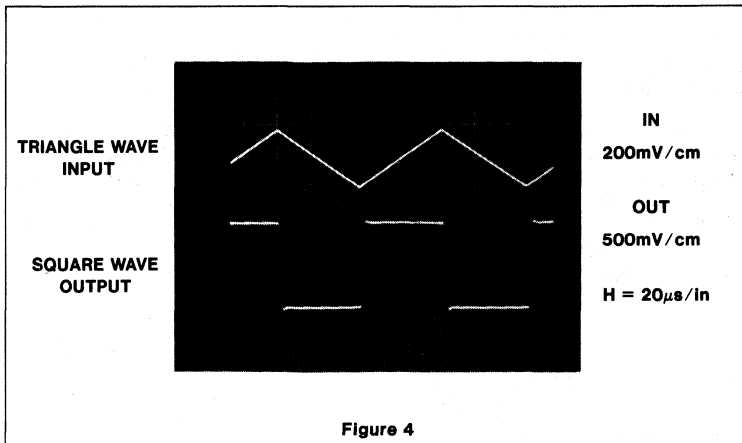
By utilizing the very high input impedance characteristic of the NE5512, an excellent active differentiator can be realized. Using the circuit shown (Figure 3), good results were obtained as shown by the wave forms in figures 4, 5 and 6. One of the primary problems with such circuits is the tendency toward instability and distortion either due to loading caused by input bias currents or amplifier non-linearity. In addition, gain increases with frequency requiring low input noise in the amplifier.

The relative stability is shown by the output signal wave forms mentioned above. Adding R_1 provides added compensation in the form of a zero near the amplifier unity gain frequency. Frequency range is 100Hz to 10kHz.

In order to obtain good differentiation, the network time constant, RC , must be small relative to the period of the highest frequency present at the input. Since the differentiator will attenuate the signal by a factor of ωRC which may be 100:1 in the operating region, the second amplifier stage is used to compensate for this loss. Various circuits are easily interfaced with the differentiator block due to the inherently low output impedance of the NE5512.



DIFFERENTIATOR WAVEFORMS



DUAL HIGH PERFORMANCE OPERATIONAL AMPLIFIER

NE/SE5512

THE OPERATIONAL INTEGRATOR

The operational complement of the active differentiator is the active integrator. The NE5512 is easily adapted to this function as shown in the circuit below (Figure 7). To obtain satisfactory integration the time constant must fulfill the following requirement:

$$RC \geq 15T$$

Where T is the period of the input wave form. For the ideal integrator

$$e_{out} = \frac{1}{RC} \int e_{in} dt$$

The factor 1/RC represents an attenuation of the input signal. The low signal level is increased by using the second half of the NE5512 as a gain stage following the operational integration. The wave forms in Figures 8 and 9 show the input-output relationship for both a sine wave and a square wave function. A good integrator must exhibit a phase shift of $\approx 89^\circ$ for sine wave input over the active frequency range. For a square wave the resultant output must be a linear ramp. The circuit shown fulfills this requirement (see Figure 7). No external compensation is required since the amplifier is unity gain stable.

DIFFERENTIATOR WAVEFORMS

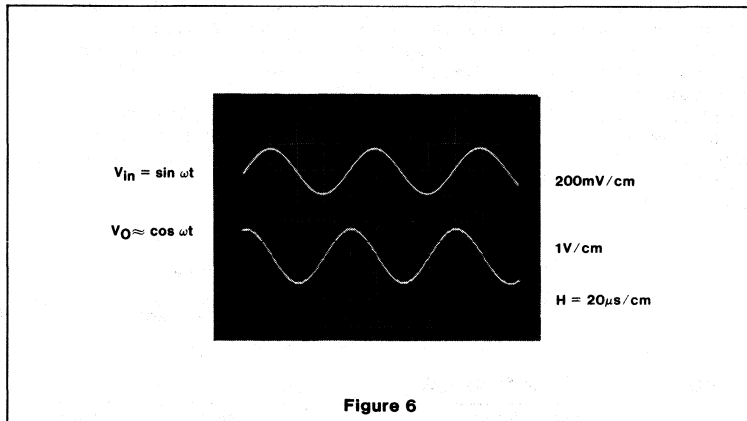


Figure 6

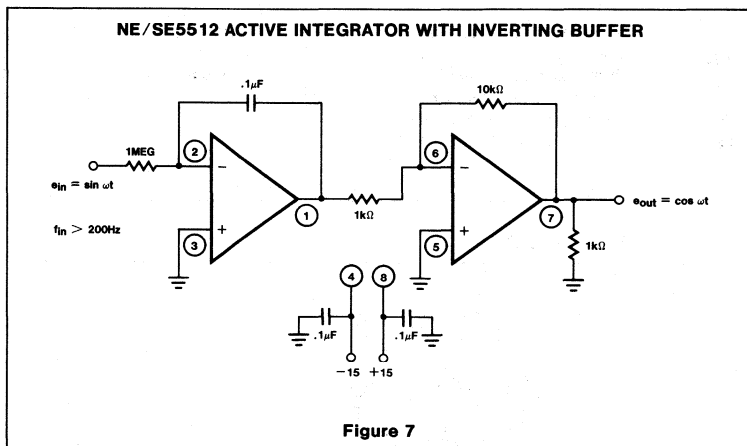


Figure 7

INTEGRATOR WAVEFORMS

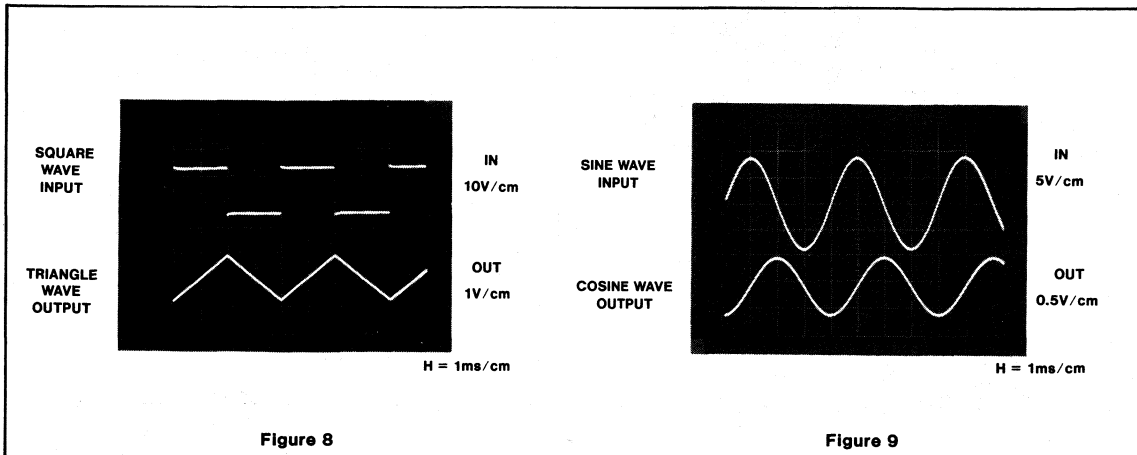


Figure 8

Figure 9

QUAD HIGH PERFORMANCE OP AMP

NE/SE5514

DESCRIPTION

The NE/SE5514 family of Quad Operational Amplifiers sets new standards in Bipolar Quad Amplifier Performance. The amplifiers feature low input bias current and low offset voltages. Pin-out is identical to LM324/LM348 which facilitates direct product substitution for improved system performance. Output characteristics are similar to a $\mu A741$ with improved slew and drive capability.

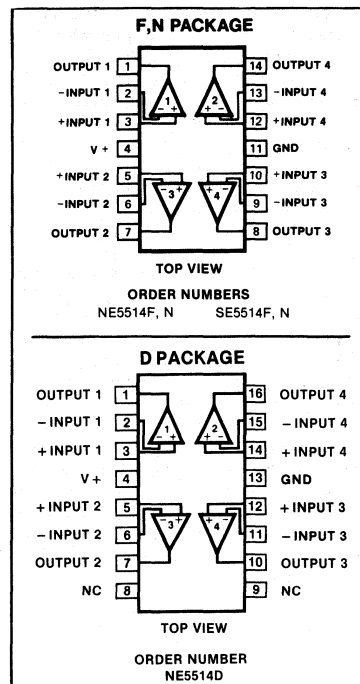
FEATURES

- Low input bias current: $< \pm 3nA$
- Low input offset current: $< \pm 3nA$
- Low input offset voltage: $< 1mV$
- Low supply current: $1.5mA/Amp$
- $1V/\mu sec$ slew rate
- High input impedance: $100M\Omega$
- High common mode impedance: $10G\Omega$
- Internal compensation for unity gain

APPLICATIONS

- AC amplifiers
- RC active filters
- Transducer amplifiers
- DC gain block
- Instrumentation amplifier

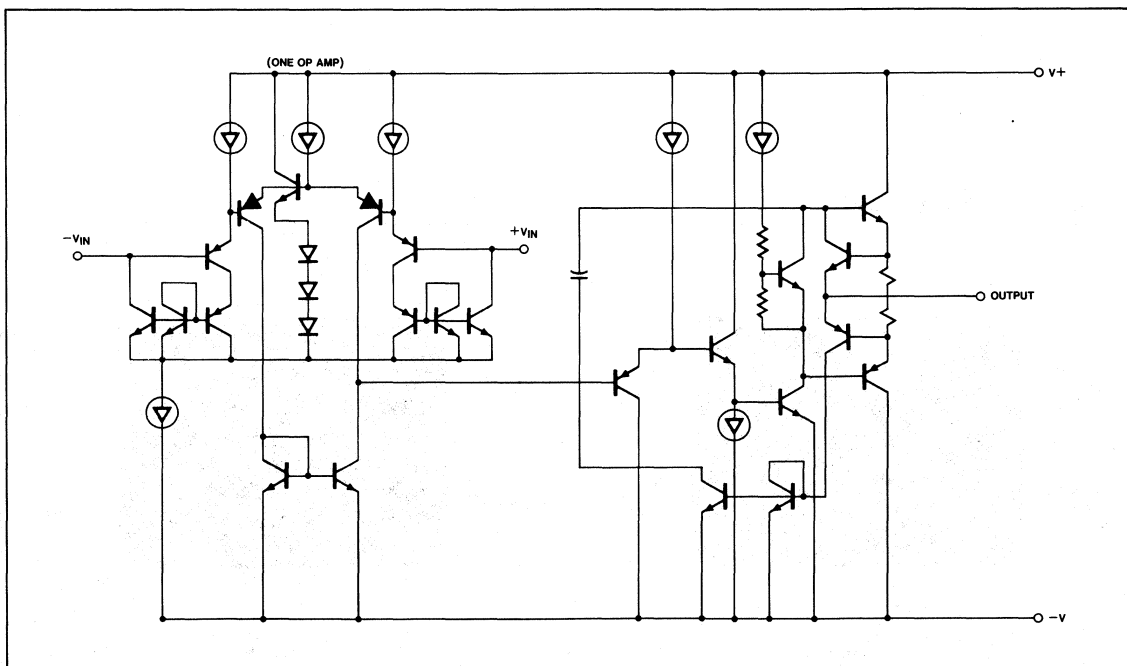
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
VCC	Supply voltage	± 16	V
V _{DIFF}	Differential input voltage	32	V
V _{IN}	Input voltage	0 to 32	V
	Output short to ground	Continuous	
T _S	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature	300	°C
T _A	Operating temperature range		
	NE5514	0 to 70	°C
	SE5514	-55 to +125	°C

EQUIVALENT SCHEMATIC



QUAD HIGH PERFORMANCE OP AMP

NE/SE5514

ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, F.R. = $-55^{\circ}C$ to $+125^{\circ}C$ (SE) $0^{\circ}C$ to $70^{\circ}C$ (NE)

PARAMETER	TEST CONDITIONS	SE5514			NE5514			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage $R_S = 100\Omega$, $T_A = +25^{\circ}C$, $T_A = F.R.$		0.7 1	2 3		1 1.5	5 6	mV
I_{OS}	Input offset current $R_S = 100k\Omega$, $T_A = +25^{\circ}C$, $T_A = F.R.$		3 4	10 20		6 8	20 30	nA
I_B	Input bias current $R_S = 100k\Omega$, $T_A = +25^{\circ}C$, $T_A = F.R.$		3 4	10 20		6 8	20 30	nA
R_{IN}	Input resistance differential $T_A = 25^{\circ}C$		100			100		M Ω
V_{CM}	Input common mode range $T_A = 25^{\circ}C$, $T_A = F.R.$	± 13.5 ± 13.5	± 13.7 ± 13.2		± 13.5 ± 13	± 13.7 ± 13.2		V
CMRR	Input common-mode rejection ratio $V_{CC} = \pm 15V$, $V_{IN} = \pm 13.5V$ (RM), $T_A = 25^{\circ}C$, $V_{IN} = \pm 13V$ (F.R.), $T_A = F.R.$	70	100		70	100		dB
AVOL GAIN	Large-signal voltage gain $R_L = 2k\Omega$, $T_A = 25^{\circ}C$ $V_C = \pm 10V$, $T_A = F.R.$	50 25	200		50 25			V/mV
S.R.	Slew rate $T_A = 25^{\circ}C$	0.6	1		0.6	1		V/ μs
GBW	Small-signal unity gain bandwidth $T_A = 25^{\circ}C$		3			3		MHz
θ_M	Phase margin $T_A = 25^{\circ}C$		45			45		Degr
V_{OUT}	Output voltage swing $R_L = 2k\Omega$, $T_A = 25^{\circ}C$ $T_A = F.R.$	± 13 ± 12.5	± 13.5 ± 13		± 13 ± 12.5	± 13.5 ± 13		V
V_{OUT}	Output voltage swing $R_L = 600\Omega^*$, $T_A = 25^{\circ}C$ $T_A = F.R.$	± 10 ± 8	± 11.5 ± 9		± 10 ± 8	± 11.5 ± 9		V
I_{CC}	Power supply current $R_L = \text{Open}$, $T_A = 25^{\circ}C$ $T_A = F.R.$		6 7	10 12		6 7	10 12	mA
PSRR	Power supply rejection ratio $T_A = 25^{\circ}C$, $T_A = F.R.$	80 80	110 100		80 80	110 100		dB
AA	Amplifier to amplifier coupling $f = 1kHz$ to $20kHz$, $T_A = 25^{\circ}C$		-120			-120		dB
HD	Total harmonic distortion $f = 10kHz$, $T_A = 25^{\circ}C$ $V_O = 7V_{RMS}$		0.01			0.01		%
V_{INN}	Input-noise voltage $f = 1kHz$, $T_A = 25^{\circ}C$		30			30		nV/ \sqrt{Hz}

NOTE

*For operation at elevated temperature, N package must be derated based on a thermal resistance of $95^{\circ}C/W$ junction to ambient.

QUAD HIGH PERFORMANCE OP AMP

NE/SE5514

FOUR QUADRANT PHOTO-CONDUCTIVE DETECTOR AMPLIFIER

When operating a photo diode in the photo-conductive mode (reverse biased) very small currents in the micro ampere range must be sensed in the photo active operating region. Dark currents in the nano amperes are common. Generally, for this reason, J-FET input preamps are used to prevent interaction and accuracy degradation due to input bias currents.

The 5514 has sufficiently low input bias current (6na) to allow its use under these circuit constraints as shown in a possible design used to sense four quadrant motion of a light source. By proper summing of the signals from the X and Y axes, four quadrant output may be fed to an X-Y plotter, oscilloscope or computer for simulation. (See figure 1).

The wide input common mode voltage range of the device allows a +10 volt supply to be used to drive the signal bridge giving high sensitivity and improved signal to noise. Obviously, input balancing is critical to achieving common mode signal rejection in addition to adequate shielding of the sensor leads. The sensor head itself must be shielded and the shield grounded to signal common to avoid unwanted noise pick up from power line and other local noise sources. Amplifier response may be shaped to aid in noise reduction by more complex filter configurations. If possible the 5514 should be located in close proximity to the sensor head.

System balance may be done under dark field conditions if adequate photo detector tracking results. However, for high accuracy systems a bipolar balance adjust added to the non-inverting output stage is more desirable. With this latter method the signal bridge is balanced for a null output under uniform light field conditions using the bridge balance pot as shown. D.C. offset is then adjusted using the balance pot on the output amplifier under dark field conditions.

MULTI-TONE BANDPASS FILTER FOR PLL TONE DECODER

In the design of a multiple tone signaling system, particularly where signals are transmitted over long lines, noise and adjacent channel interference may be a significant barrier to reliable communications.

By the use of narrow band active pre-filters to attain selectivity and gain, the effective

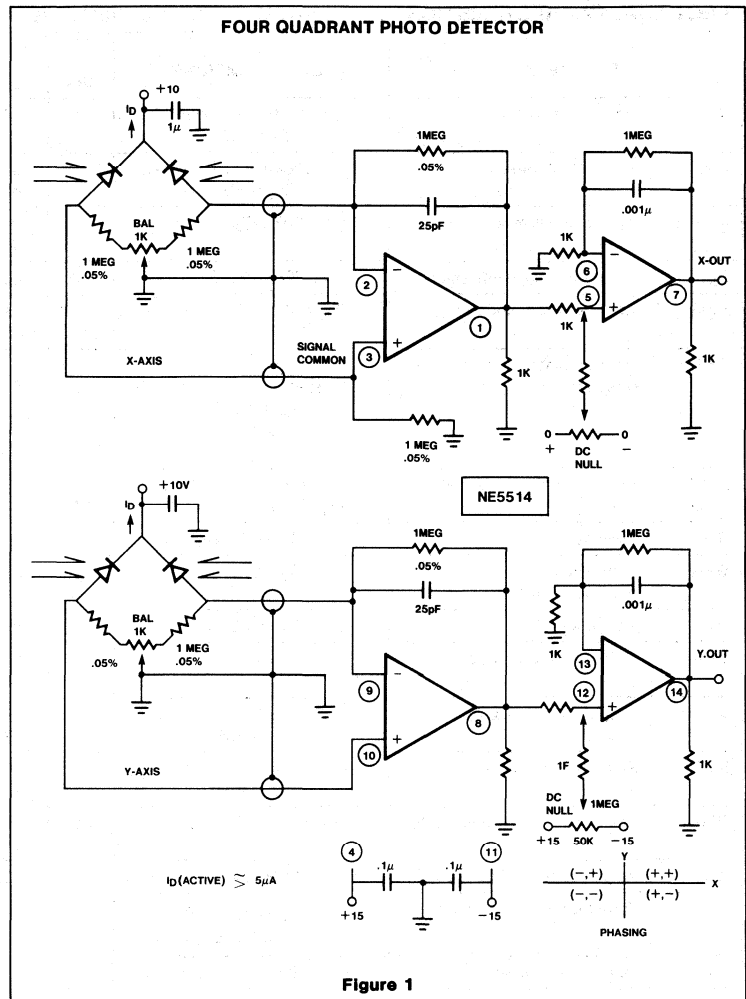


Figure 1

signal to noise ratio is greatly improved. The NE/SE5514 is easily adapted to such filter configurations due to its inherent stability. In addition its very high input impedance drastically reduces loading on the passive networks and allows for increased "Q" and large value resistors.

The circuit in Figure 2 demonstrates multiple feedback filters operating at four of the standard signaling frequencies. More channels may be added to increase the capacity of the system.

Test results obtained from this filter configuration were as follows:

Wide band signal to noise	63dB
Gain (Mid band)	30dB
Q (effective)	≈ 30
Output	OdBM (.775v _{rms})

Note that the amplifiers are operated from a single +12 volt supply and are biased to half V_{CC} by a simple resistive divider at point B which connects to all non-inverting inputs.

QUAD HIGH PERFORMANCE OP AMP

NE/SE5514

4-STATION 0-50° TEMPERATURE SENSOR

By using an NPN transistor as a temperature sensing element, the NE5514 forms the basis for a multi-station temperature sensor as shown in Figure 3. The principle used is fundamental to the current-voltage relationship of a forward biased junction. The current flow across the base-emitter junction is determined by absolute temperature in the following way:

$$I_E = -(I_C + I_B)$$

$$\text{and } I_E \propto I_S \exp(V_{BE}/V_T); V_T = \frac{kt}{q}$$

therefore, $V_{BE} \propto V_T \ln I_E/I_S$

Where I_E is the forward current and I_S is the saturation current inherent in the junction, I_E must be high enough such that the I_S variation with temperature is small relative to I_E ($I_E \gg I_S$). I_S is typically .05 pA, therefore, setting I_E to 1 or 2 μ A gives the desired condition.

Diode D_1 serves to substantially reduce error due to power supply variation by giving a fixed voltage reference. To calibrate the sensor adjust R_4 for "0" volts output from the NE5514 at 0°C. Adjust R_6 tracking resistor for a scale factor of 100 millivolts per °C output.

Only the transistor need be placed in the temperature controlled environment. Figure 4 shows the addition of an A/D converter and display to give a digital thermometer.

NE/SE5514
MFB BANDPASS FILTER
FOR
MULTI-CHANNEL TONE DECODER

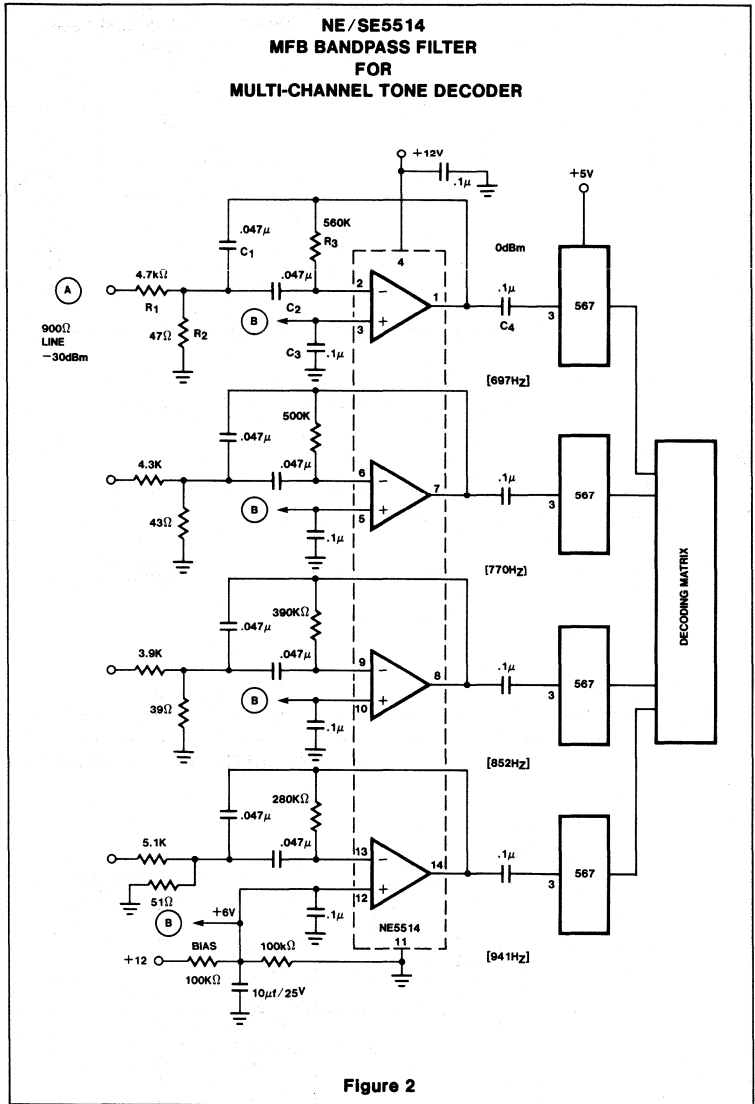


Figure 2

QUAD HIGH PERFORMANCE OP AMP

NE/SE5514

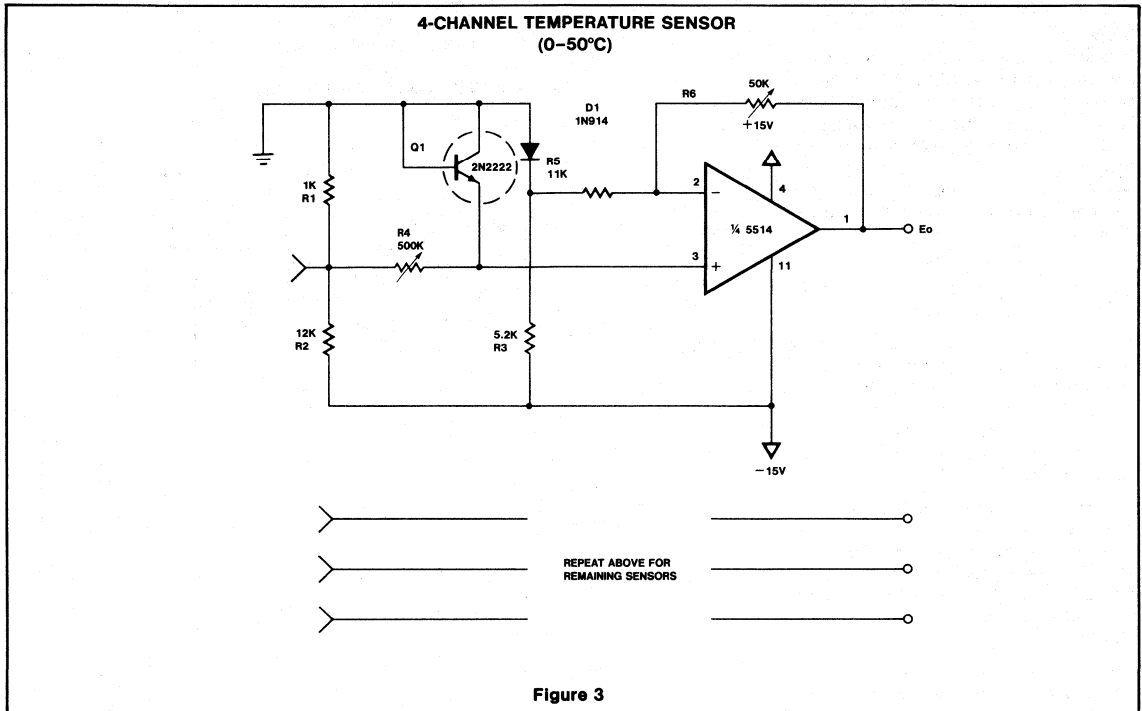


Figure 3

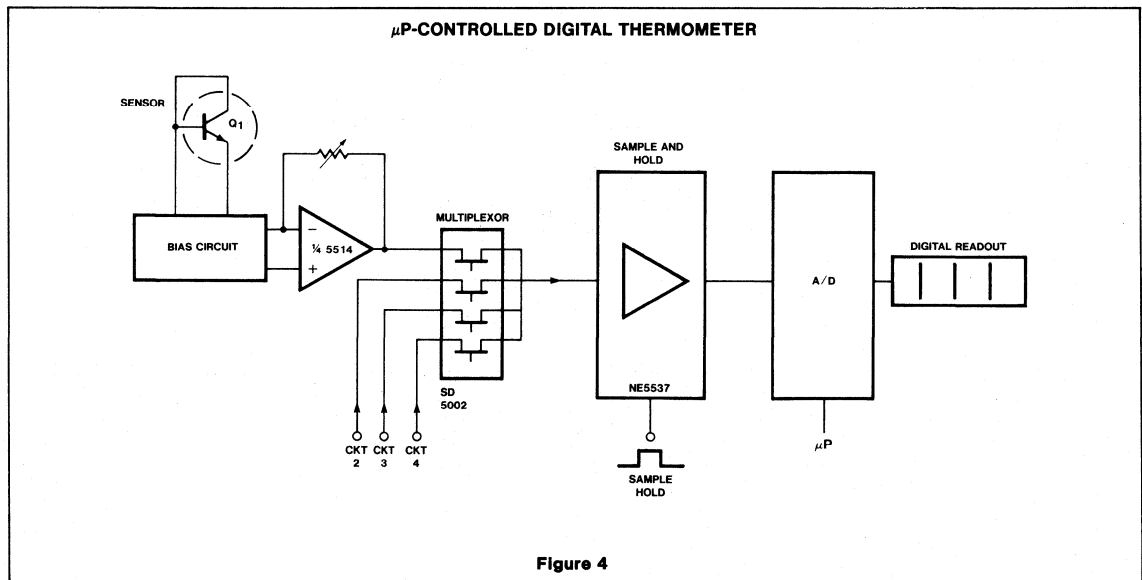


Figure 4

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

NE5517/5517A

DESCRIPTION

The NE5517 contains two current controlled transconductance amplifiers, each with a differential input and push-pull output. The NE5517 offers significant design and performance advantages over similar devices for all types of programmable gain applications. Constant impedance buffers are provided which effectively eliminate changes in output offset voltage as the amplifier bias current is varied. Circuit performance is enhanced through the use of linearizing diodes at the inputs which enable a 10 dB signal to noise improvement referenced to .5 percent THD. The NE5517 is suited for a wide variety of industrial and consumer applications and is recommended as the preferred circuit in the Dolby[®] HX (Headroom Extension) system.

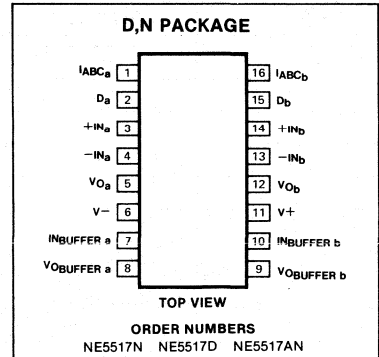
FEATURES

- Constant impedance buffers
- ΔV_{BE} of buffer is constant with amplifier I_{BIAS} change
- Pin compatible with LM13600
- Excellent matching between amplifiers
- Linearizing diodes
- High output signal-to-noise ratio

APPLICATIONS

- Multiplexers
- Timers
- Electronic music synthesizers
- Dolby[®] HX Systems
- Current-controlled amplifiers, filters
- Current-controlled oscillators, impedances

PIN CONFIGURATION



3

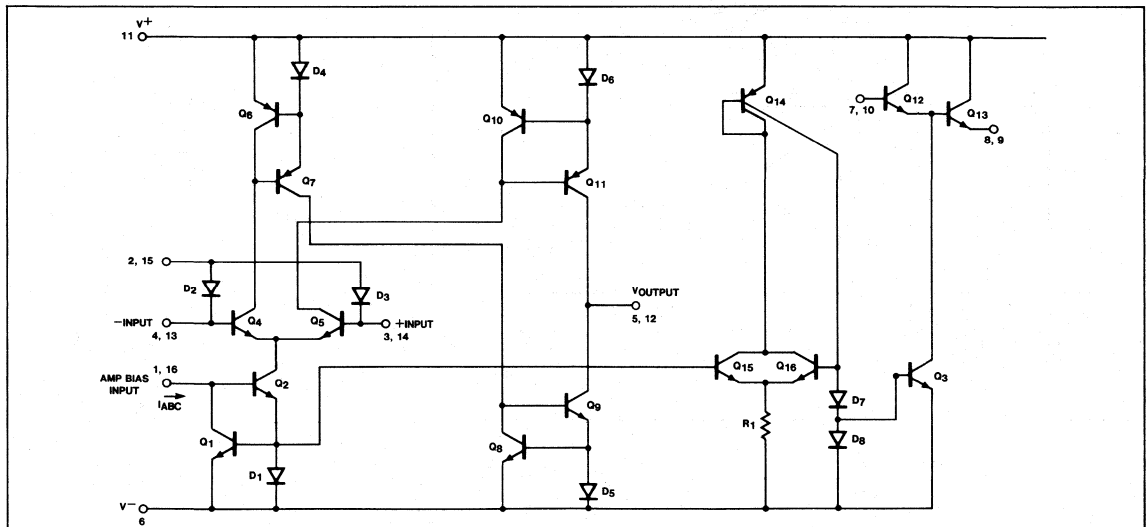
NOTE

[®]Dolby is a registered trademark of Dolby Laboratories Inc., San Francisco, Calif.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage ¹		
NE5517	36 V _{DC} or ± 18	V
NE5517A	44 V _{DC} or ± 22	V
Power Dissipation ² T _A = 25°C		
NE5517N, NE5517AN	570	mW
Differential Input Voltage	± 5	V
Diode Bias Current (I _D)	2	mA
Amplifier Bias Current (I _{ABC})	2	mA
Output Short Circuit Duration	Indefinite	
Buffer Output Current ³	20	mA
Operating Temperature Range		
NE5517N, NE5517AN	0°C to +70	°C
DC Input Voltage	+V _S to -V _S	
Storage Temperature Range	-65°C to +150	°C
Lead Temperature (Soldering, 10 Seconds)	300	°C

CIRCUIT SCHEMATIC



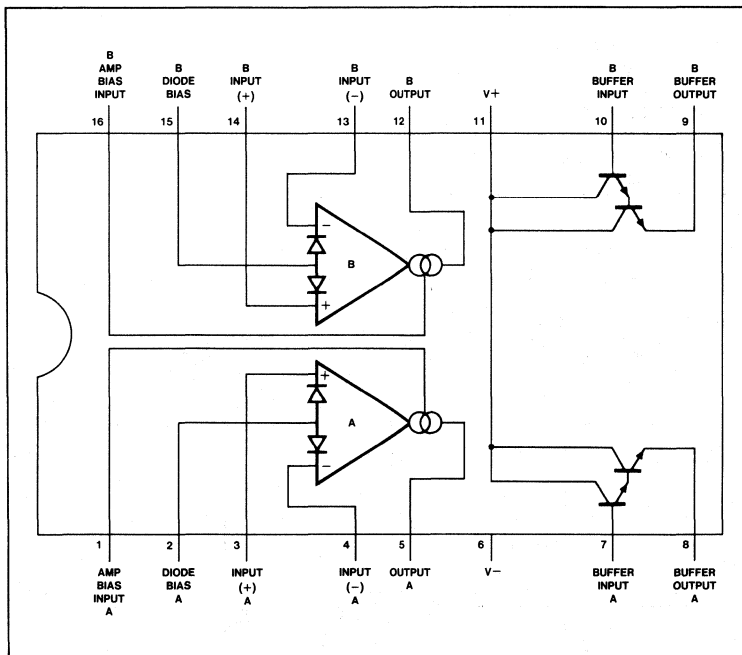
OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

NE5517/5517A

PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	I_{ABCa}	Amplifier bias input A
2	D_a	Diode bias A
3	$+IN_a$	Non-inverting input A
4	$-IN_a$	Inverting input A
5	V_{oa}	Output A
6	$V-$	negative supply
7	$IN_{Buffer} (a)$	Buffer input A
8	$V_{oBuffer} (a)$	Buffer output A
9	$V_{oBuffer} (b)$	Buffer output B
10	$IN_{Buffer} (b)$	Buffer input B
11	$V+$	Positive supply
12	V_{ob}	Output B
13	$-IN_b$	Inverting input B
14	$+IN_b$	Non-inverting input B
15	D_b	Diode bias B
16	I_{ABCb}	Amplifier bias input B

CONNECTION DIAGRAM



OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

NE5517/5517A

ELECTRICAL CHARACTERISTICS⁴

PARAMETER	TEST CONDITIONS	NE5517			NE5517A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage (V_{OS})	Over temperature range $I_{ABC} = 5\mu A$		0.4	5		0.4	2	mV
			0.3	5		0.3	2	mV
V_{OS} including diodes	Diode bias current (I_D) = $500\mu A$		0.5	5		0.5	2	mV
Input offset change	$5\mu A \leq I_{ABC} \leq 500\mu A$		0.1			0.1	3	mV
Input offset current			0.1	0.6		0.1	0.6	μA
Input bias current	Over temperature range		0.4	5		0.4	5	μA
			1	8		1	7	μA
Forward Transconductance (gm)	Over temperature range	6700	9600	13000	7700	9600	12000	μmho
		5400			4000			μmho
gm tracking			0.3			0.3		dB
Peak output current	$R_L = 0, I_{ABC} = 5\mu A$ $R_L = 0, I_{ABC} = 500\mu A$ $R_L = 0.$	350	5	650	3	5	7	μA
		300	500		350	500	650	μA
Peak output voltage Positive Negative	$R_L = \infty, 5\mu A \leq I_{ABC} \leq 500\mu A$	+12	+14.2		+12	+14.2		V
	$R_L = \infty, 5\mu A \leq I_{ABC} \leq 500\mu A$	-12	-14.4		-12	-14.4		V
Supply current	$I_{ABC} = 500\mu A$, both channels		2.6			2.6		mA
V_{OS} sensitivity Positive Negative	$\Delta V_{OS} / \Delta V+$ $\Delta V_{OS} / \Delta V-$		20	150		20	150	$\mu V / V$
			20	150		20	150	$\mu V / V$
CMRR		80	110		80	110		dB
Common mode range		± 12	± 13.5		± 12	± 13.5		V
Crosstalk	Referred to input ⁵ 20Hz < f < 20kHz		100			100		dB
Diff. input current	$I_{ABC} = 0$, input = $\pm 4V$		0.02	100		0.02	10	nA
Leakage current	$I_{ABC} = 0$ (Refer to test circuit)		0.2	100		0.2	5	nA
Input resistance		10	26		10	26		K Ω
Open loop bandwidth			2			2		MHz
Slew rate	Unity gain compensated		50			50		V / μSec
Buff. input current	5		0.4	5		0.4	5	μA
Peak buffer output voltage	5	10			10			V
ΔV_{BE} of buffer	6 Refer to Buffer V_{BE} test circuit		0.5	5		0.5	5	mV

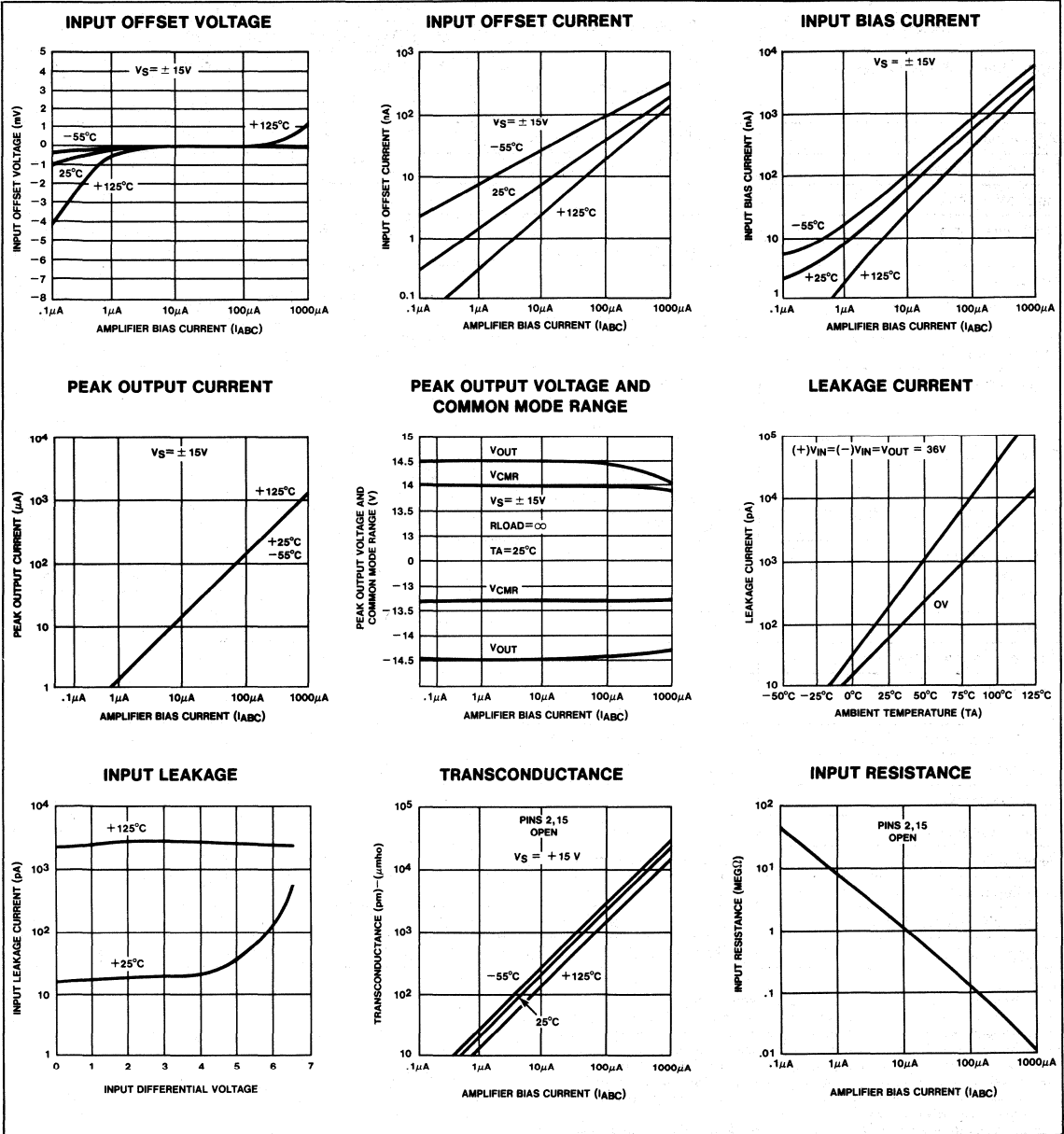
NOTES

- For selections to a supply voltage above $\pm 22V$, contact factory.
- For operating at high temperatures, the device must be derated based on a $150^\circ C$ maximum junction temperature and a thermal resistance of $175^\circ C/W$ which applies for the device soldered in a printed circuit board, operating in still air.
- Buffer output current should be limited so as to not exceed package dissipation.
- These specifications apply for $V_S = \pm 15V$, $T_A = 25^\circ C$, amplifier bias current (I_{ABC}) = $500\mu A$, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.
- These specifications apply for $V_S = \pm 15V$, $I_{ABC} = 500\mu A$, $R_{OUT} = 5k\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.
- $V_S = \pm 15$, $R_{OUT} = 5\Omega$ connected from Buffer output to $-V_S$ and $5\mu A \leq I_{ABC} \leq 500\mu A$.

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

NE5517/5517A

TYPICAL PERFORMANCE CHARACTERISTICS



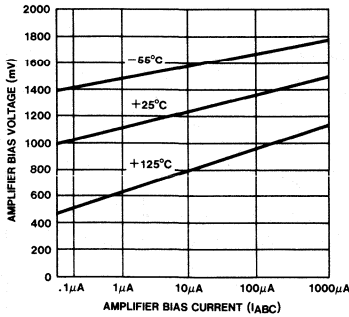
OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

NE5517/5517A

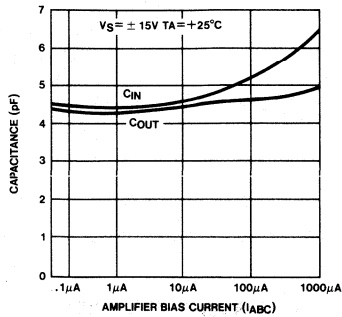
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

3

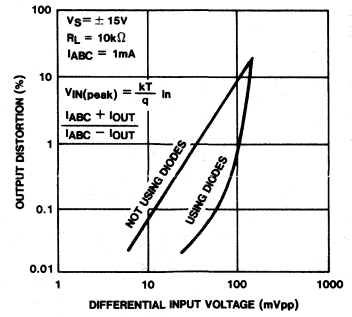
AMPLIFIER BIAS VOLTAGE vs AMPLIFIER BIAS CURRENT



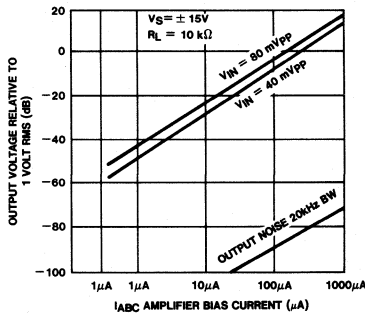
INPUT AND OUTPUT CAPACITANCE



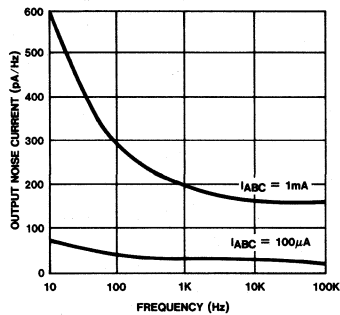
DISTORTION vs DIFFERENTIAL INPUT VOLTAGE



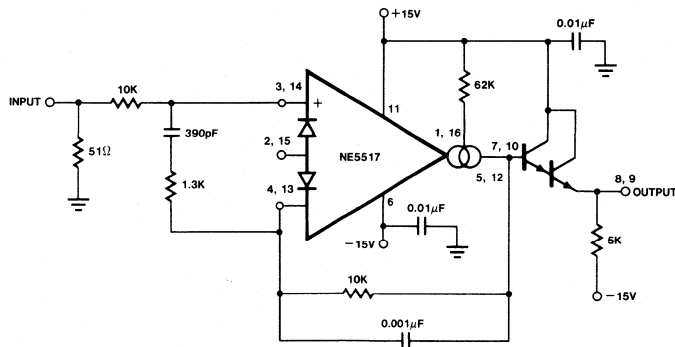
VOLTAGE vs AMPLIFIER BIAS CURRENT



OUTPUT NOISE vs FREQUENCY



UNITY GAIN FOLLOWER

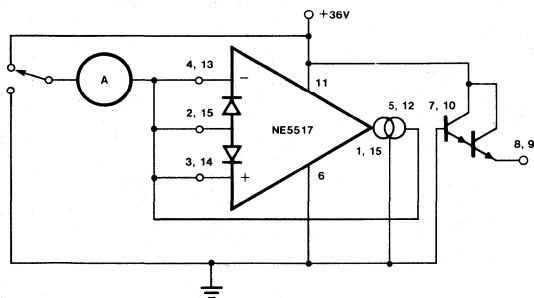


OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

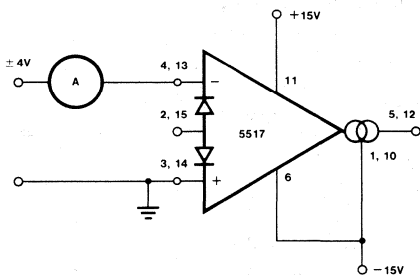
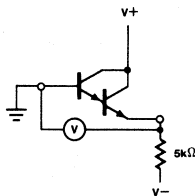
NE5517/5517A

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

LEAKAGE CURRENT TEST CIRCUIT



DIFFERENTIAL INPUT CURRENT TEST CIRCUIT

BUFFER V_{BE} TEST CIRCUIT

INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP NE/SE5532/5532A

DESCRIPTION

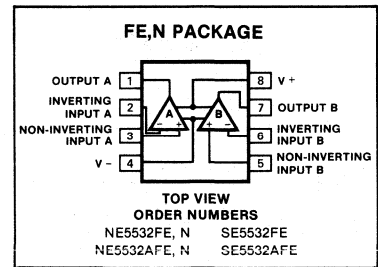
The 5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the 5532A version be used which has guaranteed noise specifications.

FEATURES

- Small-signal bandwidth: 10MHz
- Output drive capability: 600Ω, 10V (rms)
- Input noise voltage: $5nV/\sqrt{Hz}$
- DC voltage gain: 50000
- AC voltage gain: 2200 at 10kHz
- Power bandwidth: 140kHz
- Slew-rate: $9V/\mu s$
- Large supply voltage range: ± 3 to $\pm 20V$

PIN CONFIGURATION



3

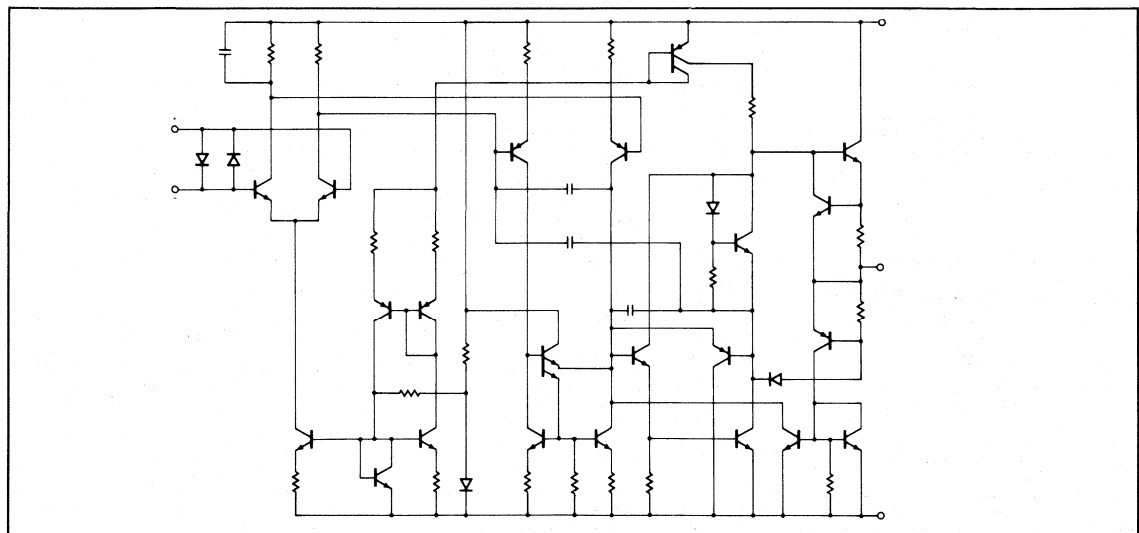
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _S Supply voltage	± 22	V
V _{IN} Input voltage	$\pm V$ supply	V
V _{DIFF} Differential input voltage ¹	$\pm .5$	V
T _A Operating temperature range	0 to 70	°C
T _{STG} Storage temperature	-65 to +150	°C
T _J Junction temperature	150	°C
P _D Power dissipation		
5532FE	1000	mW
Lead temperature (soldering, 10 sec)	300	°C

NOTES:

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to $\pm 10mA$.
2. Thermal resistance of the FE package is $125^{\circ}C/W$.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP NE/SE5532/5532A

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.^{1, 2}

PARAMETER	TEST CONDITIONS	SE5532/5532A			NE5532/5532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	Over temperature		.5	2 3		.5	4 5	mV mV
I_{OS} Offset current	Over temperature			100 200		10	150 200	nA nA
I_B Input current	Over temperature		200	400 700		200	800 1000	nA nA
I_{CC} Supply current	Over temperature			13		8	16	mA mA
V_{CM} Common mode input range		± 12	± 13		± 12	± 13		V
CMRR Common mode rejection ratio		80	100		70	100		dB
PSRR Power supply rejection ratio			10	50		10	100	$\mu\text{V}/\text{V}$
A_{VOL} Large signal voltage gain	$R_L \geq 2\text{k}\Omega$ $V_O = \pm 10\text{V}$ Over temperature $R_L \geq 600\Omega$, $V_O = \pm 10\text{V}$ Over temperature	50 25 40 20			25 15 15 10	100 50		V/mV V/mV V/mV V/mV
V_{OUT} Output swing	$R_L \geq 600\Omega$ $R_L \geq 600\Omega$, $V_S = \pm 18\text{V}$ $R_L \geq 2\text{k}\Omega$	± 12	± 13		± 12 ± 15	± 13 ± 16		V V V
R_{IN} Input resistance		30	300		30	300		k Ω
I_{SC} Output short circuit current			38			38		mA

NOTES

- For NE5532, NE5532A, $T_{Min} = 0^\circ\text{C}$, $T_{Max} = 70^\circ\text{C}$.
- For SE5532/5532A, $T_{Min} = -55^\circ\text{C}$, $T_{Max} = +125^\circ\text{C}$.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE/SE5532/5532A			UNIT
		Min	Typ	Max	
R_{OUT} Output resistance	$A_V = 30\text{dB}$ Closed loop $f = 10\text{kHz}$, $R_L = 600\Omega$		0.3		Ω
Overshoot	Voltage follower $V_{IN} = 100\text{mV}$ p-p $C_L = 100\text{pF}$ $R_L = 600\Omega$		10		%
Gain	$f = 10\text{kHz}$		2.2		V/mV
Gain bandwidth product	$C_L = 100\text{pF}$ $R_L = 600\Omega$		10		MHz
Slew rate			9		V/ μs
Power bandwidth	$V_{OUT} = \pm 10\text{V}$ $V_{OUT} = \pm 14\text{V}$, $R_L = 600\Omega$, $V_{CC} = \pm 18\text{V}$		140 100		kHz kHz

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE/SE5532			NE/SE5532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	$f_o = 30\text{Hz}$ $f_o = 1\text{kHz}$		8 5			8 5	12 6	nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
Input noise current	$f_o = 30\text{Hz}$ $f_o = 1\text{kHz}$		2.7 0.7			2.7 0.7		pA/ $\sqrt{\text{Hz}}$ pA/ $\sqrt{\text{Hz}}$
Channel separation	$f = 1\text{kHz}$, $R_S = 5\text{k}\Omega$		110			110		dB

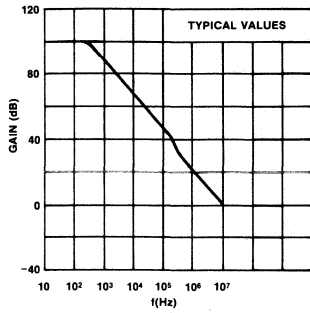
INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP

NE/SE5532/5532A

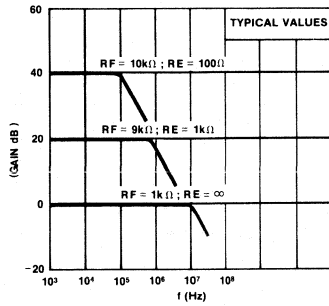
TYPICAL PERFORMANCE CHARACTERISTICS

3

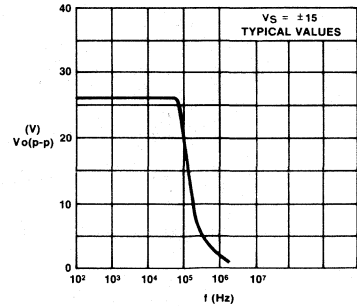
OPEN LOOP FREQUENCY RESPONSE



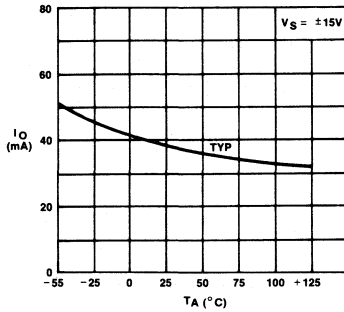
CLOSED LOOP FREQUENCY RESPONSE



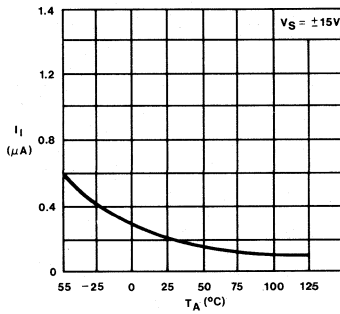
LARGE-SIGNAL FREQUENCY RESPONSE



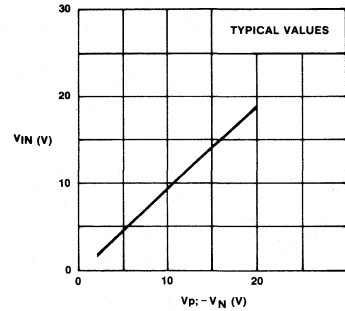
OUTPUT SHORT-CIRCUIT CURRENT



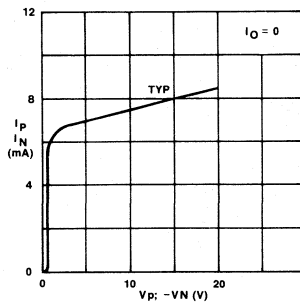
INPUT BIAS CURRENT



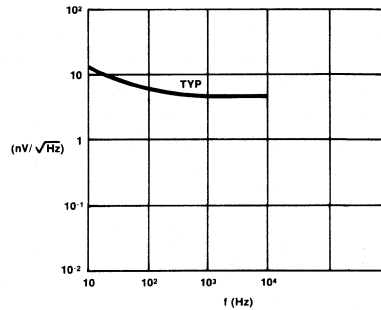
INPUT COMMON MODE VOLTAGE RANGE

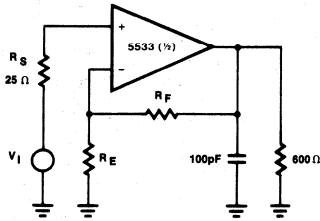
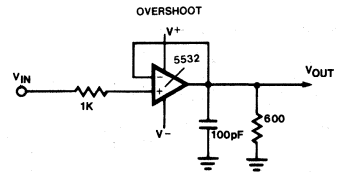


SUPPLY CURRENT



INPUT NOISE VOLTAGE DENSITY



INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP NE/SE5532/5532A**TEST CIRCUITS****CLOSED LOOP FREQUENCY RESPONSE****VOLTAGE FOLLOWER**

INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP NE/SE5532/5532A

APPLICATIONS

The Signetics 5532 High Performance Op Amp is an ideal amplifier for use in high quality and professional audio equipment which requires low noise and low distortion.

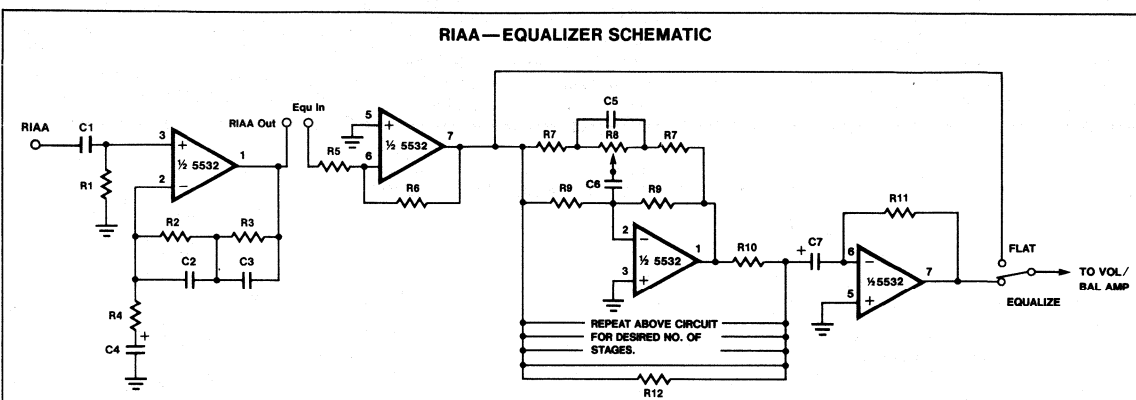
The circuit included in this application note has been assembled on a P.C. board, and tested with actual audio input devices

(Tuner and Turntable). It consists of an RIAA pre-amp, input buffer, 5-band equalizer, and mixer. Although the circuit design is not new, its performance using the 5532 has been improved.

The RIAA pre-amp section is a standard compensation configuration with low frequency boost provided by the Magnetic car-

tridge and the RC network in the op amp feedback loop. Cartridge loading is accomplished via R1. 47k was chosen as a typical value, and may differ from cartridge to cartridge.

The Equalizer section consists of an input buffer, 5 active variable band pass/notch (depending on R9's setting) filters, and an



COMPONENT VALUE TABLES

R8 = 25k R7 = 2.4k R9 = 240k			R8 = 50k R7 = 5.1k R9 = 510k			R8 = 100k R7 = 10k R9 = 1meg		
fo	C5	C6	fo	C5	C6	fo	C5	C6
23 Hz	1μF	.1μF	25 Hz	.47μF	.047μF	12 Hz	.47μF	.047μF
50 Hz	.47μF	.047μF	36 Hz	.33μF	.033μF	18 Hz	.33μF	.033μF
72 Hz	.33μF	.033μF	54 Hz	.22μF	.022μF	27 Hz	.22μF	.022μF
108 Hz	.22μF	.022μF	79 Hz	.15μF	.015μF	39 Hz	.15μF	.015μF
158 Hz	.15μF	.015μF	119 Hz	.1μF	.01μF	59 Hz	.1μF	.01μF
238 Hz	.1μF	.01μF	145 Hz	.082μF	.0082μF	72 Hz	.082μF	.0082μF
290 Hz	.082μF	.0082μF	175 Hz	.068μF	.0068μF	87 Hz	.068μF	.0068μF
350 Hz	.068μF	.0068μF	212 Hz	.056μF	.0056μF	106 Hz	.056μF	.0056μF
425 Hz	.056μF	.0056μF	253 Hz	.047μF	.0047μF	126 Hz	.047μF	.0047μF
506 Hz	.047μF	.0047μF	360 Hz	.033μF	.0033μF	180 Hz	.033μF	.0033μF
721 Hz	.033μF	.0033μF	541 Hz	.022μF	.0022μF	270 Hz	.022μF	.0022μF
1082 Hz	.022μF	.0022μF	794 Hz	.015μF	.0015μF	397 Hz	.015μF	.0015μF
1588 Hz	.015μF	.0015μF	1191 Hz	.01μF	.001μF	595 Hz	.01μF	.001μF
2382 Hz	.01μF	.001μF	1452 Hz	.0082μF	820pF	726 Hz	.0082μF	820pF
2904 Hz	.0082μF	820pF	1751 Hz	.0068μF	680pF	875 Hz	.0068μF	680pF
3502 Hz	.0068μF	680pF	2126 Hz	.0056μF	560pF	1063 Hz	.0056μF	560pF
4253 Hz	.0056μF	560pF	2534 Hz	.0047μF	470pF	1267 Hz	.0047μF	470pF
5068 Hz	.0047μF	470pF	3609 Hz	.0033μF	330pF	1804 Hz	.0033μF	330pF
7218 Hz	.0033μF	330pF	5413 Hz	.0022μF	220pF	2706 Hz	.0022μF	220pF
10827 Hz	.0022μF	220pF	7940 Hz	.0015μF	150pF	3970 Hz	.0015μF	150pF
15880 Hz	.0015μF	150pF	11910 Hz	.001μF	100pF	5955 Hz	.001μF	100pF
23820 Hz	.001μF	100pF	14524 Hz	820pF	82pF	7262 Hz	820pF	82pF
			17514 Hz	680pF	68pF	8757 Hz	680pF	68pF
			21267 Hz	560pF	56pF	10633 Hz	560pF	56pF
						12670 Hz	470pF	47pF
						18045 Hz	330pF	33pF

COMPONENT VALUES

R1	1meg	C1	22μF
R2	100k	C2	750pF
R3	1meg	C3	.0033μF
R4	1.1k	C4	33μF
R5	100k	C5	SEE TABLE
R6	100k	C6	SEE TABLE
R7	SEE TABLE	C7	2.2μF
R8	(pot) SEE TABLE		
R9	SEE TABLE		
R10	100k		
R11	100k		
R12	20k (5 STAGES)		

Figure 1

INTERNALLY COMPENSATED DUAL LOW NOISE OP AMP NE/SE5532/5532A

output summing amplifier. The input buffer is a standard unity gain design providing impedance matching between the pre amplifiers and the equalizer section. Because the 5532 is internally compensated, no external compensation is required. The 5-band active filter section is actually 5 individual active filters with the same feedback design for all 5. The main difference in all five stages is the values of C5 and C6 which are responsible for setting the center frequency of each stage. Linear pots are recommended for R9. To simplify use of this circuit, a component value table is provided, which lists center frequencies and their associated capacitor values. Notice that C5

equals (10) C6, and that the Value of R8 and R10 are related to R9 by a factor of 10 as well. The values listed in the table are common and easily found standard values.

The final stage is the summing amplifier/buffer stage, to sum the individual filters (Figure 2). Note the original signal is subtracted from the sum by a factor dependant on the number of filter stages. This subtraction is necessary to maintain a unity gain configuration at the output with all pots set to the flat position. If R13 were omitted the output with 1 volt at each stage would equal 5 volts (in this case) instead of the desired 1 volt. Full boost and cut using the table val-

ues is about $\pm 15\text{dB}$. Although 5 bands were chosen for this application, the user may have as many bands as are required. Please note that the subtracting resistor R13, must be adjusted to meet the unity requirement using $R13 = \frac{100K}{\# \text{ of stages}}$ i.e. 5 stages = 20k.

The remainder of the circuit employs the Philips TCA 730H volume, balance, and loudness-control circuit and the Signetics NE540 power driver circuit, which as shown will net about 35 watts per channel RMS. The NE540 can be found in the Signetics Analog Data Manual, and Applications Manual. Information on the TCA730A may be obtained from Signetics Analog Division.

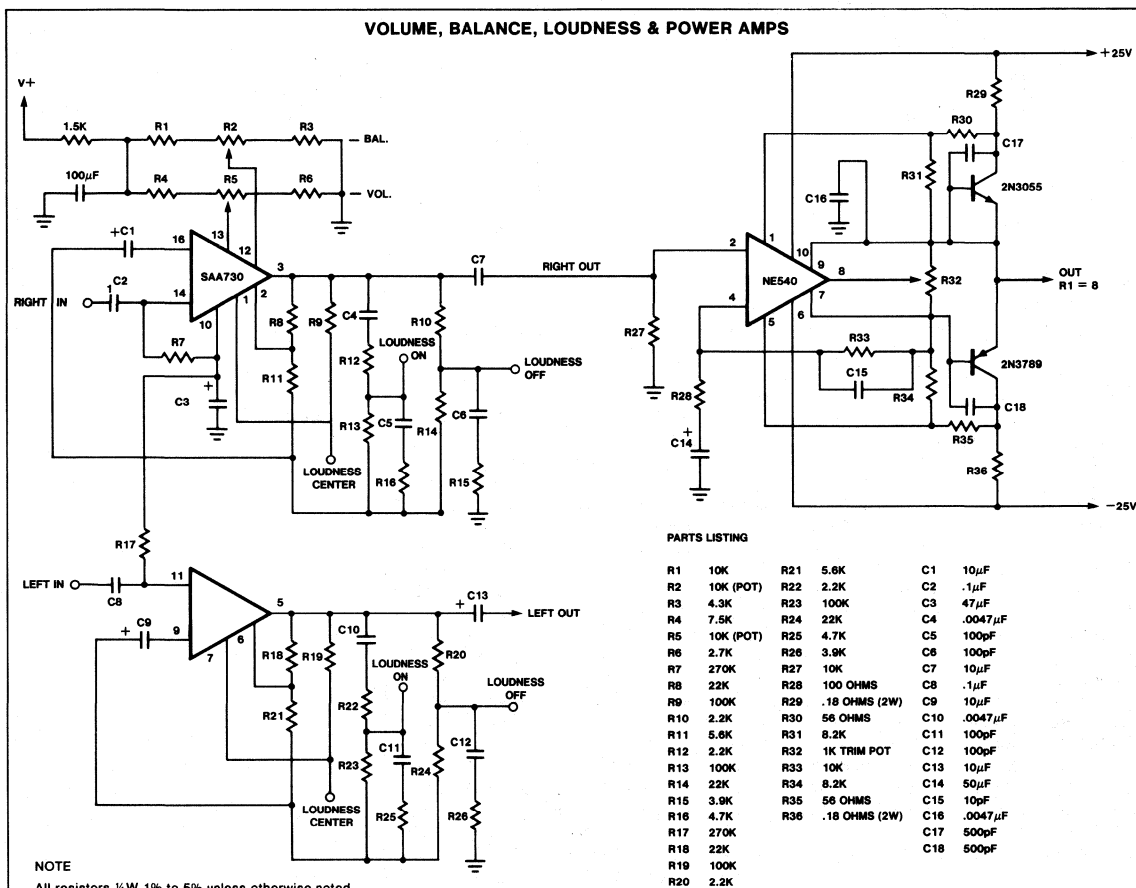


Figure 2

SINGLE AND DUAL LOW NOISE OP AMP NE5533/5533A / NE/SE5534/5534A

DESCRIPTION

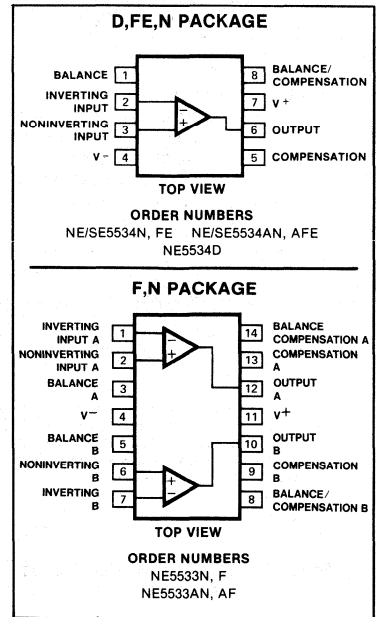
The 5533/5534 are dual and single high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

FEATURES

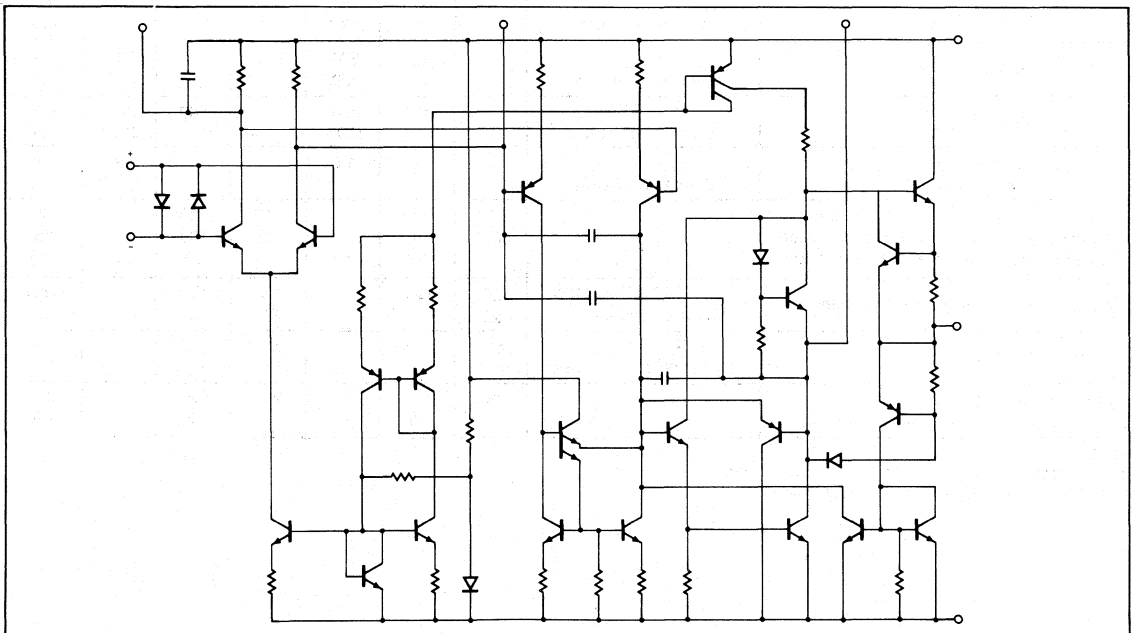
- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms) at $V_s = \pm 18V$**
- **Input noise voltage: $4nV/\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwidth: 200kHz**
- **Slew-rate: $13V/\mu s$**
- **Large supply voltage range: ± 3 to $\pm 20V$**

PIN CONFIGURATIONS



3

EQUIVALENT SCHEMATIC



SINGLE AND DUAL LOW NOISE OP AMP NE5533/5533A / NE/SE5534/5534A

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _S Supply voltage	±22	V
V _{IN} Input voltage	±V supply	V
V _{DIFF} Differential input voltage ¹	±5	V
T _A Operating temperature range		
SE5534/5534A	-55 to +125	°C
NE5533/5533A/5534/5534A	0 to +70	°C
T _{STG} Storage temperature	-65 to +150	°C
T _J Junction temperature	150	°C
P _D Power dissipation at 25°C ²		
5533N, 5534N, 5534FE	800	mW
5533F	1000	mW
Output short circuit duration ³	indefinite	
Lead temperature (soldering 10 sec)	300	°C

NOTES

- Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
- For operation at elevated temperature, derate packages based on the following junction-to-ambient thermal resistances:
 - 8-pin ceramic (FE) 140°C/W
 - 14-pin ceramic (F) 110°C/W
 - 8-pin plastic (N) 162°C/W
 - 14-pin plastic (N) 150°C/W
- Output may be shorted to ground at V_S = ±15V, T_A = 25°C. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_S = ±15V unless otherwise specified.^{1,2}

PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Offset voltage	Over temperature		.5	2 3		.5	4 5	mV mV
I _{OS} Offset current	Over temperature		10	200 500		20	300 400	nA nA
I _B Input current	Over temperature		400	800 1500		500	1500 2000	nA nA
I _{CC} Supply current Per op amp	Over temperature		4	6.5 9		4	8	mA mA
V _{CM} Common mode input range		±12	±13		±12	±13		V
CMRR Common mode rejection ratio		80	100		70	100		dB
PSRR Power supply rejection ratio			10	50		10	100	μV/V
A _{VOL} Large signal voltage gain	R _L ≥ 600Ω, V _O = ±10V Over temperature	50 25	100		25 15	100		V/mV V/mV
V _{OUT} Output swing	R _L ≥ 600Ω R _L ≥ 600Ω V _S = ±18V	±12 ±15	±13 ±16		±12 ±15	±13 ±16		V V
R _{IN} Input resistance		50	100		30	100		kΩ
I _{SC} Output short circuit current			38			38		mA

NOTES

- For NE5533/5533A/5534/5534A, T_{MIN} = 0°C, T_{MAX} = 70°C
- For SE5534/5534A, T_{MIN} = -55°C, T_{MAX} = +125°C

SINGLE AND DUAL LOW NOISE OP AMP NE5533/5533A / NE/SE5534/5534A

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
R_{OUT} Output resistance	$A_V = 30\text{dB}$ closed loop $f = 10\text{kHz}$, $R_L = 600\Omega$, $C_C = 22\text{pF}$		0.3			0.3		Ω
Transient response	Voltage follower, $V_{IN} = 50\text{mV}$ $R_L = 600\Omega$, $C_C = 22\text{pF}$, $C_L = 100\text{pF}$							
T_R Rise time Overshoot			20 20			20 20		ns %
Transient response	$V_{IN} = 50\text{mV}$, $R_L = 600\Omega$ $C_C = 47\text{pF}$, $C_L = 500\text{pF}$							
T_R Rise time Overshoot			50 35			50 35		ns %
AC Gain	$f = 10\text{kHz}$, $C_C = 0$ $f = 10\text{kHz}$, $C_C = 22\text{pF}$		6 2.2			6 2.2		V/mV V/mV
Gain bandwidth product	$C_C = 22\text{pF}$, $C_L = 100\text{pF}$		10			10		mHz
Slew rate	$C_C = 0$ $C_C = 22\text{pF}$		13 6			13 6		V/ μs V/ μs
Power bandwidth	$V_{OUT} = \pm 10\text{V}$, $C_C = 0$ $V_{OUT} = \pm 10\text{V}$, $C_C = 22\text{pF}$ $V_{OUT} = \pm 14\text{V}$, $R_L = 600\Omega$ $C_C = 22\text{pF}$, $V_{CC} = \pm 18\text{V}$		200 95 70			200 95 70		kHz kHz kHz

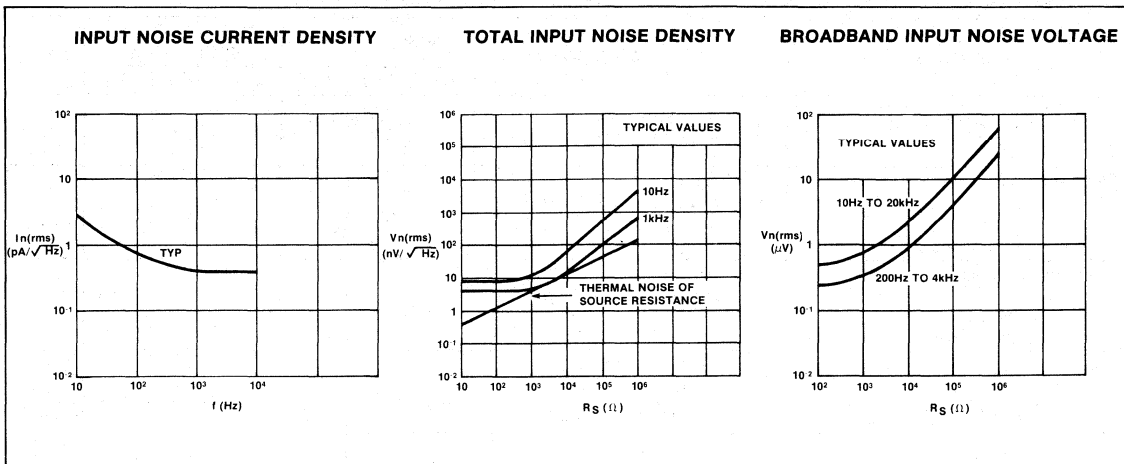
ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	5533/5534			5533A/5534A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input noise voltage	$f_o = 30\text{Hz}$ $f_o = 1\text{kHz}$		7 4			5.5 3.5	7 4.5	nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$
Input noise current	$f_o = 30\text{Hz}$ $f_o = 1\text{kHz}$		2.5 0.6			1.5 0.4		pA/ $\sqrt{\text{Hz}}$ pA/ $\sqrt{\text{Hz}}$
Broadband noise figure	$f = 10\text{Hz} - 20\text{kHz}$, $R_S = 5\text{k}\Omega$					0.9		dB
Channel separation	$f = 1\text{kHz}$, $R_S = 5\text{k}\Omega$		110			110		dB

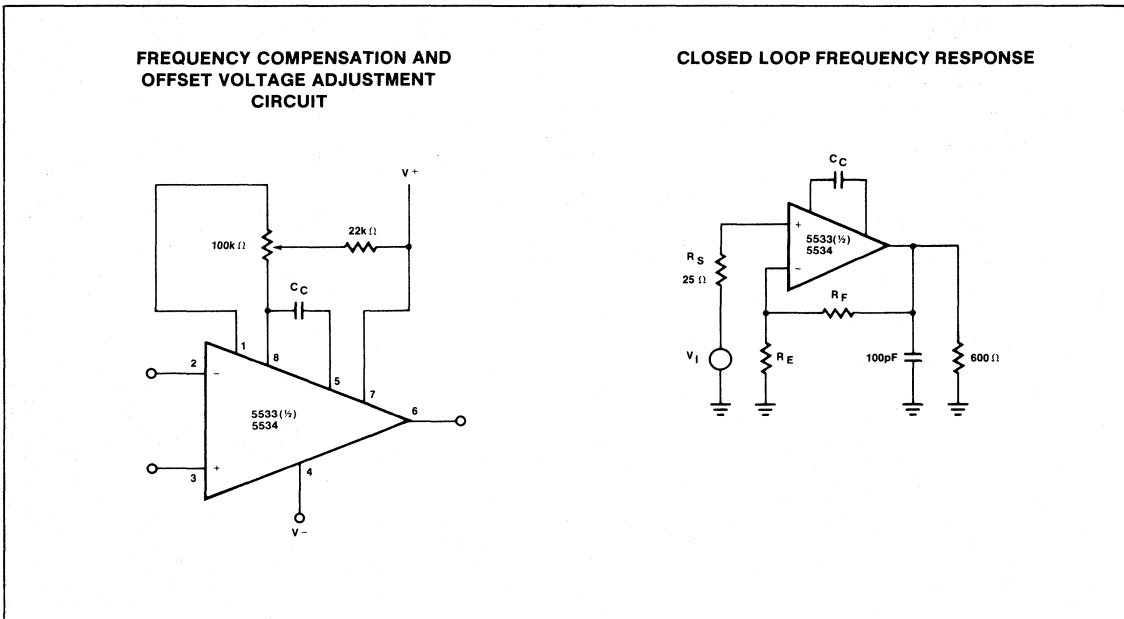
3

SINGLE AND DUAL LOW NOISE OP AMP NE5533/5533A / NE/SE5534/5534A

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



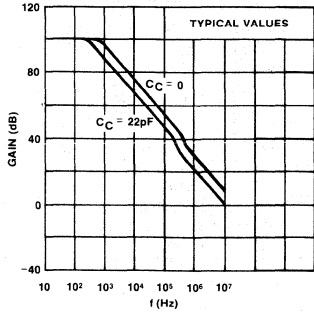
TEST LOAD CIRCUITS



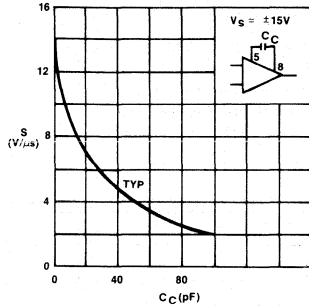
SINGLE AND DUAL LOW NOISE OP AMP NE5533/5533A / NE/SE5534/5534A

TYPICAL PERFORMANCE CHARACTERISTICS

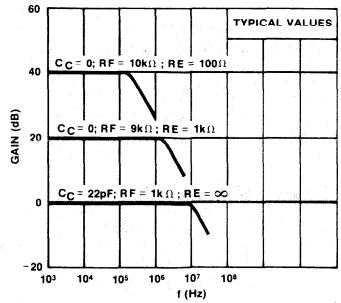
OPEN LOOP FREQUENCY RESPONSE



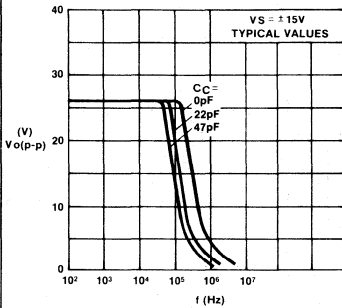
SLEW-RATE AS A FUNCTION OF COMPENSATION CAPACITANCE



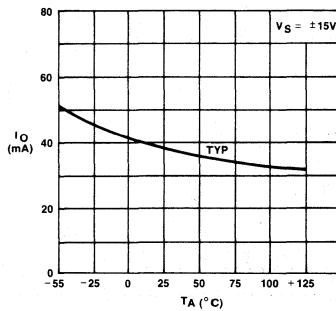
CLOSED LOOP FREQUENCY RESPONSE



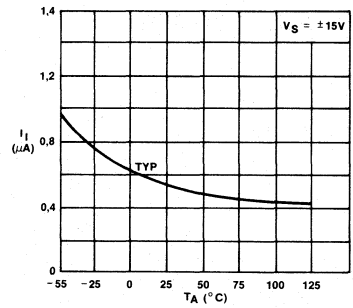
LARGE-SIGNAL FREQUENCY RESPONSE



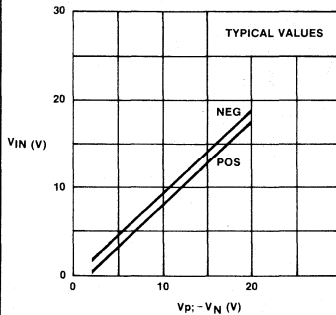
OUTPUT SHORT-CIRCUIT CURRENT



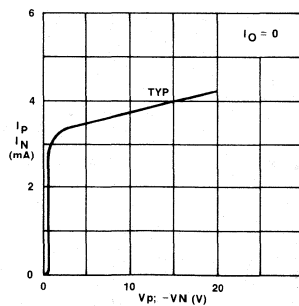
INPUT BIAS CURRENT



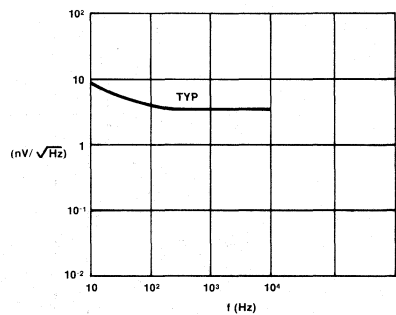
INPUT COMMON MODE VOLTAGE RANGE



SUPPLY CURRENT PER OP AMP



INPUT NOISE VOLTAGE DENSITY



3

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

NE/SE5539

DESCRIPTION

The Signetics NE5539 is a very wide bandwidth, high slew rate, monolithic operational amplifier for use in video amplifiers, RF amplifiers, and extremely high slew rate amplifiers.

Emitter follower inputs provide a true differential high input impedance device. Proper external compensation will allow design operation over a wide range of closed loop gains, both inverting and non-inverting, to meet specific design requirements.

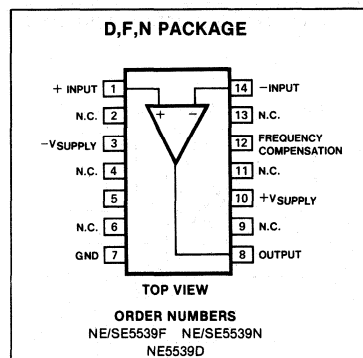
FEATURES

- Gain bandwidth product: 1.2GHz
- Slew rate: 600V/μsec
- Full power response: 48MHz
- AvOL: 50dB

APPLICATIONS

- Fast pulse amplifiers
- RF oscillators
- Fast sample and hold
- High gain video amplifiers (BW > 20MHz)

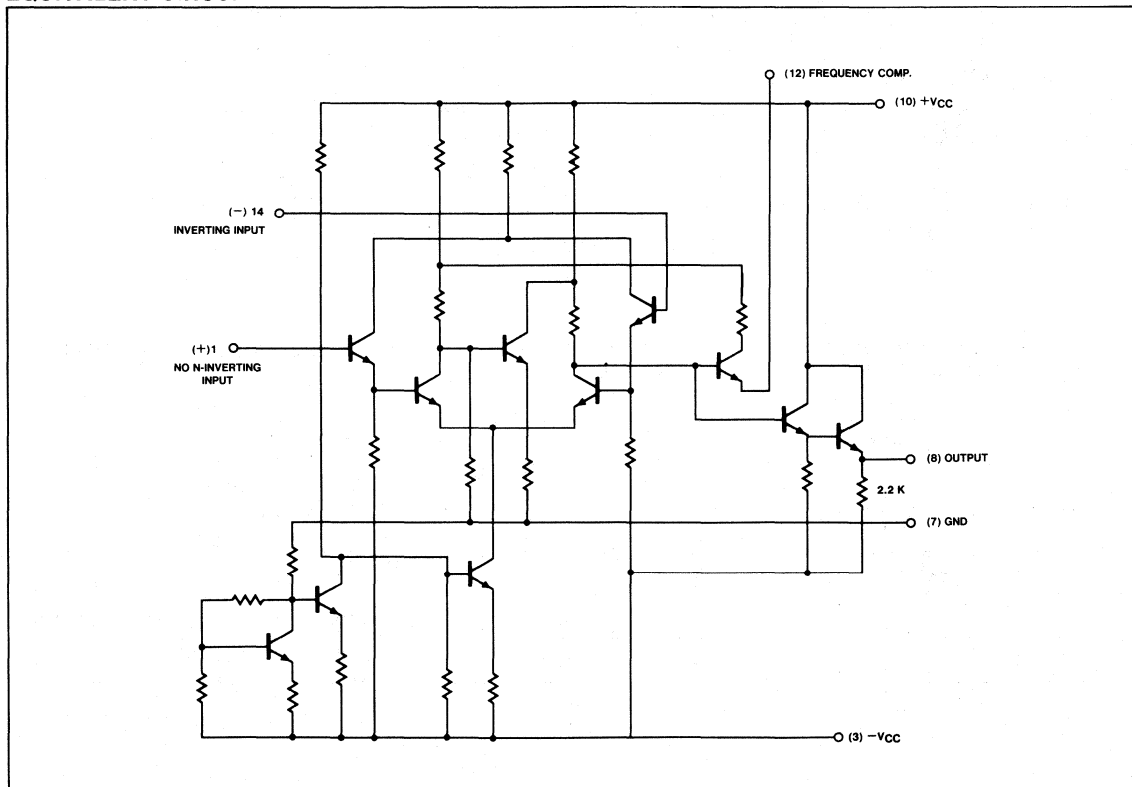
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	± 12 V
P _D	Internal power dissipation	550 mW
T _{STG}	Storage temperature range	-65 to +150 °C
T _J	Max junction temperature	150 °C
T _A	Operating temperature range	
	NE	0 to 70 °C
	SE	-55 to +125 °C
	Lead temperature	300 °C

EQUIVALENT CIRCUIT



ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

NE/SE5539

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $T_A = 25^\circ C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT	
		Min	Typ	Max	Min	Typ	Max		
V_{OS} Input offset voltage	$V_0 = 0V$, $R_S = 100\Omega$	Over temp		2	5			mV	
		$T_A = 25^\circ C$		2	3		2.5		5
I_{OS} Input offset current		Over temp		.1	3			μA	
		$T_A = 25^\circ C$.1	1				2
I_B Input bias current		Over temp		6	25			μA	
		$T_A = 25^\circ C$		5	13		5		20
CMRR Common mode rejection ratio	$F = 1\text{ kHz}$, $R_S = 100\Omega$, $V_{CM} = 1.7V$	70	80		70	85		dB	
R_{IN} Input impedance			100			100		k Ω	
R_{OUT} Output impedance			10			10		Ω	
V_{OUT} Output voltage swing	$R_L = 150\Omega$ to GND and 470Ω to $-V_{CC}$	+Swing				+2.3	+2.7	V	
		-Swing				-1.7	-2.2		
V_{OUT} Output voltage swing	$R_L = 2k\Omega$ to GND	Over temp	+Swing	+2.3	+3.0			V	
			-Swing	-1.5	-2.1				
		$T_A = 25^\circ C$	+Swing	+2.5	+3.1			V	
			-Swing	-2.0	-2.7				
I_{CC+} Positive supply current	$V_0 = 0$, $R_1 = \infty$	Over temp		14	18			mA	
		$T_A = 25^\circ C$		14	17		14		18
I_{CC-} Negative supply current	$V_0 = 0$, $R_1 = \infty$	Over temp		11	15			mA	
		$T_A = 25^\circ C$		11	14		11		15
PSRR Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$	Over temp		300	1000			$\mu V/V$	
		$T_A = 25^\circ C$					200		1000
A_{VOL} Large signal voltage gain	$V_0 = +2.3V$, $-1.7V$ $R_L = 150\Omega$ to GND, 470Ω to $-V_{CC}$					47	52	57	dB
A_{VOL} -Large signal voltage gain	$V_0 = +2.3V$, $-1.7V$ $R_L = 2K$ to GND	Over temp							dB
		$T_A = 25^\circ C$					47	52	
A_{VOL} Large signal voltage gain	$V_0 = +2.5V$, $-2.0V$ $R_L = 2\Omega$ to GND	Over temp	46		60				dB
		$T_A = 25^\circ C$	48	53	58				

NOTE

1. Differential input voltage should not exceed 0.25 volts to prevent excessive input bias current and common mode voltage 2.5 volts. These voltage limits may be exceeded if current limit is 10mA.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND & 390Ω to $-V_{CC}$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5539			NE5539			UNIT
		Min	Typ	Max	Min	Typ	Max	
Gain bandwidth product	$A_{CL} = 7$ $V_0 = 0.1\text{ Vp-p}$		1200					MHz
Small signal bandwidth	$A_{CL} = 2$ $R_L = 150\Omega$		110					MHz
Settling time	$A_{CL} = 2$ $R_L = 150\Omega$		15					nSec
Slew rate	$A_{CL} = 2$ $R_L = 150\Omega$		600			330		V/ μ Sec
Propagation delay	$A_{CL} = 2$ $R_L = 150\Omega$		7			10		nSec
Full power response	$A_{CL} = 2$ $R_L = 150\Omega$		48			20		MHz
Full power response	$A_V = 7$, $R_L = 150\Omega$		20					MHz
Wide band noise (RMS)	$B_W = 5\text{ MHz}$, $R_S = 50\Omega$		5					μV

3

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

NE/SE5539

DC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 6V$, $T_A = 25^\circ C$ unless otherwise specified

PARAMETERS	TEST CONDITIONS	SE5539			UNIT	
		Min	Typ	Max		
V_{OS} Input offset voltage	Over temp		2	5	mV	
	$T_A = 25^\circ C$		2	3		
I_{OS} Input offset current	Over temp		.1	3	μA	
	$T_A = 25^\circ C$.1	1		
I_B Input bias current	Over temp		5	20	μA	
	$T_A = 25^\circ C$		4	10		
CMRR Common mode rejection ratio	$V_{CM} = \pm 1.3V$, $R_S = 100\Omega$	70	85		dB	
I_{CC+} Positive supply current	Over temp		11	14	mA	
	$T_A = 25^\circ C$		11	13		
I_{CC-} Negative supply current	Over temp		8	11	mA	
	$T_A = 25^\circ C$		8	10		
PSRR Power supply rejection ratio	$\Delta V_{CC} = \pm 1V$		300	1000	$\mu V/V$	
V_{OUT} Output voltage swing	$R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$	Over temp	+ Swing	+ 1.4	+ 2.0	V
			- Swing	- 1.1	- 1.7	
		$T_A = 25^\circ C$	+ Swing	+ 1.5	+ 2.0	
			- Swing	- 1.4	- 1.8	

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 8V$, $R_L = 150\Omega$ to GND and 390Ω to $-V_{CC}$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE5539			UNIT
		Min	Typ	Max	
Gain bandwidth product	$A_{CL} = 7$		700		MHz
Small signal bandwidth	$A_{CL} = 2$		120		MHz
Settling time	$A_{CL} = 2$		23		ns
Slew rate	$A_{CL} = 2$		330		$V/\mu s$
Propagation delay	$A_{CL} = 2$		4.5		ns
Full power response	$A_{CL} = 2$		20		MHz

NE5539 COLOR VIDEO AMPLIFIER

The NE5539 wide band operational amplifier is easily adapted for use as a color video amplifier. A typical circuit is shown (figure 1) along with the Vectoroscope photograph showing the amplifier response to a standard NTSC color signal. (Note that the input reference vectors are displayed simultaneously with the output.) The polar representation indicates amplifier differential

phase error overall to be less than 2° . Gain also remains linear or constant with the varying input amplitudes.

The amplifier circuit was optimized for a 75Ω input and output termination impedance with a gain of 10 (20dB).

A second series of test waveforms show the amplifier's response to a 3.58MHz burst signal (figures 2 and 3).

Finally, the amplifier response is shown as a function of time for the NTSC signal with no perceptible droop or overshoot in response to step functions (see figure 4). Note that no external compensation was required since the gain was greater than 7 (17dB).

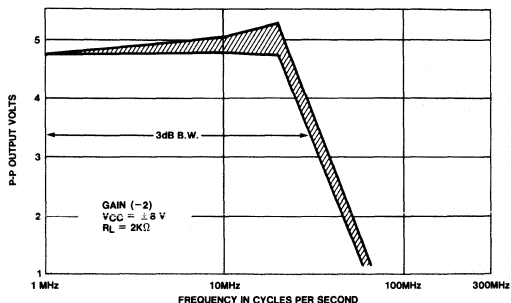
V_{CC} is ± 8 volts for all cases shown.

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

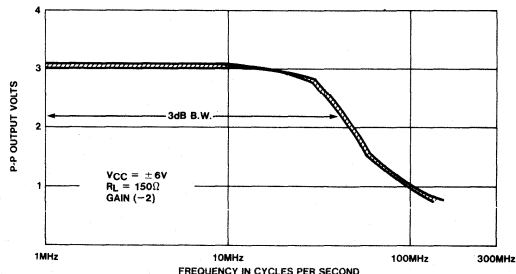
NE/SE5539

3

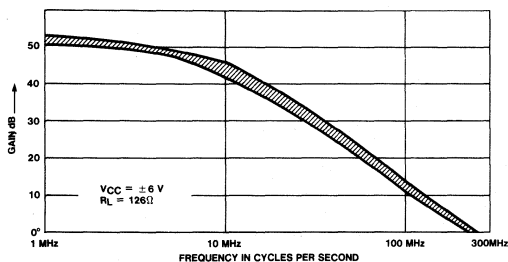
POWER BANDWIDTH (SE)



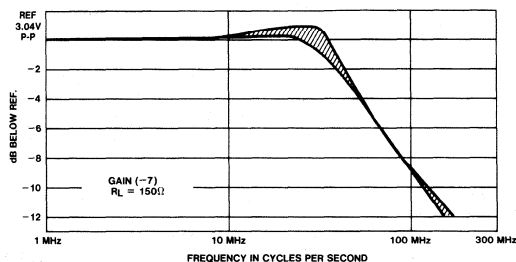
POWER BANDWIDTH (NE)



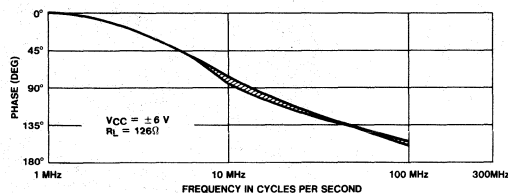
SE5539 OPEN LOOP GAIN vs FREQUENCY



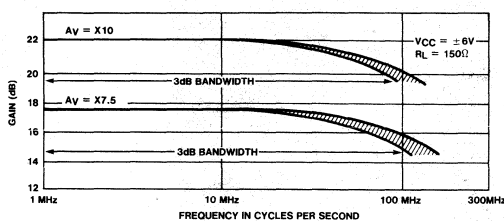
POWER BANDWIDTH




SE5539 OPEN LOOP PHASE vs FREQUENCY



GAIN BANDWIDTH PRODUCT vs FREQUENCY

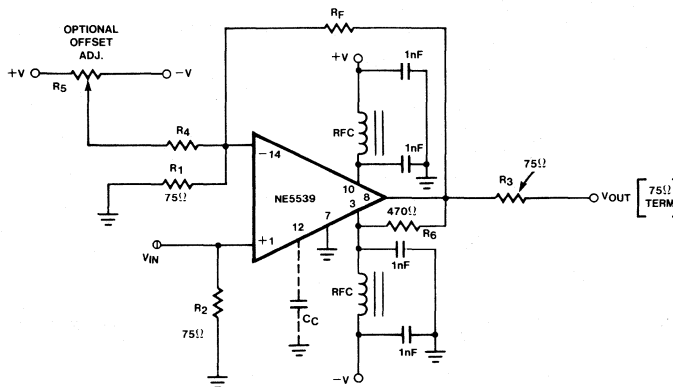


NOTE
 Indicates typical distribution $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

NE/SE5539

28dB NON-INVERTING AMP SAMPLE P.C. LAYOUT

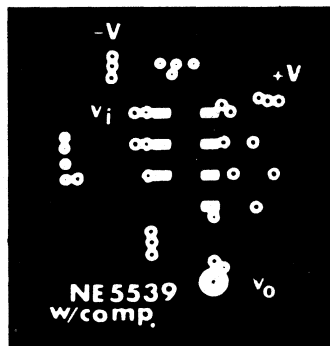


$R_1 = 75\Omega$ 5% CARBON
 $R_2 = 75\Omega$ 5% CARBON
 $R_3 = 75\Omega$ 5% CARBON
 $R_4 = 36K$ 5% CARBON

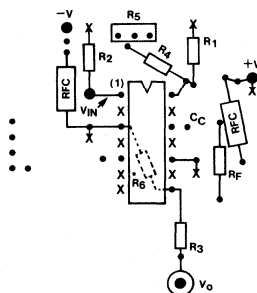
$R_5 = 20K$ TRIMPOT (CERMET)
 $R_f = 1.5K$ (28dB GAIN)
 $R_6 = 470\Omega$ 5% CARBON

RFC 3T # 26 BUSSWIRE ON
 FERROXCUBE VK 200 09/3B CORE
 BYPASS CAPACITORS
 1nF CERAMIC
 (MEPCO OR EQUIV.)

TOP PLANE COPPER¹ (Component Side)

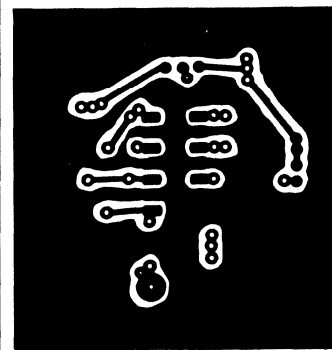


COMPONENT SIDE (Component Layout)



NOTE
 (X) indicates ground connection to top plane.
 * R_6 is on bottom side.

BOTTOM PLANE COPPER¹



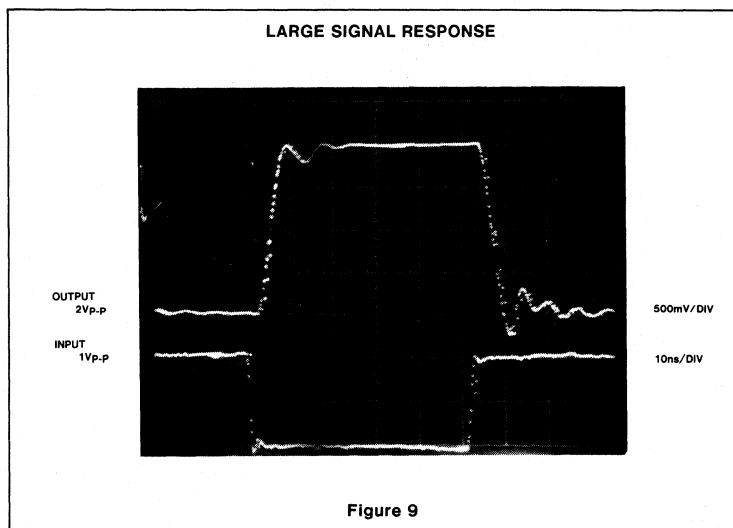
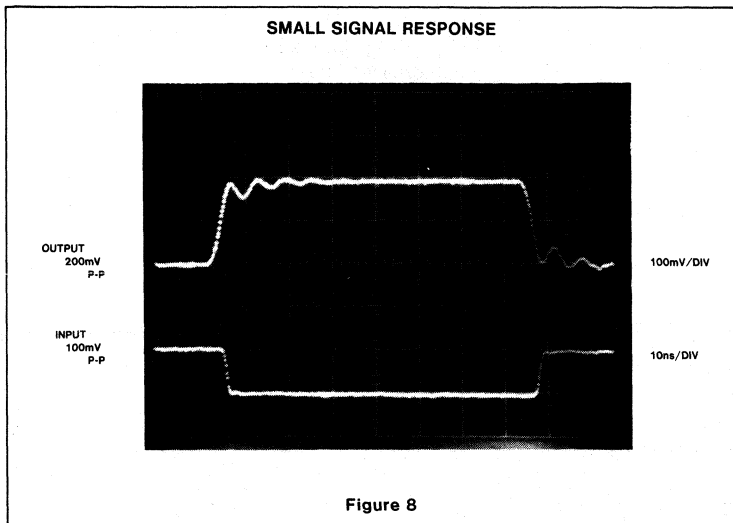
NOTE
 Bond edges of top and bottom ground plane copper.

Figure 10

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

NE/SE5539

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ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

NE/SE5539

The primary reasoning behind this procedure is to force the closed loop circuit to appear as a gain of X7 above the critical frequency where phase changes rapidly (approx. 70MHz; refer to figure 7a). The lag network raises the phase at the upper operating frequencies, greatly improving the phase margin.

The calculations below show the application of these principles to the circuit in figure 7b.

The circuit shown has an inverting gain of 2, therefore solving for R₂:

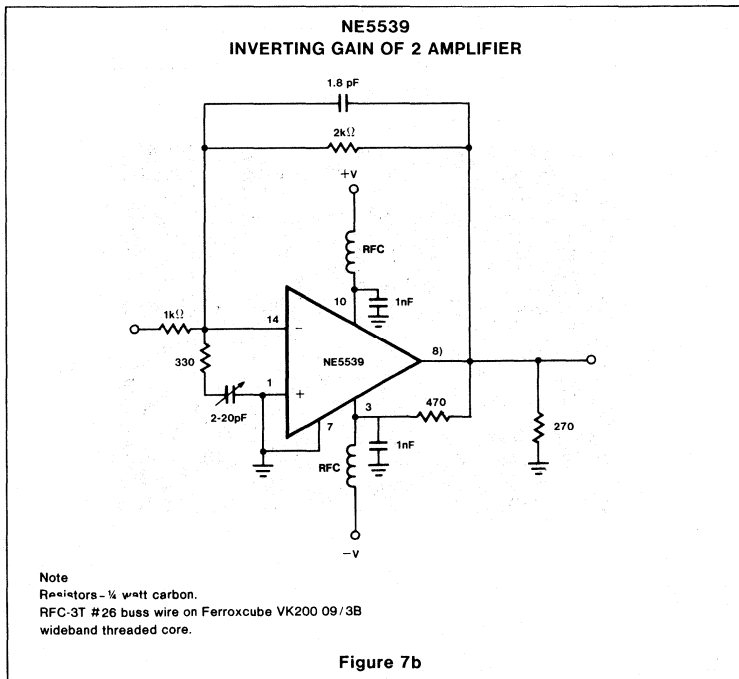
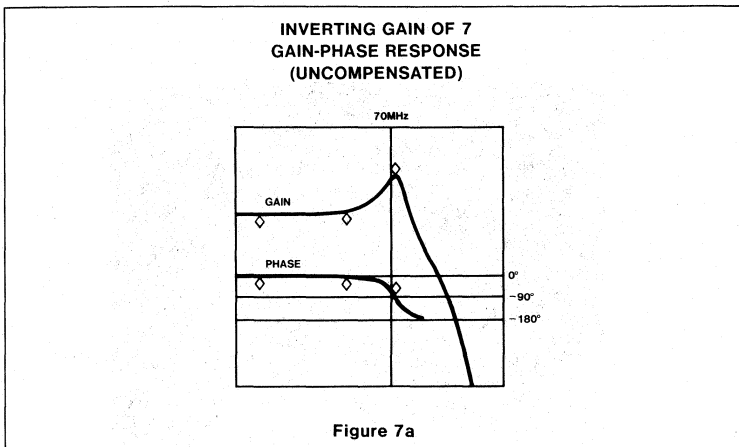
$$R_2 \cong \frac{R_f}{7 - |A_{CL}|} \cong \frac{2K}{7 - 2} = 400$$

Let R₂ = 330Ω

Assuming a gain band width product of 350 MHz, C_G may now be calculated as follows:

$$\therefore C_G \cong \frac{5}{\pi \cdot 330 \cdot 350 \cdot 10^6} \cong 14pF$$

In the circuit shown, a lead compensation capacitor of ≈ 1.6pF was used with a value of R₂ of 330Ω and C_G was a 2 - 20pF trimmer cap (JFD piston-type). Rise and fall times of 2.8 to 3ns were measured in the small signal mode with quite adequate range in the lag compensation trimmer to optimize overshoot and reduce ringing (see pulse response—figures 9 and 10).



ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

NE/SE5539

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CIRCUIT LAYOUT CONSIDERATIONS

As may be expected for an ultra-high frequency, wide gain bandwidth amplifier, the physical circuit layout is extremely critical. A double-sided printed circuit board will result in more favorable system operation (see figure 10).

The effect of the distributed and input capacitance added by the inverting node of the amplifier must be considered when calculating actual system closed loop performance. The RC product of the input resistor (R_{IN}) in parallel with C_{dist} and feedback resistor (R_F) create a pole at pin 14 (figure 5). This frequency must fall beyond the unity gain frequency of the system in order to maintain stability and system performance.

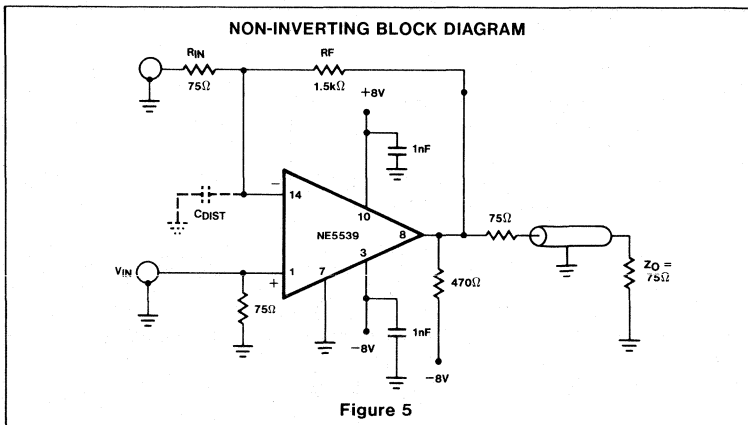


Figure 5

CLOSED LOOP GAIN LESS THAN 7

The NE5539 is stable for all closed loop gains greater than seven (7). When operating at gains less than seven (7), the device can become unstable. The circuit in figure 7 is an example of a unity gain inverting amplifier. The compensation components are added to obtain stable operation.

Capacitor C_L improves the phase margin (of the operational amplifier) by compensating for the lag introduced by the distributed capacitor (C_D).

It can be shown that the optimal conditions for amplifier stability occur when $R_1 C_D = R_F C_L$; however, when the stability criteria is obtained, it should be noted that the actual bandwidth of the closed loop amplifier will be reduced.

The actual value for C_L , based on a distributed capacitance of 3.5pFd, would be $\approx 2pF$.

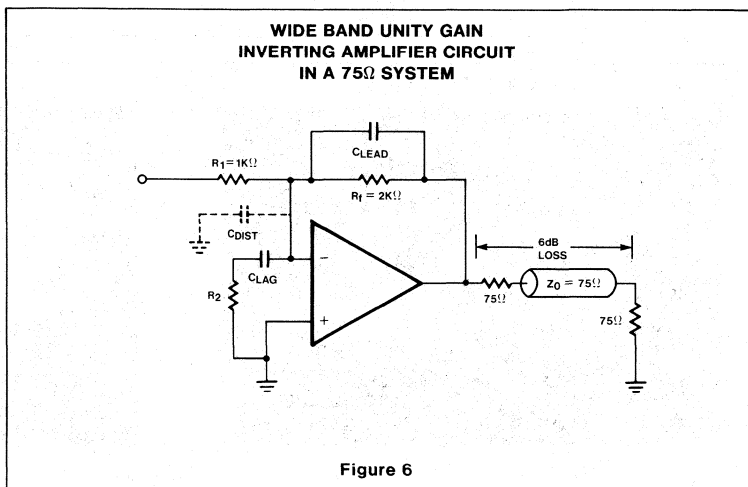


Figure 6

Determination of Compensation Capacitance:

$$C_{lead} = \frac{C_{dist}}{A_{CL}}$$

The above equation defines the relationship between the distributed capacitance, closed loop gain (A_{CL}), and the compensation capacitor (C_L). For closed loop stability and gains less than 5, C_{lead} becomes a practical consideration. When bandwidth is of primary concern, the simple lead compensation will usually be adequate. However, if transient response is also a factor in the design, then a lag compensation network (C_G, R_2) may be necessary.

For practical applications, the following equations can be used to determine the proper lag compensation components:

$$\frac{R_f}{R_1 \parallel R_2} \geq 7 \quad \text{(Equation 1)}$$

$$\therefore R_2 \leq \frac{R_f}{7 - A_{CL}} \quad \text{(Equation 2)}$$

(Using Equation 1 to insure a closed loop gain of X7 above the network break frequency allows you to solve for R_2 , the lag network resistor.)

C_{lag} may be approximated by the following equations. First set the lag network break frequency in relation to the amplifier total gain product (open loop).

$$\begin{aligned} \text{Set } \omega_{lag} &\approx \frac{2\pi \cdot \text{GBW}}{10} \text{ rad/sec} \\ &\approx \frac{\pi \cdot \text{GBW}}{5} \text{ rad/sec,} \\ \text{then } \omega_{lag} &= \frac{1}{R_2 C_{lag}} \end{aligned}$$

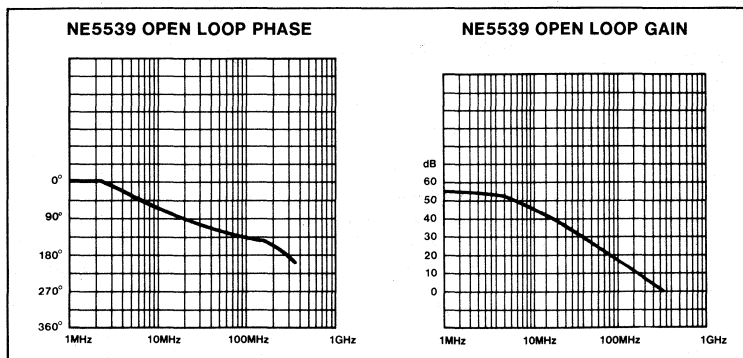
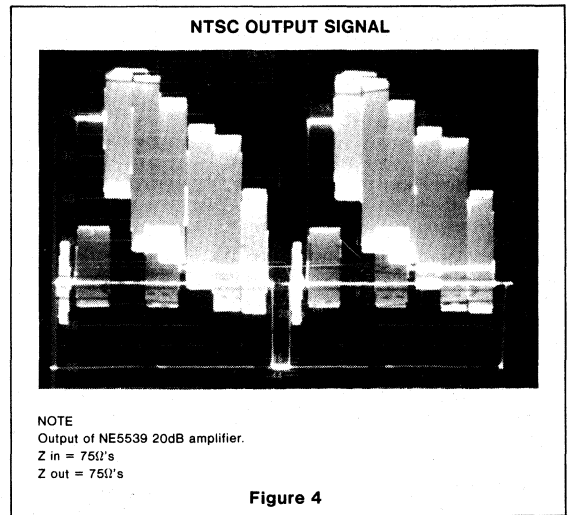
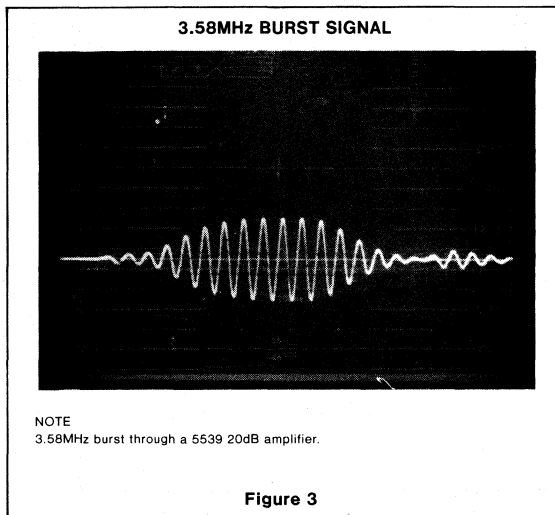
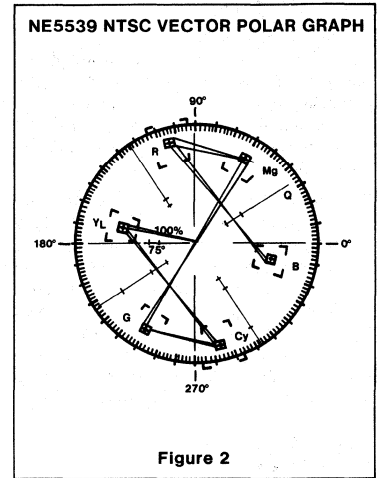
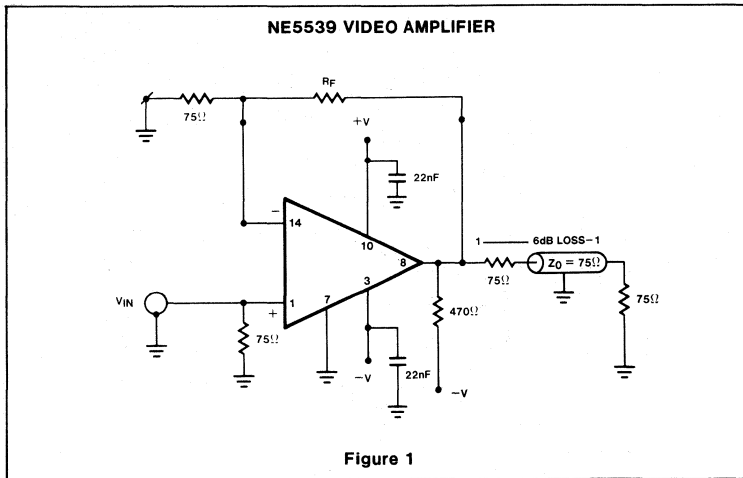
and C_{lag} may now be determined.

$$\therefore C_{lag} \approx \frac{5}{\pi \cdot R_2 \cdot \text{GBW}} \quad \text{(Equation 3)}$$

< Assume GBW = 350MHz >

ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

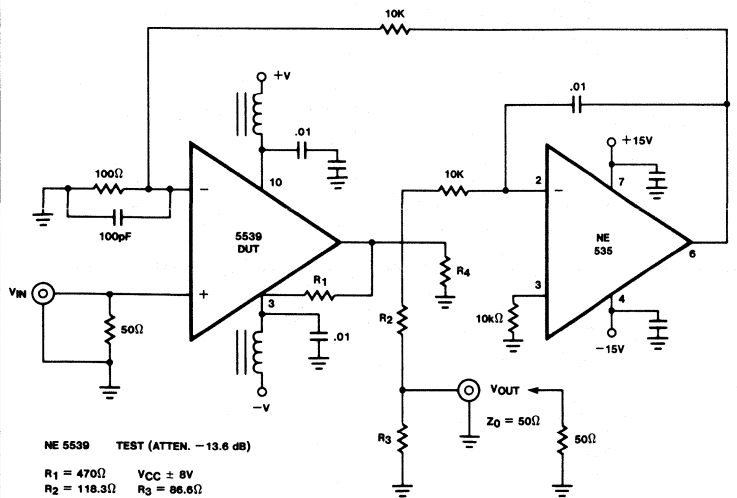
NE/SE5539



ULTRA HIGH FREQUENCY OPERATIONAL AMPLIFIER

NE/SE5539

OPEN LOOP GAIN/PHASE TEST CIRCUIT



- NE 5539 TEST (ATTEN. -13.6 dB)
- R₁ = 470Ω V_{CC} ± 8V
- R₂ = 118.3Ω R₃ = 88.6Ω
- SE 5539 TEST (ATTEN -1.7 dB) (TERMINATED)
- R₁ = 390Ω V_{CC} ± 6V
- R₂ = 140Ω
- R₃ = 75Ω R₄ = 470Ω

3

GENERAL PURPOSE OPERATIONAL AMPLIFIER

μ A741/ μ A741C/SA741C

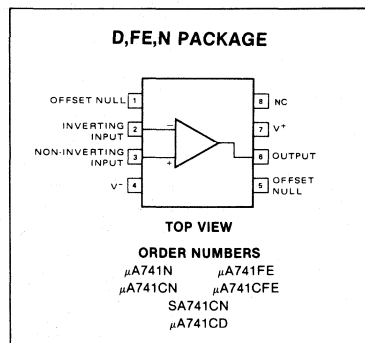
DESCRIPTION

The μ A741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μ A741 is short-circuit protected and allows for nulling of offset voltage.

FEATURES

- Internal frequency compensation
- Short circuit protection
- Excellent temperature stability
- High input voltage range

PIN CONFIGURATION



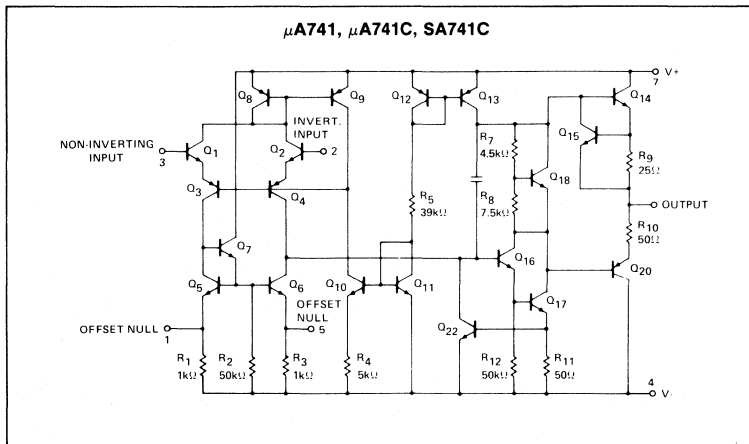
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μ A741C	± 18	V
μ A741	± 22	V
Internal power dissipation		
N package	500	mW
FE package	1000	mW
Differential input voltage	± 30	V
Input voltage ¹	± 15	V
Output short-circuit duration	Continuous	
Operating temperature range		
μ A741C	0 to +70	$^{\circ}$ C
SA741C	-40 to +85	$^{\circ}$ C
μ A741	-55 to +125	$^{\circ}$ C
Storage temperature range	-65 to +150	$^{\circ}$ C
Lead temperature (soldering 60sec)	300	$^{\circ}$ C

NOTE

1. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT SCHEMATIC



GENERAL PURPOSE OPERATIONAL AMPLIFIER

 μ A741/ μ A741C/SA741CDC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	μ A741			μ A741C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	$R_S = 10\text{k}\Omega$ $R_S = 10\text{k}\Omega$, over temp.		1.0 1.0	5.0 6.0		2.0 6.0 7.5	mV mV	
I_{OS} Offset current	Over temp. $T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$		20 7.0 20	200 200 500		20 200 300	nA nA nA nA	
I_{BIAS} Input bias current	Over temp. $T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$		80 30 300	500 500 1500		80 500 800	nA nA nA nA	
V_{OUT} Output voltage swing	$R_L = 10\text{k}\Omega$ $R_L = 2\text{k}\Omega$, over temp.	± 12 ± 10	± 14 ± 13		± 12 ± 10	± 14 ± 13	V V	
A_{VOL} Large signal voltage gain	$R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$ $R_L = 2\text{k}\Omega$, $V_O = \pm 10\text{V}$, over temp.	50 25	200		20 15	200	V/mV V/mV	
Offset voltage adjustment range			± 30			± 30	mV	
PSRR Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$ $R_S \leq 10\text{k}\Omega$, over temp.		10	150		10 150	$\mu\text{V/V}$ $\mu\text{V/V}$	
CMRR Common mode rejection ratio	Over temp.	70	90				dB dB	
I_{CC} Supply current	$T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$		1.4 1.5 2.0	2.8 2.5 3.3		1.4 2.8	mA mA mA	
V_{IN} Input voltage range	(μ A741, over temp.)	± 12	± 13		± 12	± 13	V	
R_{IN} Input resistance		0.3	2.0		0.3	2.0	M Ω	
P_d Power consumption	$T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$		50 45 45	85 75 100		50 85	mW mW mW	
R_{OUT} Output resistance			75			75	Ω	
I_{SC} Output short-circuit current			25			25	mA	

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GENERAL PURPOSE OPERATIONAL AMPLIFIER

μ A741/ μ A741C/SA741C

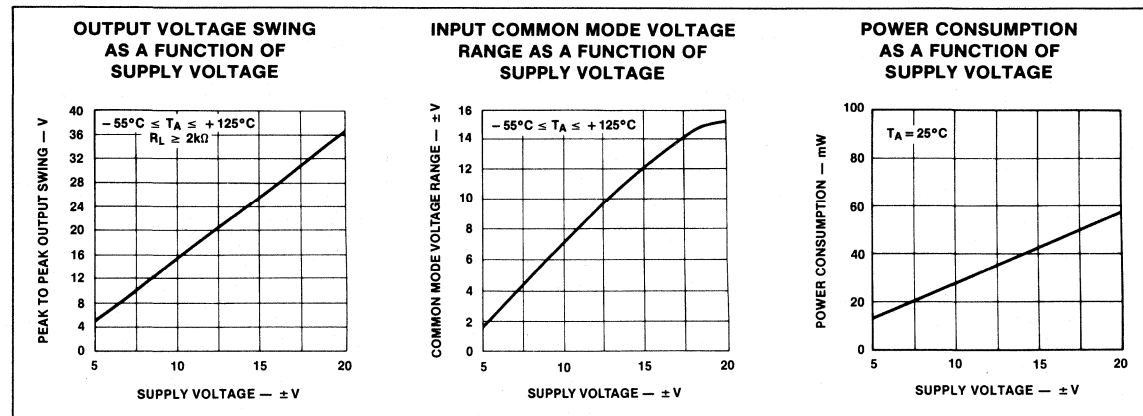
DC ELECTRICAL CHARACTERISTICS (Cont'd) $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	SA741C			UNIT
		Min	Typ	Max	
V _{OS} Offset voltage	R _S = 10k Ω R _S = 10k Ω , over temp.		2.0	6.0	mV
				7.5	mV
I _{OS} Offset current	Over temp.		20	200	nA
				500	nA
I _{BIAS} Input bias current	Over temp.		80	500	nA
				1500	nA
V _{OUT} Output voltage swing	R _L = 10k Ω R _L = 2k Ω , over temp.	± 12	± 14		V
		± 10	± 13		V
A _{VOL} Large signal voltage gain	R _L = 2k Ω , V _O = $\pm 10\text{V}$ R _L = 2k Ω , V _O = $\pm 10\text{V}$, over temp.	20	200		V/mV
		15			V/mV
Offset voltage adjustment range			± 30		mV
PSRR Supply voltage rejection ratio	R _S \leq 10k Ω		10	150	$\mu\text{V/V}$
CMRR Common mode rejection ratio					dB
I _{CC} Supply current			1.4	2.8	mA
V _{IN} Input voltage range	(μA741, over temp.)	± 12	± 13		V
		0.3	2.0		M Ω
P _d Power consumption			50	85	mW
R _{OUT} Output resistance			75		Ω
I _{SC} Output short-circuit current			25		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, unless otherwise specified.

PARAMETER	TEST CONDITIONS	μ A741, μ A741C			UNIT
		Min	Typ	Max	
Parallel input resistance	Open loop, f = 20Hz				M Ω
Parallel input capacitance	Open loop, f = 20Hz		1.4		pF
Unity gain crossover frequency	Open loop		1.0		MHz
Transient response unity gain	V _{IN} = 20mV, R _L = 2k Ω , C _L \leq 100pf				μs
Rise time			0.3		μs
Overshoot			5.0		%
Slew rate	C \leq 100pf, R _L \geq 2k, V _{IN} = $\pm 10\text{V}$		0.5		V/ μs

TYPICAL PERFORMANCE CHARACTERISTICS



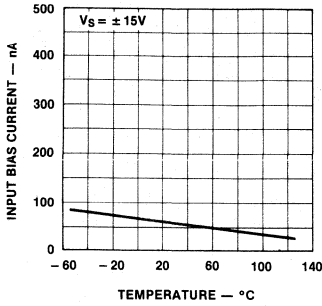
GENERAL PURPOSE OPERATIONAL AMPLIFIER

μ A741/ μ A741C/SA741C

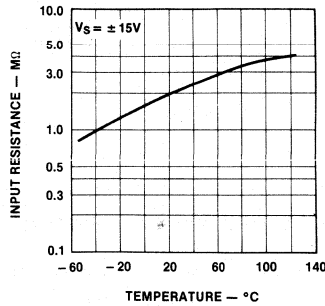
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

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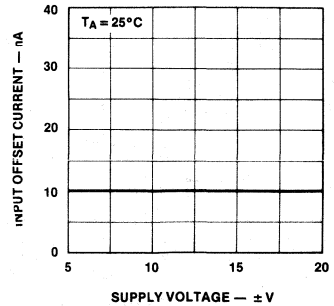
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



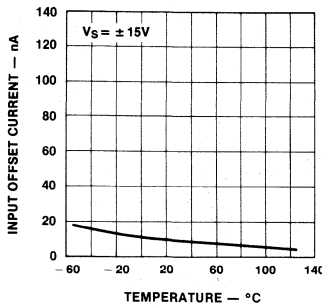
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



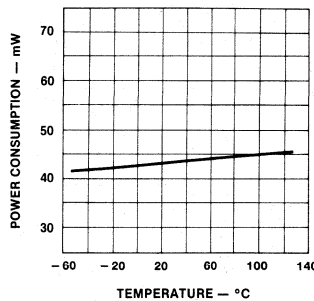
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



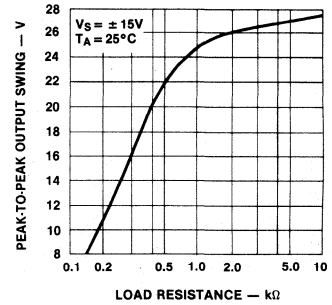
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



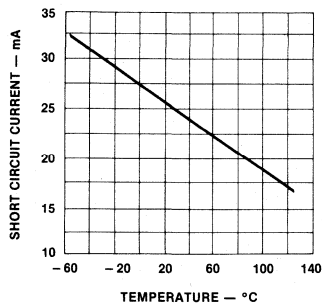
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



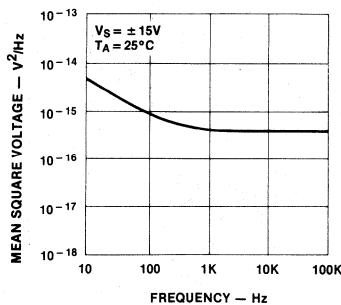
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



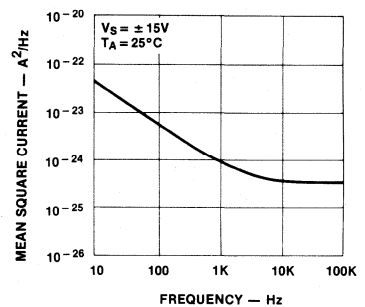
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

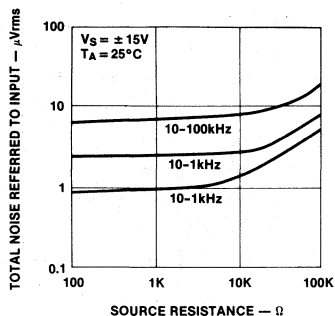


GENERAL PURPOSE OPERATIONAL AMPLIFIER

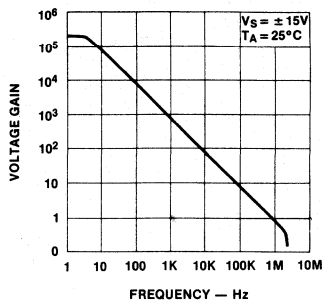
μ A741/ μ A741C/SA741C

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

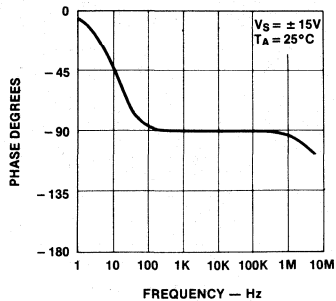
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



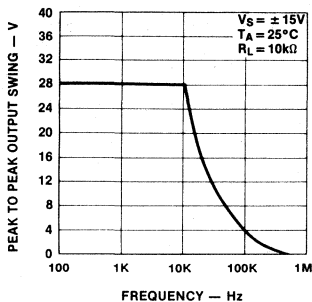
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



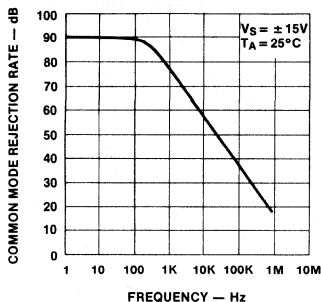
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



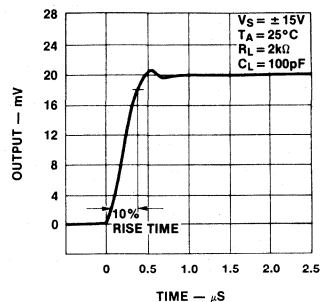
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



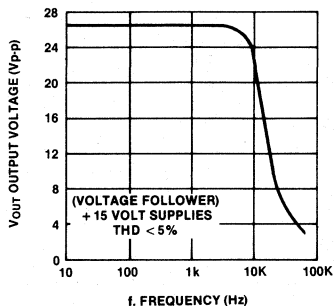
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



POWER BANDWIDTH (Large Signal Swing vs Frequency)



DUAL OPERATIONAL AMPLIFIER

μ A747/747C/SA747C

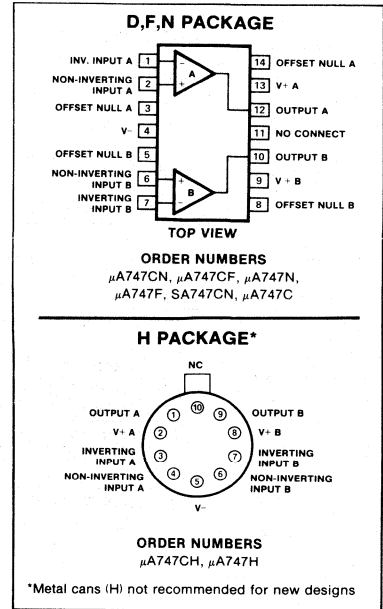
DESCRIPTION

The 747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip. High common mode voltage range and absence of "latch-up" make the 747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The 747 is short-circuit protected and requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μ A741 data sheet.

FEATURES

- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch-up

PIN CONFIGURATIONS

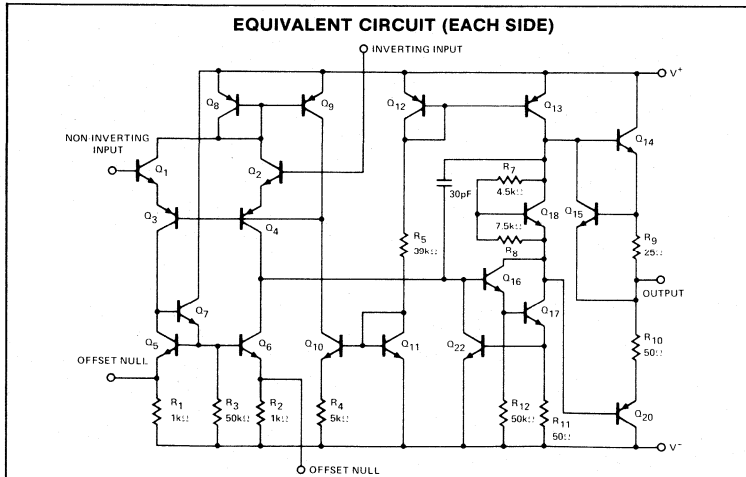


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ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μ A747	± 22	V
μ A747C	± 18	V
SA747C	± 18	V
Internal power dissipation		
H Package	500	mW
N,F Packages	670	mW
Differential input voltage	± 30	V
Input voltage	± 15	V
Voltage between offset null and V-	± 0.5	V
Storage temperature range	-65 to +155	$^{\circ}$ C
Operating temperature range		
μ A747	-55 to +125	$^{\circ}$ C
μ A747C	0 to +70	$^{\circ}$ C
SA747C	-40 to +85	$^{\circ}$ C
Lead temperature (soldering, 60 sec)	300	$^{\circ}$ C
Output short-circuit duration	indefinite	

EQUIVALENT SCHEMATIC



DUAL OPERATIONAL AMPLIFIER

 μ A747/747C/SA747CDC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SA747C			UNIT
		Min	Typ	Max	
V _{OS} Offset voltage	$R_S \leq 10\text{k}\Omega$		2.0	6.0	mV
	$R_S \leq 10\text{k}\Omega$, over temp		3.0	7.5	mV
I _{OS} Offset current	Over temp		20	200	nA
				500	nA
I _{BIAS} Input current	Over temp			500	nA
				1500	nA
V _{OUT} Output voltage swing	$R_L \geq 2\text{k}\Omega$, over temp	± 10	± 13		V
	$R_L \geq 10\text{k}\Omega$, over temp	± 12	± 14		V
I _{CC} Supply current	Over temp		1.7	2.8	mA
			2.0	3.3	mA
Power consumption	Over temp		50	85	mW
			60	100	mW
Input capacitance			1.4		pF
Offset voltage adjustment range			± 15		V
Output resistance			75		Ω
Channel separation			120		dB
PSRR Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$, over temp		30	150	$\mu\text{V}/\text{V}$
A _{VOL} Large signal voltage gain (DC)	$R_L \geq 2\text{k}\Omega$ V _{OUT} = $\pm 10\text{V}$	25,000			V/V
CMRR	$R_S \leq 10\text{k}\Omega$, V _{CM} $\pm 12\text{V}$ over temp	70			dB

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	$\mu\text{A747}/\mu\text{A747C}/\text{SA747C}$			UNIT
		Min	Typ	Max	
Transient response Risetime Overshoot	V _{IN} = 20mV, R ₁ = 2k Ω , C ₁ < 100pf Unity gain CL \leq 100pf Unity gain CL \leq 100pf		0.3		μs
			5.0		%
			0.5		V/ μs
Slew rate	R _L > 2k Ω				V/ μs

DUAL OPERATIONAL AMPLIFIER

 μ A747/747C/SA747CDC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

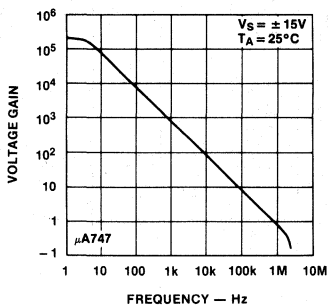
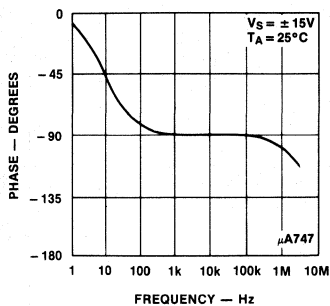
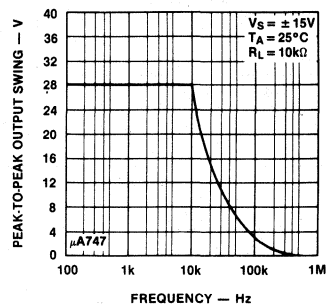
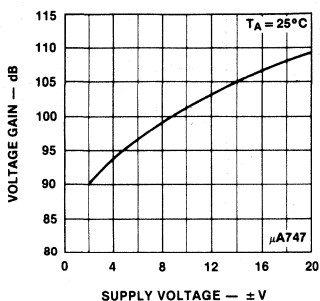
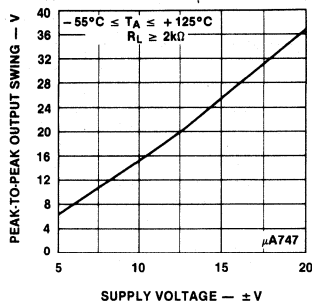
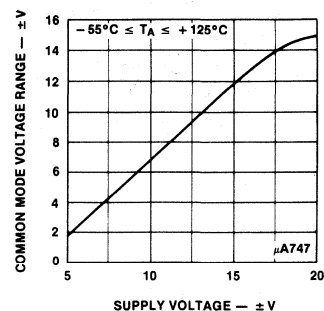
PARAMETER	TEST CONDITIONS	μ A747			μ A747C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	$R_S \leq 10\text{k}\Omega$ $R_S \leq 10\text{k}\Omega$, over temp		2.0 3.0	5.0 6.0		2.0 3.0	6.0 7.5	mV mV
I_{OS} Offset current	$T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ Over temp		20 7.0 85	200 200 500		20 7.0	200 300	nA nA nA nA
I_{BIAS} Input current	$T_A = 125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ Over temp		80 30 300	500 500 1500		80 30	500 800	nA nA nA nA
V_{OUT} Output voltage swing	$R_L \geq 2\text{k}\Omega$, over temp $R_L \geq 10\text{k}\Omega$, over temp	± 10 ± 12	± 13 ± 14		± 10 ± 12	± 13 ± 14		V V
I_{CC} Supply current each side	$T_A = 125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ Over temp		1.7 1.5 2.0	2.8 2.5 3.3		1.7 2.0	2.8 3.3	mA mA mA mA
Power consumption	$T_A = 125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ Over temp		50 45 60	85 75 100		50 60	85 100	mW mW mW mW
Input capacitance			1.4			1.4		pF
Offset voltage adjustment range			± 15			± 15		V
Output resistance			75			75		Ω
Channel separation			120			120		dB
PSRR Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$, over temp		30	150		30	150	$\mu\text{V}/\text{V}$
A_{VOL} Large signal voltage gain (DC)	$R_L \geq 2\text{k}\Omega$ $V_{OUT} = \pm 10\text{V}$ Over temp	50,000 25,000			25,000 15,000			V/V V/V
CMRR	$R_S \leq 10\text{k}\Omega$, $V_{CM} \pm 12\text{V}$ over temp	70			70			dB

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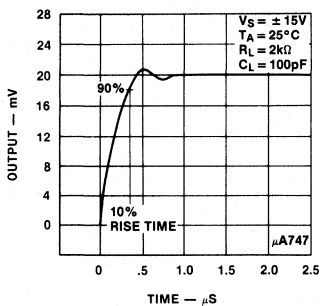
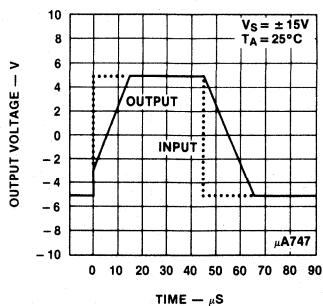
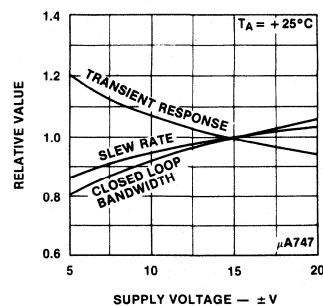
DUAL OPERATIONAL AMPLIFIER

 μ A747/747C/SA747C

TYPICAL PERFORMANCE CHARACTERISTICS

OPEN LOOP VOLTAGE GAIN
AS A FUNCTION OF
FREQUENCYOPEN LOOP PHASE RESPONSE
AS A FUNCTION OF
FREQUENCYOUTPUT VOLTAGE SWING
AS A FUNCTION OF
FREQUENCYOPEN LOOP VOLTAGE GAIN
AS A FUNCTION OF
SUPPLY VOLTAGEOUTPUT VOLTAGE SWING
AS A FUNCTION OF
SUPPLY VOLTAGEINPUT COMMON MODE VOLTAGE
RANGE AS A FUNCTION OF
SUPPLY VOLTAGE

TRANSIENT RESPONSE

VOLTAGE FOLLOWER
LARGE SIGNAL PULSE
RESPONSEFREQUENCY CHARACTERISTICS
AS A FUNCTION OF
SUPPLY VOLTAGE

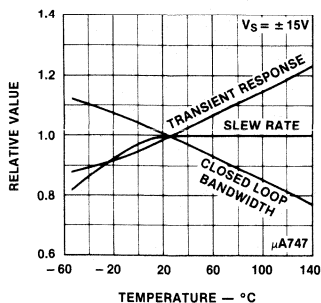
DUAL OPERATIONAL AMPLIFIER

μ A747/747C/SA747C

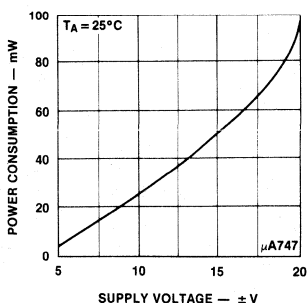
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

3

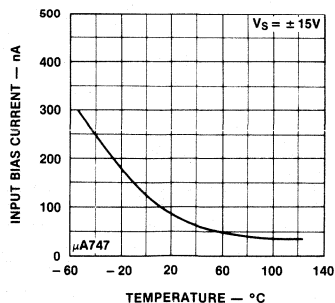
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



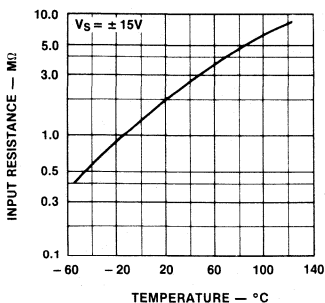
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



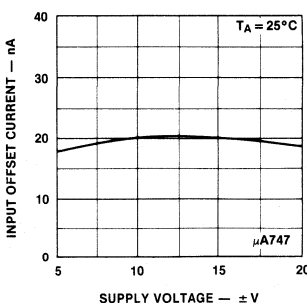
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



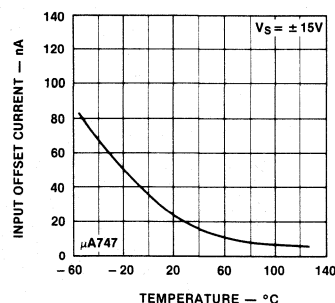
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



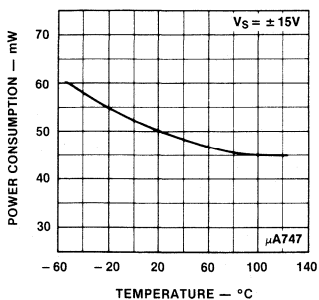
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



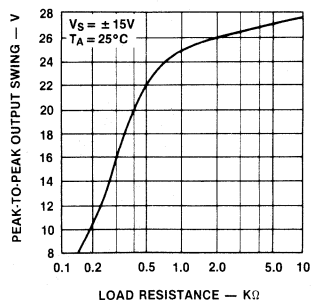
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



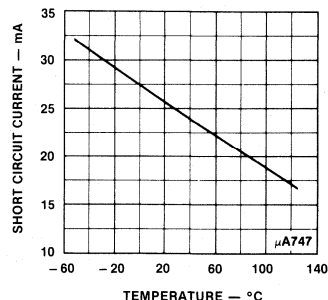
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

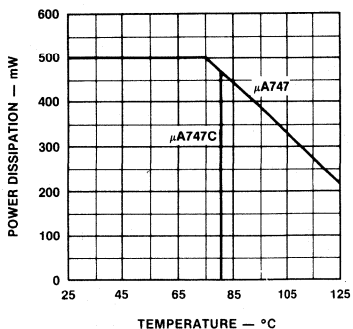


DUAL OPERATIONAL AMPLIFIER

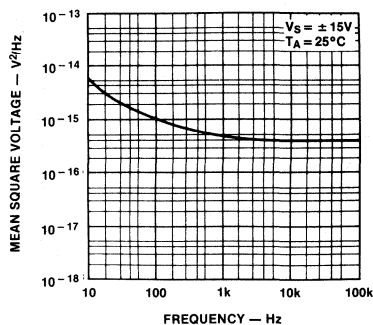
μ A747/747C/SA747C

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

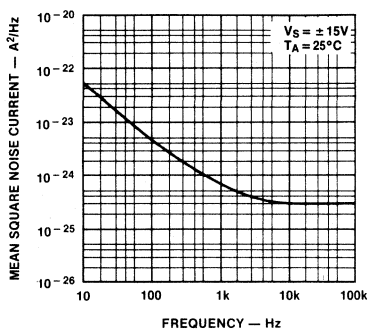
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



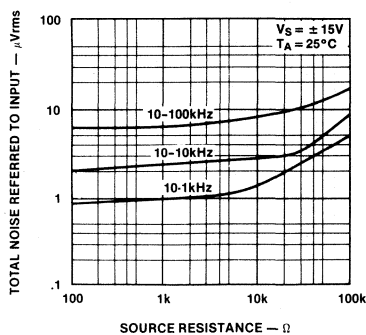
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

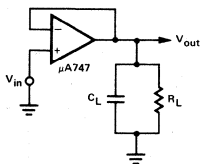


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

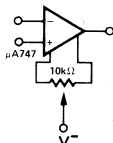


TEST CIRCUITS

TRANSIENT RESPONSE TEST CIRCUIT



VOLTAGE OFFSET NULL CIRCUIT



GENERAL PURPOSE OPERATIONAL AMPLIFIER

μ A748/748C

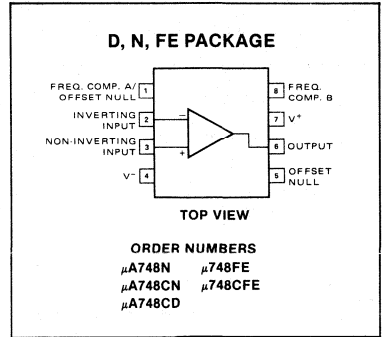
DESCRIPTION

The 748 is a High Performance Operational Amplifier featuring high gain, short circuit immunity, offset voltage null capability, simplified compensation and excellent temperature stability.

FEATURES

- Short circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch-up

PIN CONFIGURATION



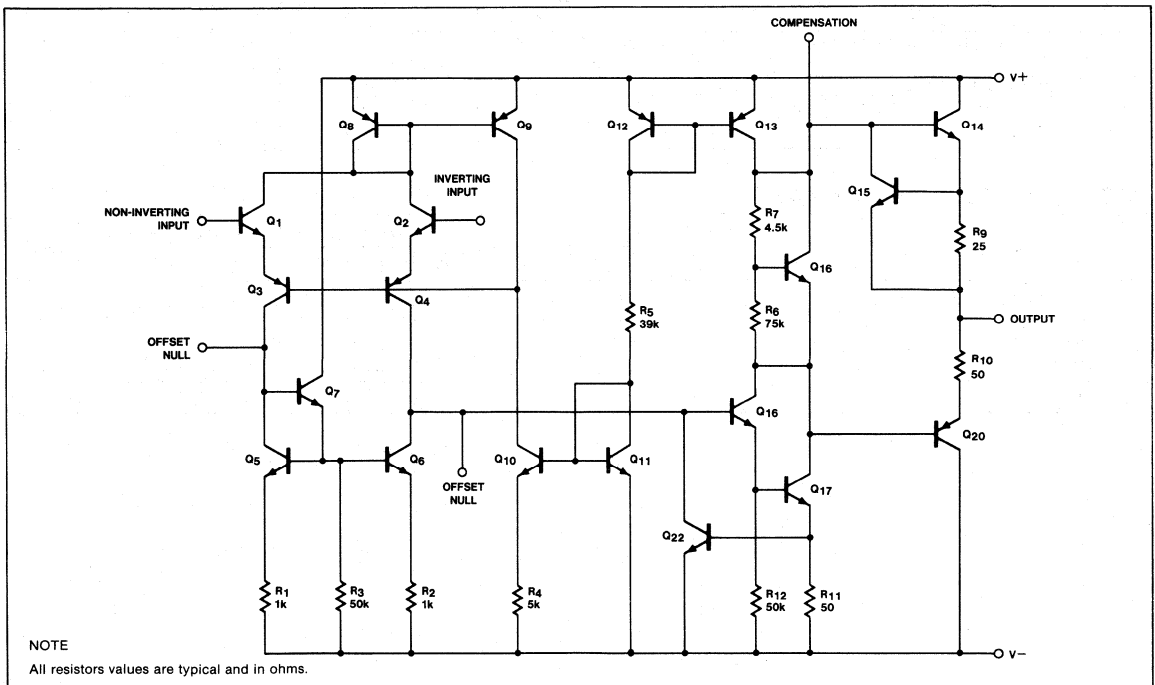
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
μ A748	± 22	V
μ A748C	± 18	V
Internal power dissipation ¹	500	mW
Differential output voltage	± 30	V
Input voltage ²	± 15	V
Storage temperature range	-65 to +150	$^{\circ}$ C
Operating temperature range		
μ A748	-55 to +125	$^{\circ}$ C
μ A748C	0 to +70	$^{\circ}$ C
Lead temperature	300	$^{\circ}$ C
Output short circuit duration ³	indefinite	

NOTES

1. Rating applies for case temperatures to +70 $^{\circ}$ C.
2. For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +70 $^{\circ}$ C ambient temperature.

EQUIVALENT CIRCUIT



NOTE

All resistors values are typical and in ohms.

3

GENERAL PURPOSE OPERATIONAL AMPLIFIER

 μ A748/748CDC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS [§]	μ A748			μ A748C			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage	$R_S \leq 10\text{k}\Omega$, $T_A = 25^\circ\text{C}$ Over temperature		1.0	5.0 6.0		2.0	6.0 7.5	mV mV
I_{OS} Offset current	$25^\circ \leq T_A \leq T_{max}$ $T_{min} \leq T_A \leq 25^\circ\text{C}$		20 7.0 85	200 200 500		20 9.0 35	200 300 300	nA nA nA
I_{BIAS} Input current	$25^\circ \leq T_A \leq T_{max}$ $T_{min} \leq T_A \leq 25^\circ\text{C}$		80 30 300	500 500 1500		80 40 130	500 800 800	nA nA nA
V_{CM} Common mode voltage range	Over temperature	± 12	± 13		± 12	± 13		V

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	μ A748			μ A748C			UNIT
		Min	Typ	Max	Min	Typ	Max	
CMRR Common mode rejection ratio	$R_S \leq \pm 10\text{k}\Omega$, over temperature	70	90		70	90		dB
R_{IN} Input resistance		0.3	2.0		.30	2.0		M Ω
V_{OUT} Output voltage swing	$R_L \geq 2\text{k}\Omega$, over temperature $R_L \geq 10\text{k}\Omega$, over temperature	± 10 ± 12	± 13 ± 14		± 10 ± 12	± 13 ± 14		V V
I_{CC} Supply current	$25^\circ \leq T_A \leq T_{max}$ $T_{min} \leq T_A \leq 25^\circ\text{C}$		1.7 1.5 2.0	2.83 2.50 3.33		1.7 1.6 1.8	2.83 3.33 3.33	mA mA mA
P_d Power consumption	$T_A = 25^\circ\text{C}$ $25^\circ \leq T_A \leq T_{max}$ $T_{min} \leq T_A \leq 25^\circ\text{C}$		50 45 60	85 75 100		50 48 54	85 100 100	mW mW mW
PSRR Supply voltage rejection ratio	$R_S \leq 10\text{k}\Omega$, over temperature		30	150		30	150	$\mu\text{V}/\text{V}$
Output resistance	$T_A = 25^\circ\text{C}$		75			75		Ω
A_{VOL} Large signal voltage gain	$R_L \geq 2\text{k}\Omega$ $V_{OUT} \pm 10\text{V} \pm 15\text{V}$ Over temperature	50 25	200		50 25	200		V/mV V/mV
Input capacitance			1.4			1.4		pF
Offset voltage adjustment range			± 15			± 15		mV

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	μ A748			μ A748C/SA748C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient response (unity gain)	$V_{IN} = 20\text{mV}$, $R_L = 2\text{k}\Omega$ $C_L \leq 100\text{pF}$ $C_1 = 30\text{pF}$							
Rise time			0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew rate	$R_L \geq 2\text{k}\Omega$ $C_1 = 30\text{pF}$		0.5			0.5		V/ μs

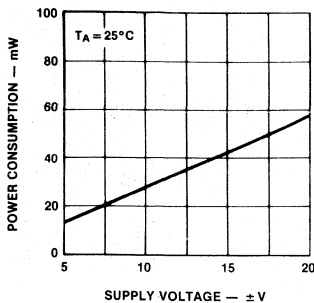
GENERAL PURPOSE OPERATIONAL AMPLIFIER

μ A748/748C

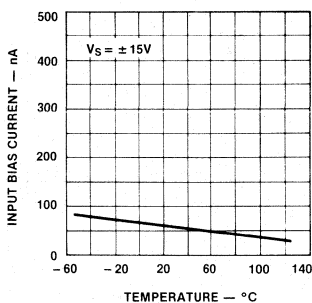
TYPICAL CHARACTERISTIC CURVES

3

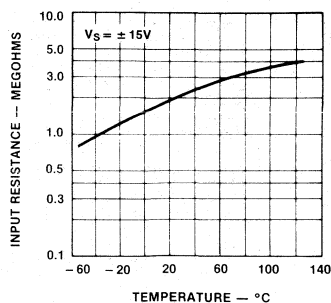
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



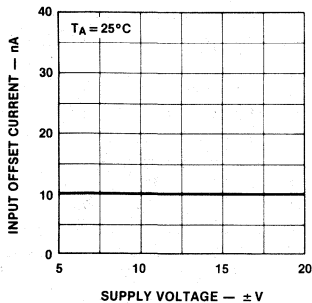
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



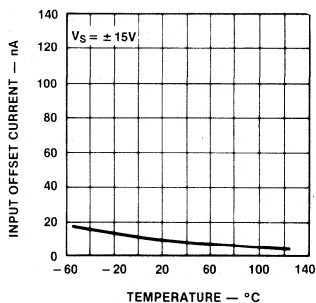
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



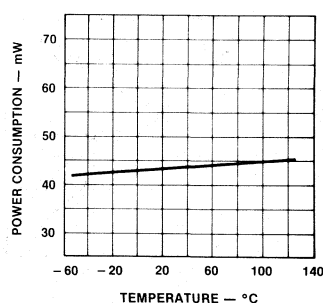
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



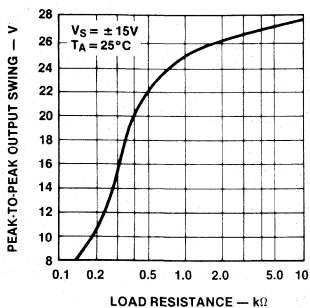
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



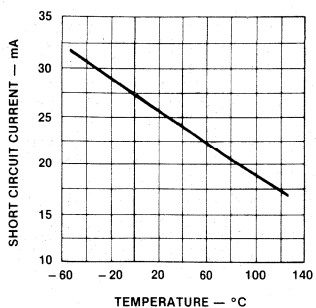
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



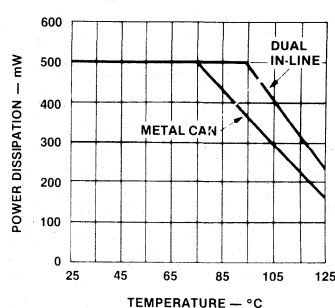
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

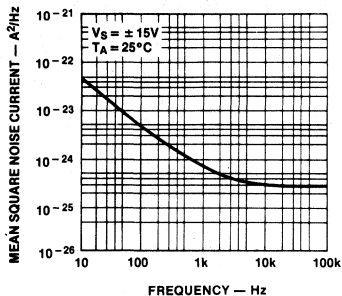


GENERAL PURPOSE OPERATIONAL AMPLIFIER

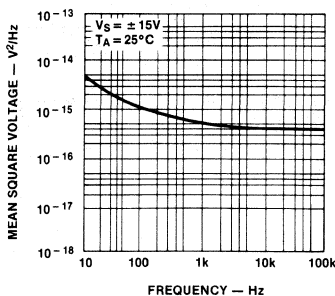
μ A748/748C

TYPICAL CHARACTERISTIC CURVES (Cont'd)

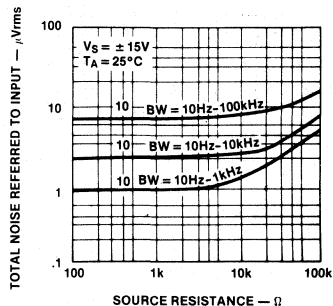
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



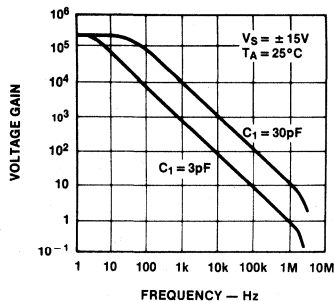
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



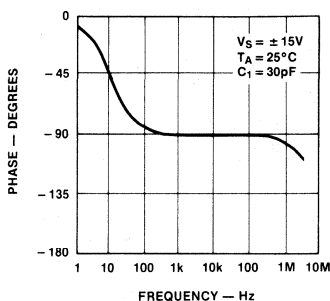
BROADBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



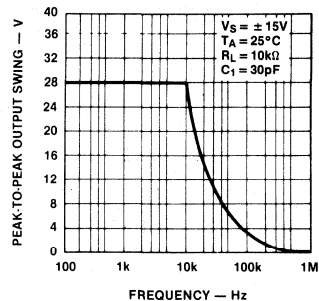
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



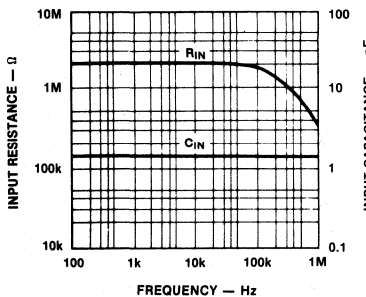
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



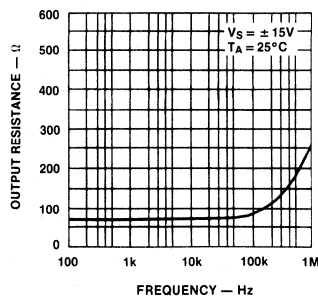
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



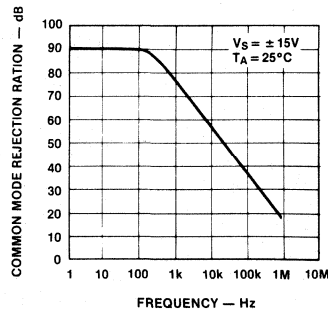
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

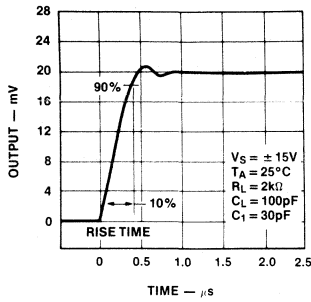


GENERAL PURPOSE OPERATIONAL AMPLIFIER

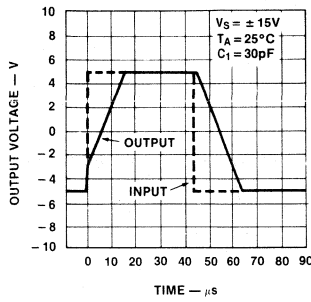
μ A748/748C

TYPICAL CHARACTERISTIC CURVES (Cont'd)

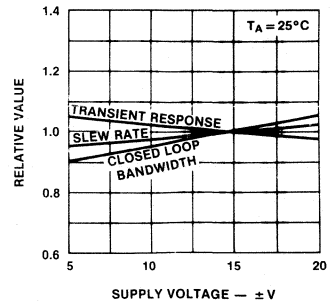
TRANSIENT RESPONSE



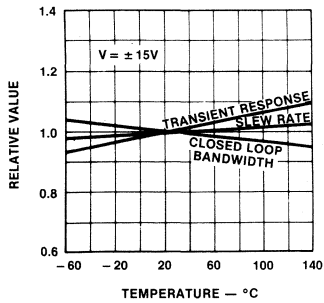
**VOLTAGE FOLLOWER
LARGE SIGNAL PULSE RESPONSE**



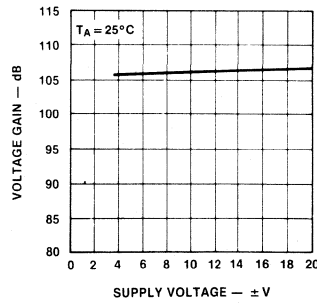
**FREQUENCY CHARACTERISTICS
AS A FUNCTION OF
SUPPLY VOLTAGE**



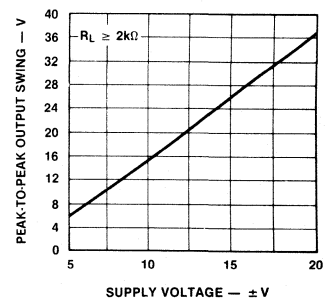
**FREQUENCY CHARACTERISTICS
AS A FUNCTION OF
AMBIENT TEMPERATURE**



**OPEN LOOP VOLTAGE GAIN
AS A FUNCTION OF
SUPPLY VOLTAGE**



**OUTPUT VOLTAGE SWING
AS A FUNCTION OF
SUPPLY VOLTAGE**



3

Section 4 Video Amplifiers

INDEX

Section 4 — Video Amplifiers

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NE/SE592	4-3
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Video Amplifier	4-3
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VIDEO AMPLIFIER

NE/SE592

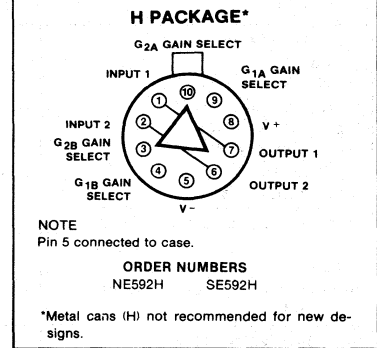
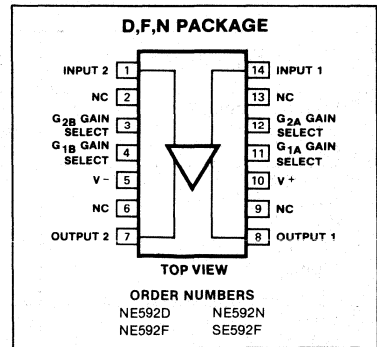
DESCRIPTION

The SE/NE592 is a monolithic, two stage, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display, video recorder systems, and floppy disc head amplifiers. The 592 is a pin-for-pin replacement for the μ A733.

FEATURES

- 120MHz bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required
- Wave shaping with minimal external components

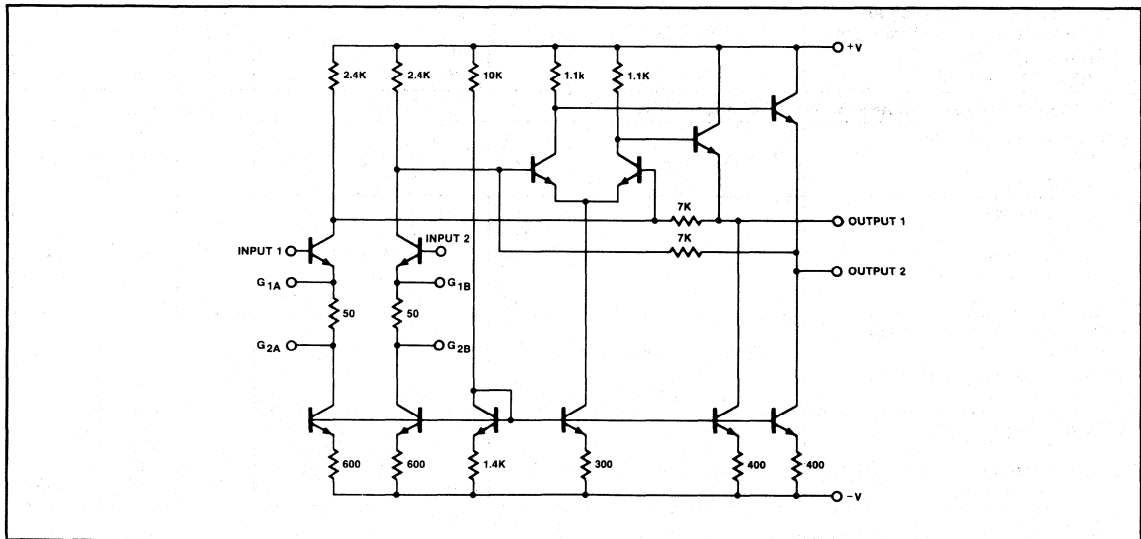
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	RATING	UNIT
Supply voltage	± 8	V
Differential input voltage	± 5	V
Common mode Input voltage	± 6	V
Output current	10	mA
Operating temperature range		
SE592K	-55 to +125	$^\circ\text{C}$
NE592K	0 to +70	$^\circ\text{C}$
Storage temperature range	-65 to +150	$^\circ\text{C}$
Power dissipation	500	mW

EQUIVALENT CIRCUIT



4

VIDEO AMPLIFIER

NE/SE592

DC ELECTRICAL CHARACTERISTICS $T_A = +25^\circ\text{C}$, $V_S = \pm 6\text{V}$, $V_{CM} = 0$ unless otherwise specified.
 Recommended operating supply voltages $V_S = \pm 6.0\text{V}$

PARAMETER	TEST CONDITIONS	NE592			SE592			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain Gain 1 ¹ Gain 2 ²	$R_L = 2\text{k}\Omega$, $V_{OUT} = 3\text{V p-p}$	250 80	400 100	600 120	300 90	400 100	500 110	V/V V/V
Bandwidth Gain 1 ¹ Gain 2 ²			40 90			40 90		MHz MHz
Rise Time Gain 1 ¹ Gain 2 ²	$V_{OUT} = 1\text{V p-p}$		10.5 4.5	12		10.5 4.5	10	ns ns
Propagation delay Gain 1 ¹ Gain 2 ²	$V_{OUT} = 1\text{V p-p}$		7.5 6.0	10		7.5 6.0	10	ns ns
Input resistance Gain 1 ¹ Gain 2 ²		10	4.0 30		20	4.0 30		k Ω k Ω
Input capacitance ²	Gain 2		2.0			2.0		pF
Input offset current			0.4	5.0		0.4	3.0	μA
Input bias current			9.0	30		9.0	20	μA
Input noise voltage	BW 1kHz to 10MHz		12			12		μVrms
Input voltage range				± 1.0			± 1.0	V
Common mode rejection ratio Gain 2	$V_{CM} \pm 1\text{V}$, $F < 100\text{kHz}$	60	86		60	86		dB
Gain 2	$V_{CM} \pm 1\text{V}$, $F = 5\text{MHz}$		60			60		dB
Supply voltage rejection ratio Gain 2	$\Delta V_S = \pm 0.5\text{V}$	50	70		50	70		dB
Output offset voltage Gain 2 ²	$R_L = \infty$		0.35	0.75		0.35	0.75	V
Output common mode voltage	$R_L = \infty$	2.4	2.9	3.4	2.4	2.9	3.4	V
Output voltage swing differential	$R_L = 2\text{K}$	3.0	4.0		3.0	4.0		V
Output resistance			20			20		Ω
Power supply current	$R_L = \infty$		18	24		18	24	mA
THE FOLLOWING SPECS APPLY OVER TEMPERATURE		$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$			$-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			
Differential voltage gain Gain 1 ¹ Gain 2 ²	$R_L = 2\text{k}\Omega$, $V_{OUT} = 3\text{V p-p}$	250 80		600 120	200 80		600 120	V/V V/V
Input resistance Gain 2 ²		8.0			8.0			k Ω
Input offset current				6.0			5.0	μA
Input bias current				40			40	μA
Input voltage range		± 1.0			± 1.0			V
Common mode rejection ratio Gain 2	$V_{CM} \pm 1\text{V}$, $F < 100\text{kHz}$	50			50			dB
Supply voltage rejection ratio Gain 2	$\Delta V_S = \pm 0.5\text{V}$	50			50			dB
Output offset voltage Gain 2 ²	$R_L = \infty$			0.75			0.75	V
Output voltage swing differential	$R_L = 2\text{K}$	2.5			2.5			V
Power supply current	$R_L = \infty$			27			27	mA

NOTES

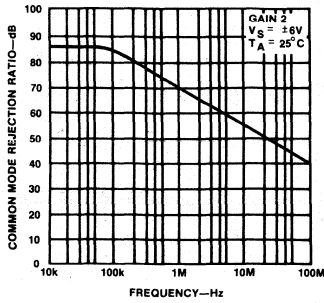
- Gain select pins G_{1A} and G_{1B} connected together.
- Gain select pins G_{2A} and G_{2B} connected together.
- All gain select pins open.

VIDEO AMPLIFIER

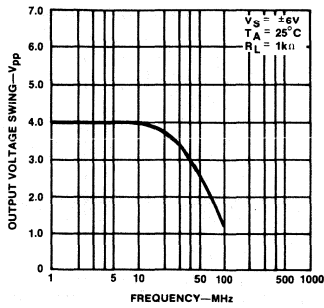
NE/SE592

TYPICAL PERFORMANCE CHARACTERISTICS

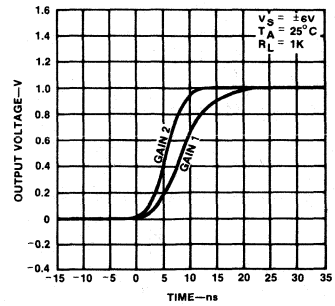
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

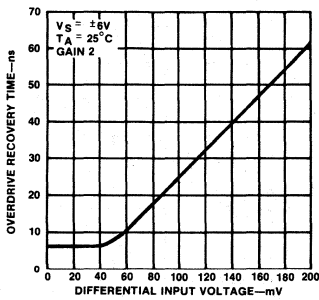


PULSE RESPONSE

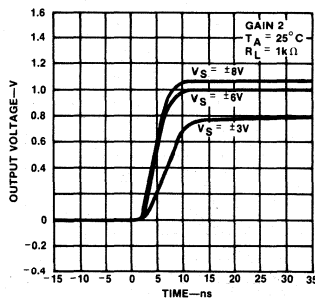


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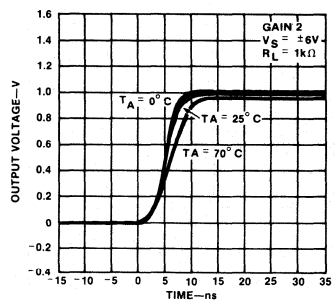
DIFFERENTIAL OVERDRIVE RECOVERY TIME



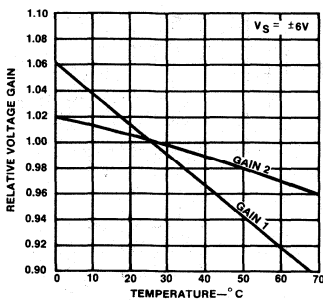
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



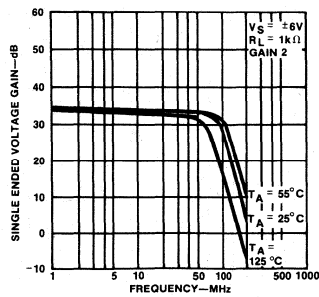
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



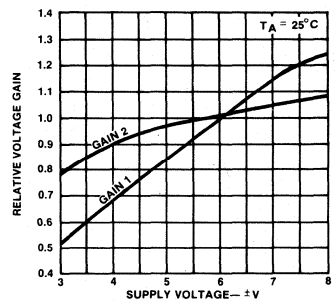
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE



VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

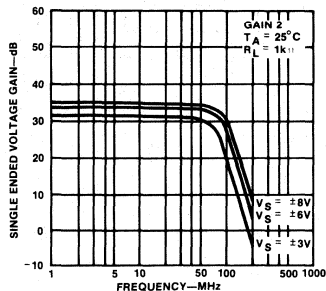


VIDEO AMPLIFIER

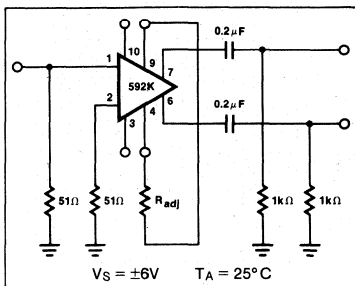
NE/SE592

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

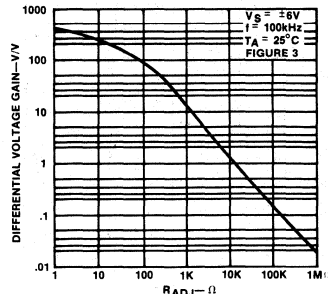
GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



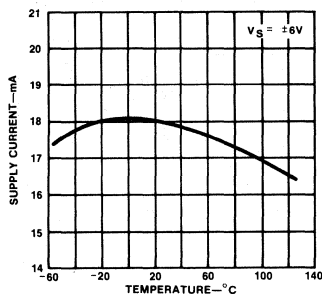
VOLTAGE GAIN ADJUST CIRCUIT



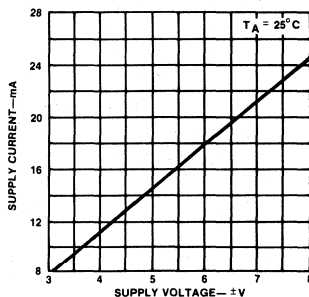
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



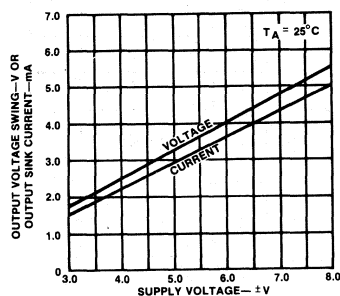
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



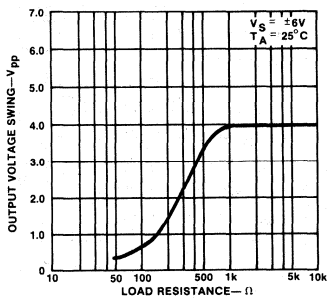
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



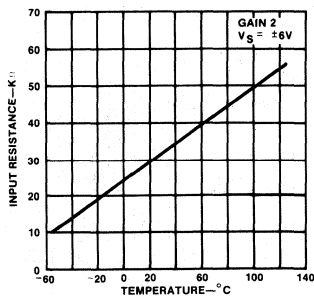
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



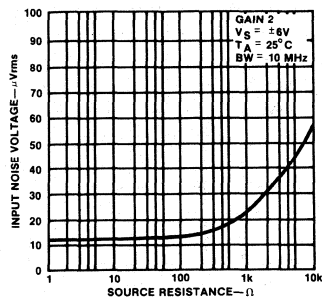
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE

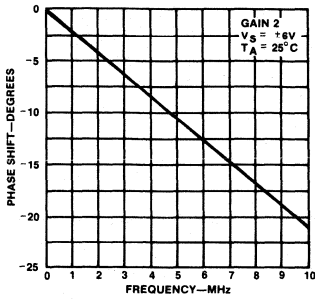


VIDEO AMPLIFIER

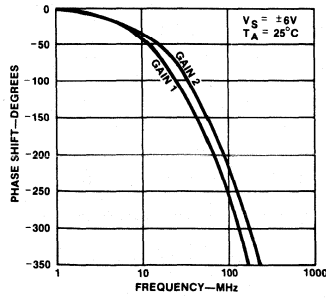
NE/SE592

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

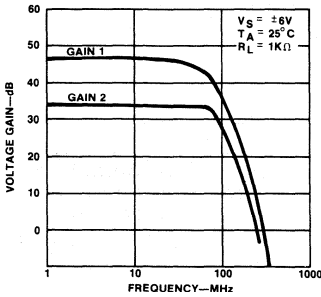
PHASE SHIFT AS A FUNCTION OF FREQUENCY



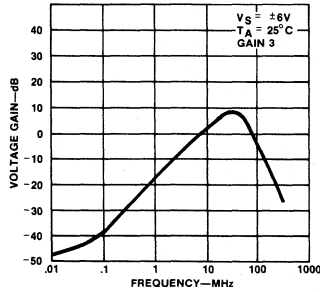
PHASE SHIFT AS A FUNCTION OF FREQUENCY



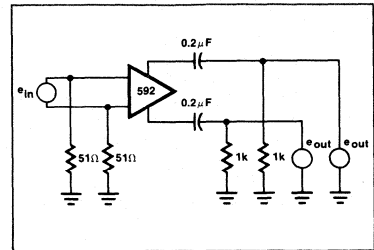
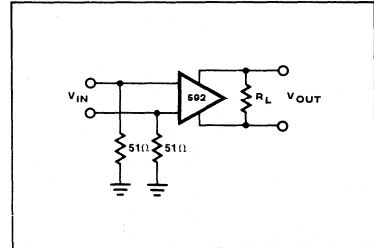
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



VOLTAGE GAIN AS A FUNCTION OF FREQUENCY (ALL GAIN SELECT PINS OPEN)



TEST CIRCUITS $T_A = 25^\circ C$ unless otherwise specified



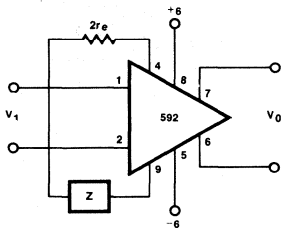
4

VIDEO AMPLIFIER

NE/SE592

TYPICAL APPLICATIONS

FILTER NETWORKS



$$\frac{V_0(s)}{V_1(s)} \approx \frac{1.4 \times 10^4}{Z(s) + 2r_e}$$

$$\approx \frac{1.4 \times 10^4}{Z(s) + 32}$$

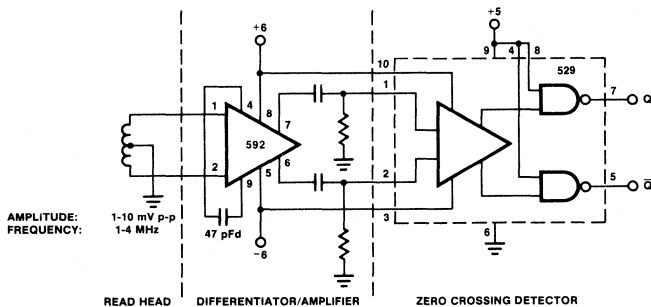
BASIC CONFIGURATION

Z NETWORK	FILTER TYPE	$V_0(s)$ TRANSFER $V_1(s)$ FUNCTION
	LOW PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{1}{s + R/L} \right]$
	HIGH PASS	$\frac{1.4 \times 10^4}{R} \left[\frac{s}{s + 1/RC} \right]$
	BAND PASS	$\frac{1.4 \times 10^4}{L} \left[\frac{s}{s^2 + R/L s + 1/LC} \right]$
	BAND REJECT	$\frac{1.4 \times 10^4}{R} \left[\frac{s^2 + 1/LC}{s^2 + 1/LC + s/RC} \right]$

NOTE

In the networks above, the R value used is assumed to include $2r_e$, or approximately 32Ω.

DISC/TAPE PHASE MODULATED READBACK SYSTEMS



AMPLITUDE:
FREQUENCY:

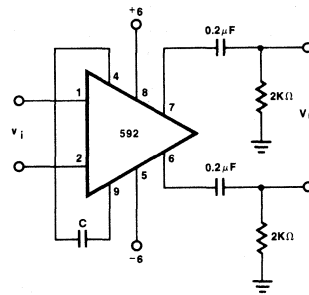
1-10 mV p-p
1-4 MHz

READ HEAD

DIFFERENTIATOR/AMPLIFIER

ZERO CROSSING DETECTOR

DIFFERENTIATION WITH HIGH COMMON MODE NOISE REJECTION



FOR FREQUENCY $F_1 \ll 1/2 \pi (32) C$
 $V_0 \approx 1.4 \times 10^4 C \frac{dV_i}{dT}$

DIFFERENTIAL VIDEO AMPLIFIER

μ A733/733C

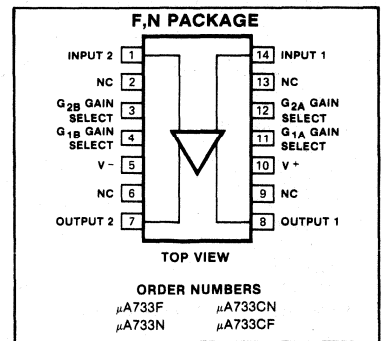
DESCRIPTION

The 733 is a monolithic differential input, differential output, wideband video amplifier. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter follower outputs to the inputs of the second stage. The emitter follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

FEATURES

- 120MHz bandwidth
- 250k Ω input resistance
- Selectable gains of 10, 100 and 400
- No frequency compensation required
- Mil std 883A,B,C available

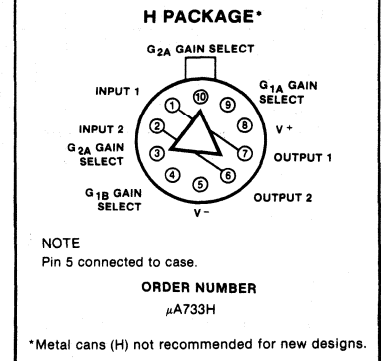
PIN CONFIGURATION



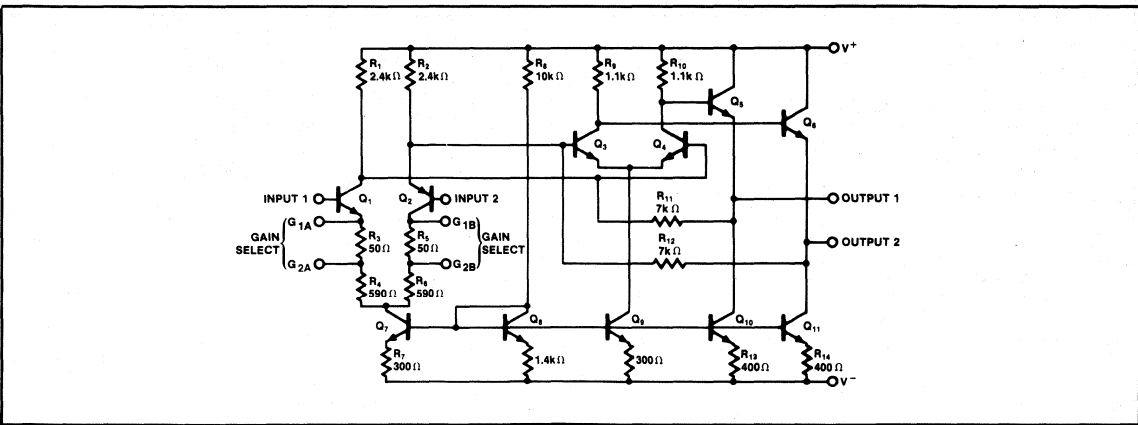
4

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Differential input Voltage	± 5	V
Common mode input Voltage	± 6	V
V _{CC}	± 8	V
Output current	10	mA
Junction temperature	+150	$^{\circ}$ C
Storage temperature range	-65 to +150	$^{\circ}$ C
Operation temperature range		
μA733C	0 to +75	$^{\circ}$ C
μA733	-55 to +125	$^{\circ}$ C
P _D Power dissipation		mW
K package	500	mW
N, F package	670	mW



CIRCUIT SCHEMATIC



DIFFERENTIAL VIDEO AMPLIFIER

 μ A733/733C
DC ELECTRICAL CHARACTERISTICS $T_A = +25^\circ\text{C}$, $V_S = \pm V$, $V_{CM} = 0$ unless otherwise specified.
 Recommended operating supply voltages $V_S = \pm 6.0V$.

PARAMETER	TEST CONDITIONS	μ A733C			μ A733			UNITS
		Min	Typ	Max	Min	Typ	Max	
Differential voltage gain	$R_I = 2k\Omega$, $V_{OUT} = 3V_{p-p}$							
Gain 1 ¹		250	400	600	300	400	500	V/V
Gain 2 ²		80	100	120	90	100	110	V/V
Gain 3 ³		8.0	10	12	9.0	10	11	V/V
Bandwidth	$V_{OUT} = 1V_{p-p}$							
Gain 1 ¹			40			40		MHz
Gain 2 ²			90			90		MHz
Gain 3 ³			120			120		MHz
Rise time								
Gain 1 ¹		10.5			10.5		ns	
Gain 2 ²		4.5	12		4.5	10	ns	
Gain 3 ³		2.5			2.5		ns	
Propagation delay	$V_{OUT} = 1V_{p-p}$							
Gain 1 ¹			7.5			7.5		ns
Gain 2 ²			6.0	10		6.0	10	ns
Gain 3 ³			3.6			3.6		ns
Input resistance	Gain 2	10	Gain 1 ¹	4.0	20	Gain 1 ¹	4.0	k Ω
Gain 2 ²			30	Gain 2 ²		30	k Ω	
Gain 3 ³			250	Gain 3 ³		250	k Ω	
Input capacitance ²	BW = 1kHz to 10MHz	± 1.0	Gain 2	2.0	± 1.0	Gain 2	2.0	pF
Input offset current			0.4	5.0		0.4	3.0	μ A
Input bias current			9.0	30		9.0	20	μ A
Input noise voltage			12			12		μ Vrms
Input voltage range								V
Common mode	VCM = $\pm V$, $f \leq 100\text{kHz}$ VCM = $\pm 1V$, $F = 5\text{MHz}$	60	Rejection ratio	Gain 2	60	Rejection ratio	Gain 2	dB
Gain 2			86	Gain 2		86	dB	
Supply voltage			60	Supply voltage		60		
Rejection ratio	$\Delta V_S = \pm 0.5V$	50	Gain 2	70	50	Gain 2	70	dB
Gain 2								
Output offset voltage	$R_L = \infty$	2.4	Gain 1 ¹	0.6	2.4	Gain 1 ¹	0.6	V
Gain 2 and 3 ^{2,3}			0.35	1.5		0.35	1.5	V
Output common mode voltage	$R_L = \infty$	3.0	2.9	3.4	3.0	2.9	3.4	V
Output voltage swing, differential	$R_L = 2k$	3.0	4.0		3.0	4.0		
Output sink current		2.5	3.6		2.5	3.6		mA
Output resistance			20			20		Ω
Power supply current	$R_L \pm \infty$		18	24		18	24	mA

NOTES

- Gain select pins G_{1A} and G_{1B} connected together.
- Gain select pins G_{2A} and G_{2B} connected together.
- All gain select pins open.

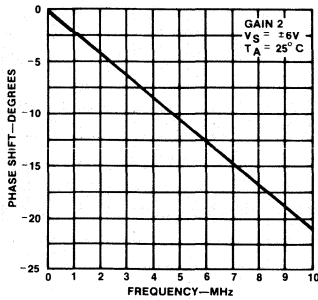
DIFFERENTIAL VIDEO AMPLIFIER

μ A733/733C

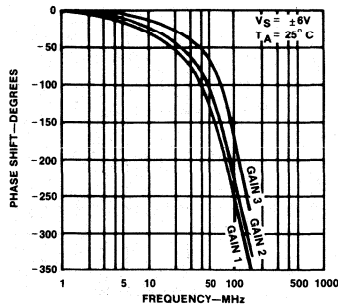
TYPICAL PERFORMANCE CHARACTERISTICS

4

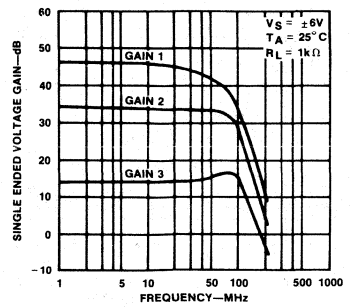
PHASE SHIFT AS A FUNCTION OF FREQUENCY



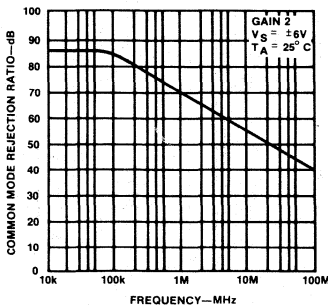
PHASE SHIFT AS A FUNCTION OF FREQUENCY



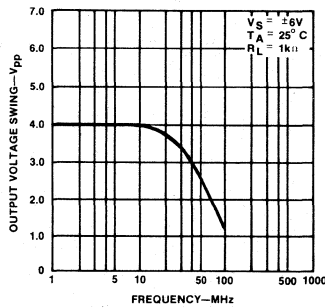
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



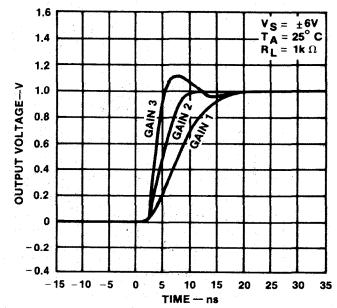
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



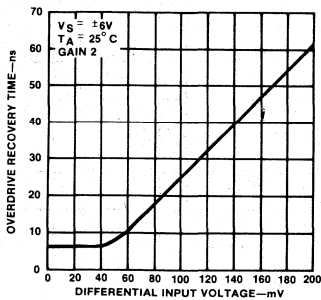
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



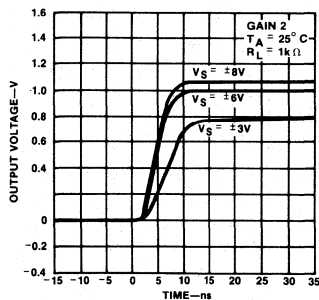
PULSE RESPONSE



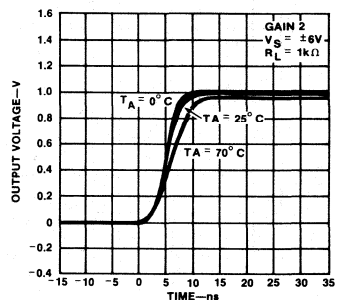
DIFFERENTIAL OVERDRIVE RECOVERY TIME



PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



PULSE RESPONSE AS A FUNCTION OF TEMPERATURE

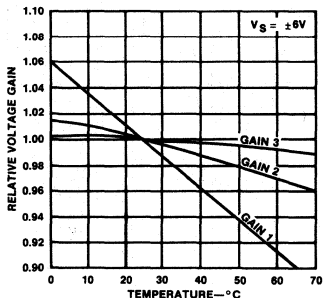


DIFFERENTIAL VIDEO AMPLIFIER

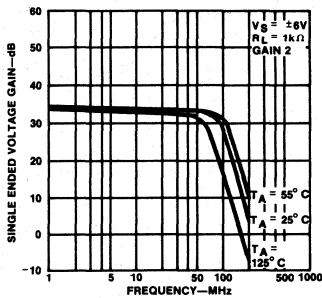
μ A733/733C

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

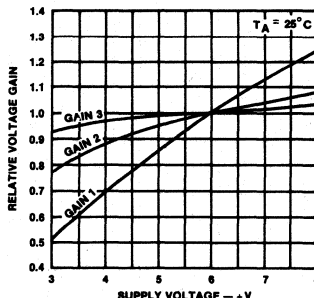
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



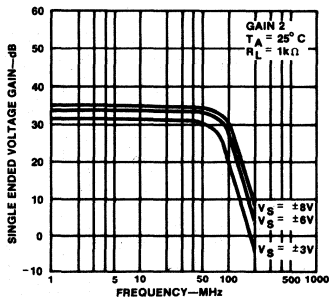
GAIN vs FREQUENCY AS A FUNCTION OF TEMPERATURE



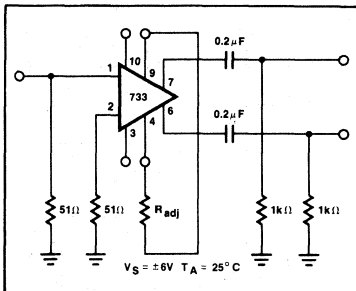
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



GAIN vs FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

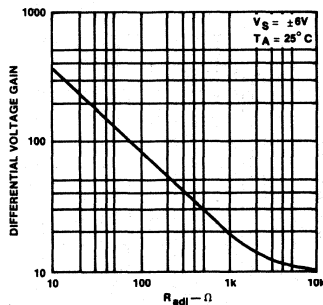


VOLTAGE GAIN ADJUST CIRCUIT

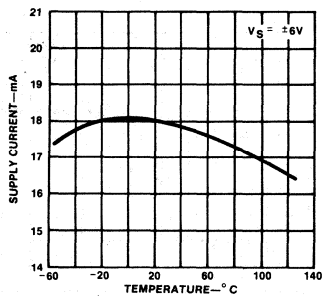


(Pin numbers apply to K Package)

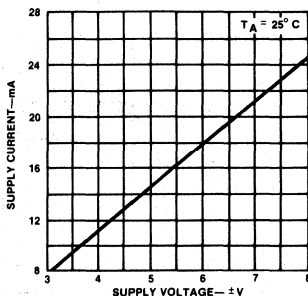
VOLTAGE GAIN AS A FUNCTION OF RADJ (FIGURE 3)



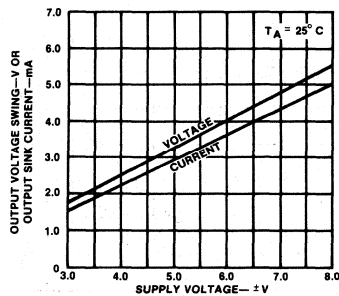
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



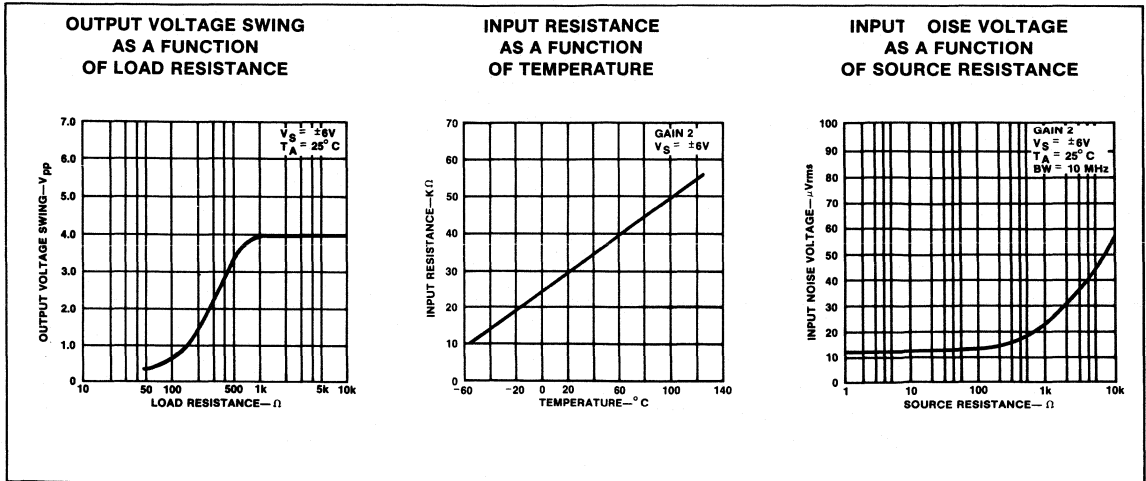
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



DIFFERENTIAL VIDEO AMPLIFIER

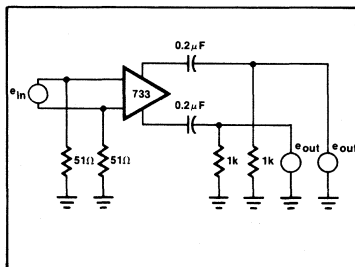
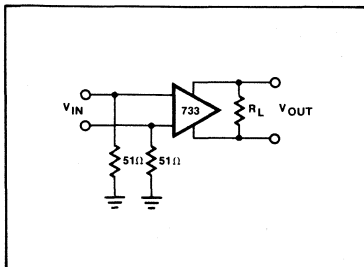
μ A733/733C

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



4

TEST CIRCUITS $T_A = 25^\circ\text{C}$ unless otherwise specified.



Section 5 Timers

INDEX

Section 5 — Timers

Index	5-1
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NE/SE555/SE555C Timer	5-3
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NE/SA/SE558 Quad Timer	5-12

TIMER

NE/SE555/SE555C

DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

FEATURES

- Turn off time less than 2 μ s
- Maximum operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per $^{\circ}$ C

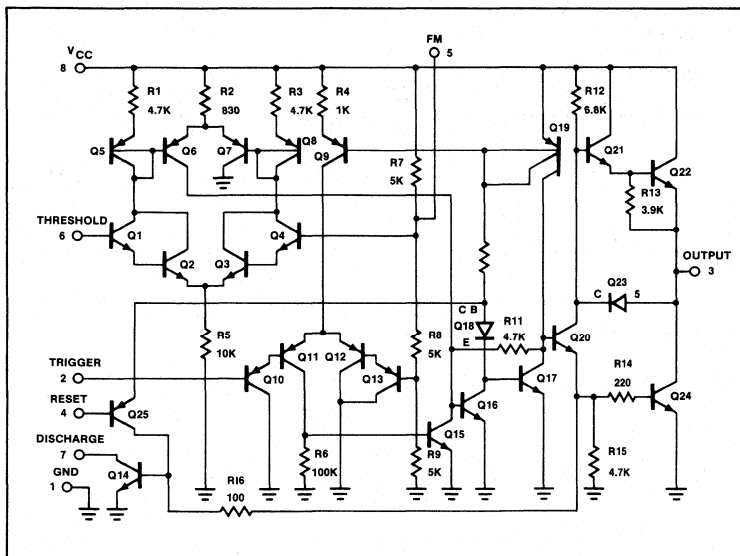
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

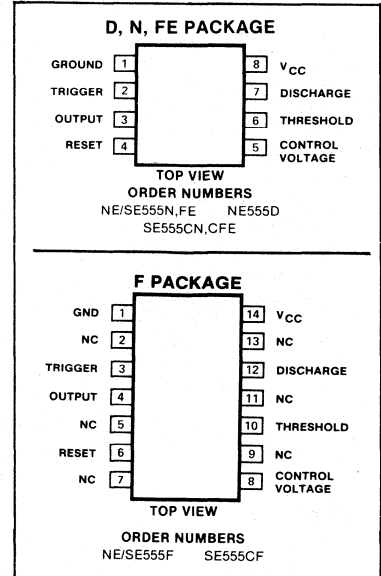
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE555	+18	V
NE555, SE555C,	+16	V
Power dissipation	600	mW
Operating temperature range		
NE555	0 to +70	$^{\circ}$ C
SE555, SE555C	-55 to +125	$^{\circ}$ C
Storage temperature range	-65 to +150	$^{\circ}$ C
Lead temperature (soldering, 60sec)	300	$^{\circ}$ C

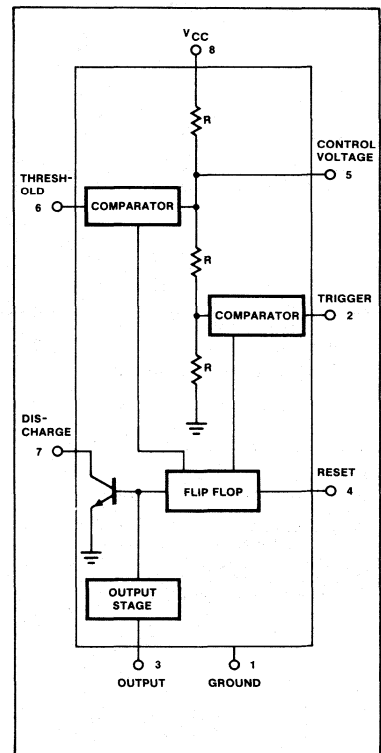
EQUIVALENT SCHEMATIC



PIN CONFIGURATIONS



BLOCK DIAGRAM



5

TIMER

NE/SE555/SE555C

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state) ¹	$V_{CC} = 5\text{V}$ $R_L = \infty$ $V_{CC} = 15\text{V}$ $R_L = \infty$		3 10	5 12		3 10	6 15	mA mA
Timing error (monostable) Initial accuracy ² Drift with temperature Drift with supply voltage	$R_A = 2\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$		0.5 30 0.05	2.0 100 0.2		1.0 50 0.1	3.0 3.0 0.5	% ppm/ $^\circ\text{C}$ %/V
Timing error (astable) Initial accuracy ² Drift with temperature Drift with supply voltage	$R_A, R_B = 1\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$ $V_{CC} = 15\text{V}$		1.5 90 0.15			2.25 150 0.3		% ppm/ $^\circ\text{C}$ %/V
Control voltage level	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	V V
Threshold voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V
Threshold current ³			0.1	0.25		0.1	0.25	μA
Trigger voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	V V
Trigger current	$V_{TRIG} = 0\text{V}$		0.5	0.9		0.5	2.0	μA
Reset voltage ⁴		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.4	mA
Reset current	$V_{RESET} = 0\text{V}$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15\text{V}$ $I_{SINK} = 10\text{mA}$ $I_{SINK} = 50\text{mA}$ $I_{SINK} = 100\text{mA}$ $I_{SINK} = 200\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SINK} = 8\text{mA}$ $I_{SINK} = 5\text{mA}$		0.1 0.4 2.0 2.5	0.15 0.5 2.2		0.1 0.4 2.0 2.5	0.25 0.75 2.5	V V V V
Output voltage (high)	$V_{CC} = 15\text{V}$ $I_{SOURCE} = 200\text{mA}$ $I_{SOURCE} = 100\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SOURCE} = 100\text{mA}$	13.0 3.0	12.5 3.3		12.75 2.75	12.5 3.3		V V V
Turn off time ⁵	$V_{RESET} = V_{CC}$		0.5	2.0		0.5		μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	na

NOTES

- Supply current when output high typically 1mA less.
- Tested at $V_{CC} = 5\text{V}$ and $V_{CC} = 15\text{V}$.
- This will determine the maximum value of $R_A + R_B$, for 15V operation, the max total $R = 10$ megohm, and for 5V operation, the max total $R = 3.4$ megohm.
- Specified with trigger input high.
- Time measured from a positive going input pulse from 0 to $0.8 \times V_{CC}$ into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

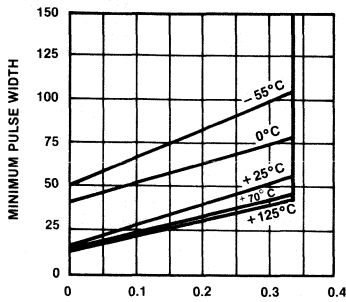
TIMER

NE/SE555/SE555C

TYPICAL PERFORMANCE CHARACTERISTICS

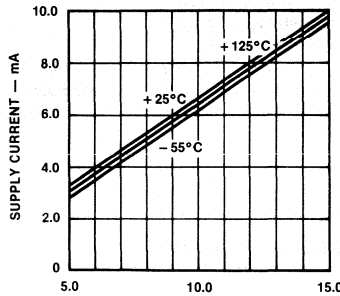
5

**MINIMUM PULSE WIDTH
REQUIRED FOR TRIGGERING**



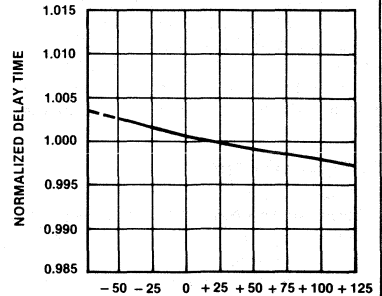
LOWEST VOLTAGE LEVEL OF TRIGGER PULSE

**SUPPLY CURRENT
vs SUPPLY VOLTAGE**



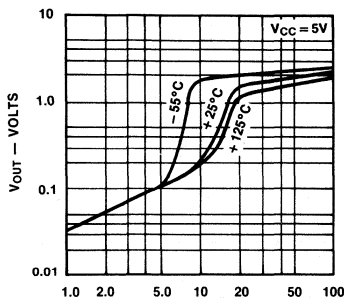
SUPPLY VOLTAGE — VOLTS

**DELAY TIME
vs TEMPERATURE**



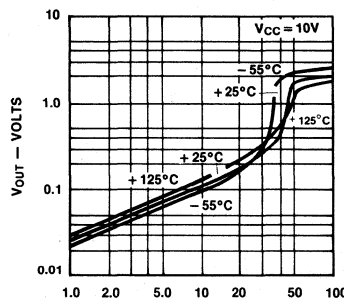
TEMPERATURE — °C

**LOW OUTPUT VOLTAGE
vs OUTPUT SINK CURRENT**



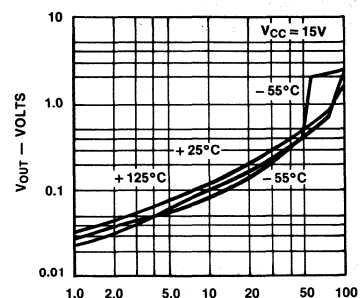
I_{SINK} — mA

**LOW OUTPUT VOLTAGE
vs OUTPUT SINK CURRENT**



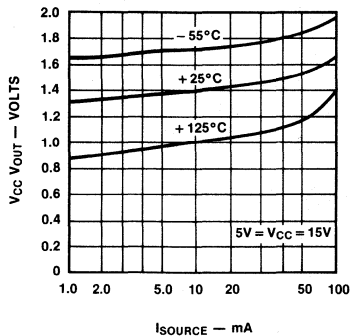
I_{SINK} — mA

**LOW OUTPUT VOLTAGE
vs OUTPUT SINK CURRENT**



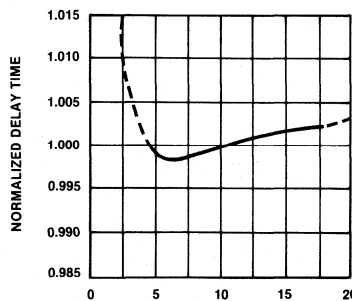
I_{SINK} — mA

**HIGH OUTPUT VOLTAGE DROP
vs OUTPUT SOURCE CURRENT**



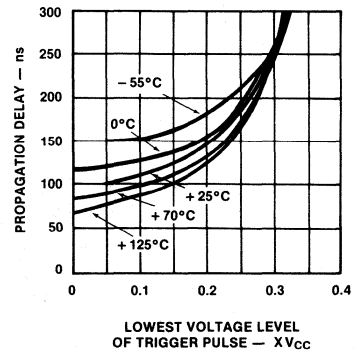
I_{SOURCE} — mA

**DELAY TIME vs
SUPPLY VOLTAGE**



SUPPLY VOLTAGE — V

**PROPAGATION DELAY
vs VOLTAGE LEVEL
OF TRIGGER PULSE**



LOWEST VOLTAGE LEVEL
OF TRIGGER PULSE — X V_{CC}

DUAL TIMER

NE/SA/SE556

DESCRIPTION

The 556 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

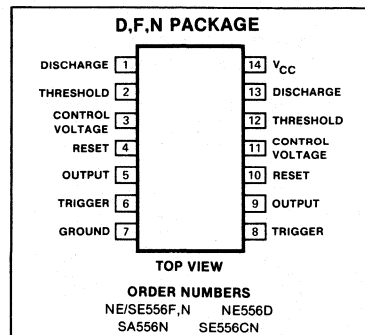
APPLICATIONS

- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch tone encoder

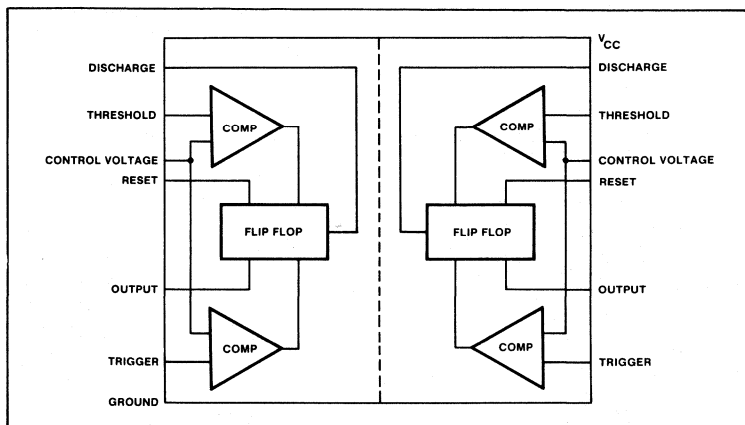
FEATURES

- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C
- SE566 MIL STD 883A, B, C available, N38510 (JAN planned, 38510 processing available).

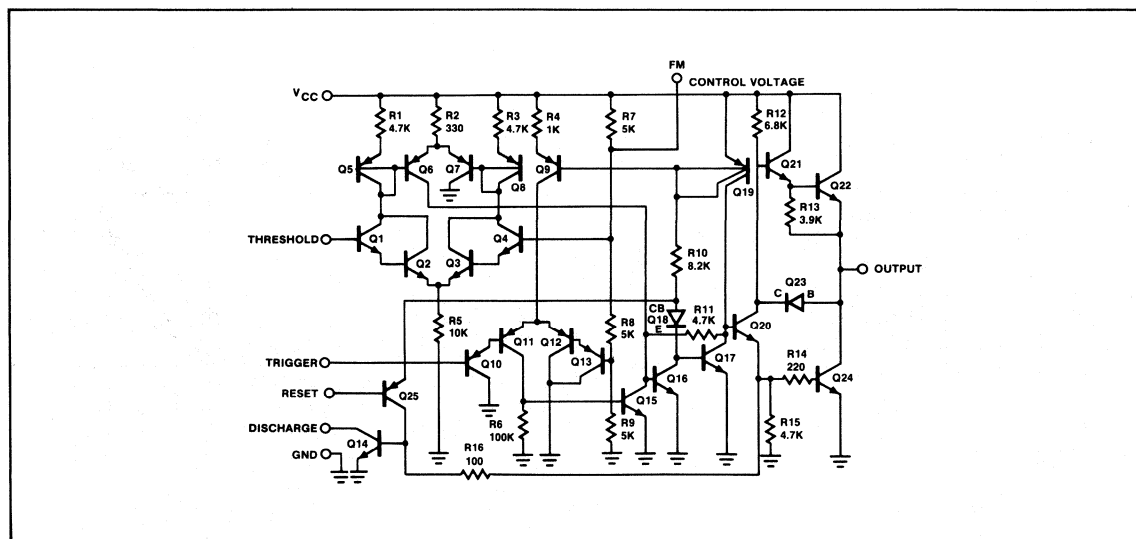
PIN CONFIGURATION



BLOCK DIAGRAM



EQUIVALENT SCHEMATIC (Shown for one circuit only)



DUAL TIMER

NE/SA/SE556

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
NE/SA556, SE556C	+16	V
SE556	+18	V
Power dissipation	600	mW
Operating temperature range		
NE556	0 to +70	°C
SA556	-40 to +85	°C
SE556, SE556C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature	+300	°C
(Soldering, 60 sec)		

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE556			NE/SA556/SE556C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state) ¹	$V_{CC} = 5\text{V}$ $R_L = \infty$ $V_{CC} = 15\text{V}$ $R_L = \infty$		6 20	10 24		6 20	12 30	mA mA
Timing error (monostable)	$R_A = 2\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$							
Initial accuracy ²			0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	$R_A, R_B = 1\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$ $V_{CC} = 15\text{V}$							
Initial accuracy ²			1.5			2.25		%
Drift with temperature			90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	V V
Threshold voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V
Threshold current ³			30	250		30	250	nA
Trigger voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	V V
Trigger current	$V_{TRIG} = 0\text{V}$		0.5	0.9		0.5	2.0	μA
Reset voltage ⁵		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.6	mA
Reset current	$V_{RESET} = 0\text{V}$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15\text{V}$ $I_{SINK} = 10\text{mA}$ $I_{SINK} = 50\text{mA}$ $I_{SINK} = 100\text{mA}$ $I_{SINK} = 200\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SINK} = 8\text{mA}$ $I_{SINK} = 5\text{mA}$		0.1 0.4 2.0 2.5	0.15 0.5 2.25		0.1 0.4 2.0 2.5	0.25 0.75 3.2	V V V V
Output voltage (high)	$V_{CC} = 15\text{V}$ $I_{SOURCE} = 200\text{mA}$ $I_{SOURCE} = 100\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SOURCE} = 100\text{mA}$	13.0	12.5 13.3		12.75	12.5 13.3		V V
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics ⁴								
Initial accuracy ²			0.5	1.0		1.0	2.0	%
Drift with temperature			10			10		ppm/°C
Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

NOTES See following page

5

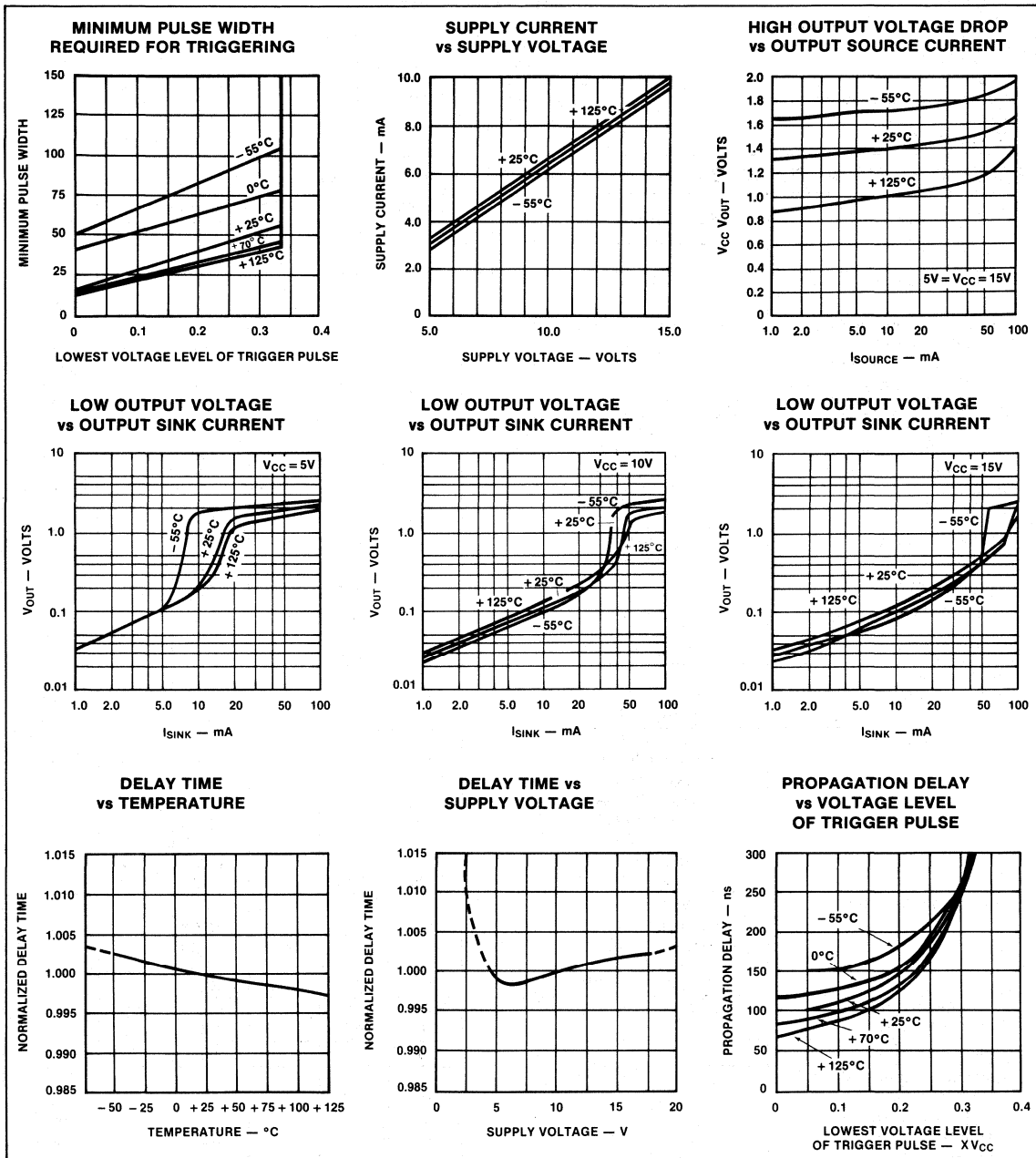
DUAL TIMER

NE/SA/SE556

NOTES

- Supply current when output is high is typically 1.0mA less.
- Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
- This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total $R = 10$ meg-ohms, and for 5V operation, the max. total $R = 3.4$ meg-ohms.
- Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
- Specified with trigger input high.

TYPICAL PERFORMANCE CHARACTERISTICS



DUAL TIMER

NE/SA/SE556-1/SE556-1C

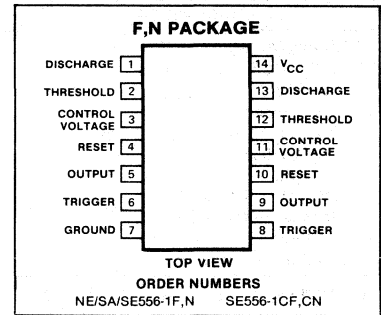
DESCRIPTION

The 556-1 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556-1 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200mA.

FEATURES

- Turn off time less than $2\mu S$
- Maximum operating frequency greater than 500kHz
- Timing from microseconds to hours
- Replaces two 555 timers
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per $^{\circ}C$

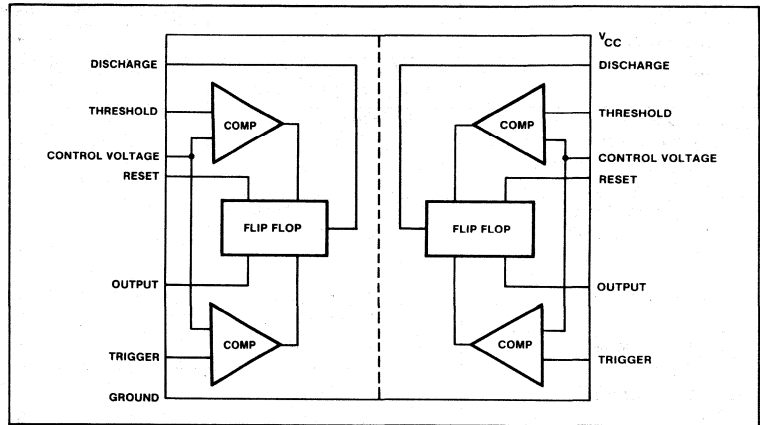
PIN CONFIGURATION



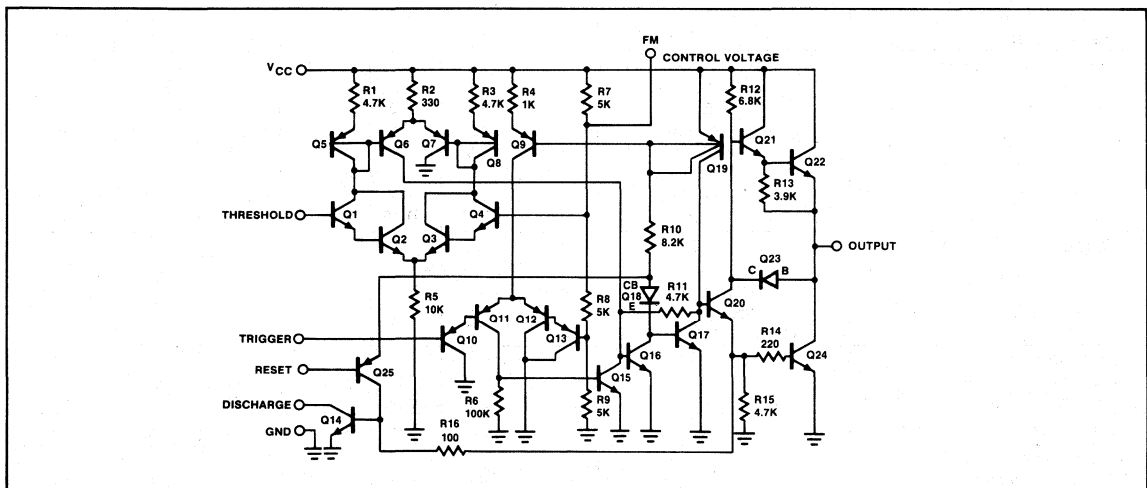
APPLICATIONS

- Precision timing
- Sequential timing
- Pulse shaping
- Pulse generator
- Missing pulse detector
- Tone burst generator
- Pulse width modulation
- Time delay generator
- Frequency division
- Industrial controls
- Pulse position modulation
- Appliance timing
- Traffic light control
- Touch tone encoder

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC (Shown for one circuit only)



DUAL TIMER

NE/SA/SE556-1/SE556-1C

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
NE/SA556-1, SE556-1C	+16	V
SE556-1	+18	V
Power dissipation	1.20	W
Operating temperature range		
NE/SA556-1	0 to +70	°C
SA556-1	-40 to +85	°C
SE556-1, SE556-1C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE556-1			NE556-1/SE556-1C			UNITS
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current (low state) ¹	$V_{CC} = 5\text{V}$ $R_L = \infty$ $V_{CC} = 15\text{V}$ $R_L = \infty$		6 20	10 24		6 20	12 30	mA mA
Timing error (monostable)	$R_A = 2\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$							
Initial accuracy ²			0.5	1.5		0.75	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	$R_A, R_B = 1\text{k}\Omega$ to $100\text{k}\Omega$ $C = 0.1\mu\text{F}$ $V_{CC} = 15\text{V}$							
Initial accuracy ²			1.5			2.25		%
Drift with temperature			90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9.6 2.9	10.0 3.33	10.4 3.8	9.0 2.6	10.0 3.33	11.0 4.0	V V
Threshold voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	9.4 2.7	10.0 3.33	10.6 4.0	8.8 2.4	10.0 3.33	11.2 4.2	V V
Threshold current ³			30	250		30	250	nA
Trigger voltage	$V_{CC} = 15\text{V}$ $V_{CC} = 5\text{V}$	4.8 1.45	5.0 1.67	5.2 1.9	4.5 1.1	5.0 1.67	5.6 2.2	V V
Trigger current	$V_{TRIG} = 0\text{V}$		0.5	0.9		0.5	2.0	μA
Reset voltage ⁵		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.6	mA
Reset current	$V_{RESET} = 0\text{V}$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15\text{V}$ $I_{SINK} = 10\text{mA}$ $I_{SINK} = 50\text{mA}$ $I_{SINK} = 100\text{mA}$ $I_{SINK} = 200\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SINK} = 8\text{mA}$ $I_{SINK} = 5\text{mA}$		0.1 0.4 0.8 2.5	0.15 0.5 1.2		0.1 0.4 2.0 2.5	0.25 0.75 2.5 V	V V V V V V V
Output voltage (high)	$V_{CC} = 15\text{V}$ $I_{SOURCE} = 200\text{mA}$ $I_{SOURCE} = 100\text{mA}$ $V_{CC} = 5\text{V}$ $I_{SOURCE} = 100\text{mA}$	13.0 3.0	12.5 13.3 3.3		12.75 2.75	12.5 13.3 3.3		V V V
Turn off time ⁶	$V_{RESET} = V_{CC}$		0.5	2.0		0.5		μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	nA
Matching characteristics ⁴								
Initial accuracy ²			0.5	1.0		1.0	2.0	%
Drift with temperature			± 10			± 10		ppm/°C
Drift with supply voltage			0.1	0.2		0.2	0.5	%/V

NOTES

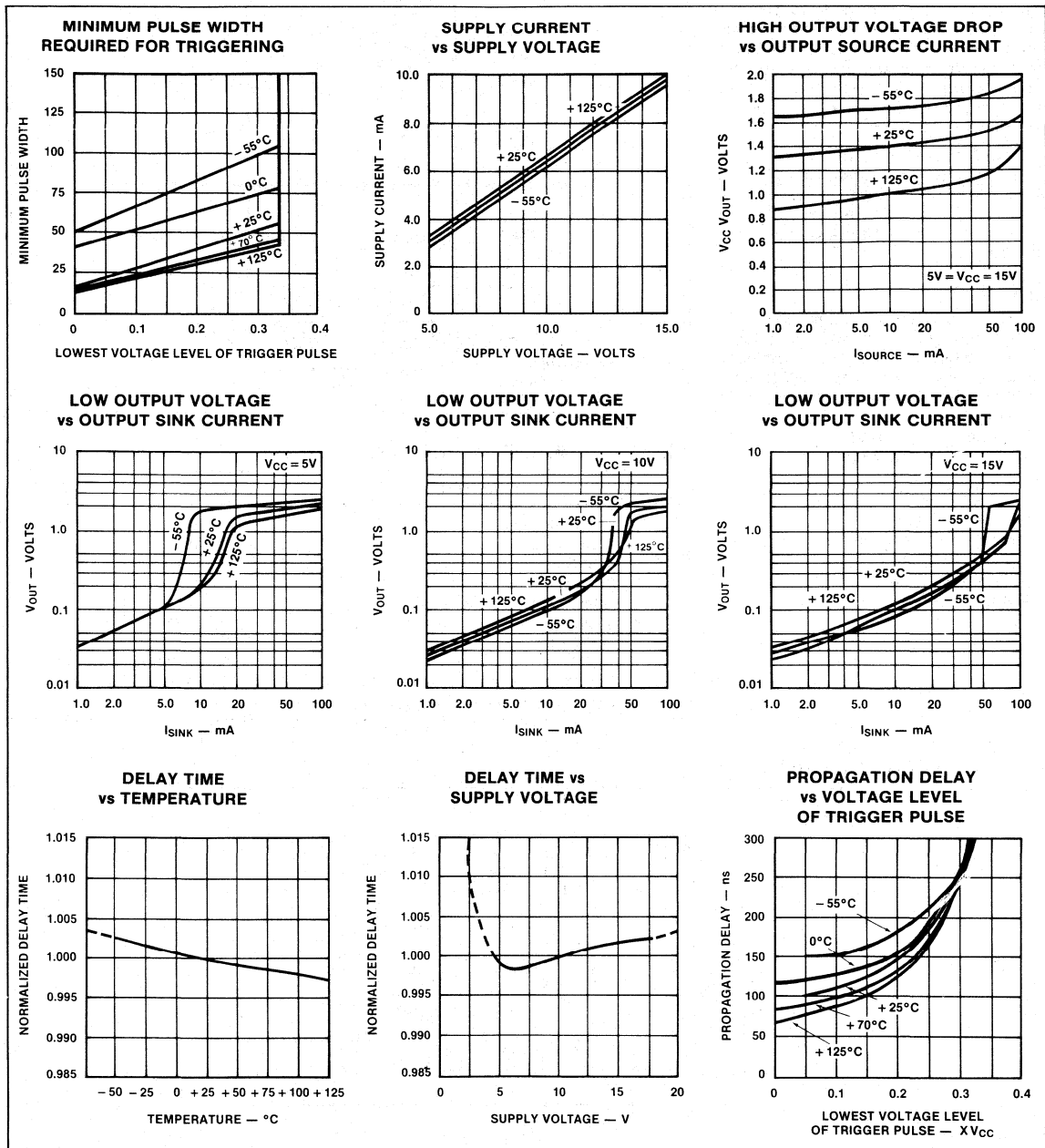
See following page

DUAL TIMER

NE/SA/SE556-1/SE556-1C

- NOTES**
- Supply current when output is high is typically 1.0mA less.
 - Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
 - This will determine the maximum value of $R_A + R_B$. For 15V operation, the maximum total $R = 10$ megohms, and for 5V operation, the max. total $R = 3.4$ megohms.
 - Matching characteristics refer to the difference between performance characteristics for each timer section in the monostable mode.
 - Specified with trigger input high.
 - Time measured from a positive going input pulse from 0 to $0.8 V_{CC}$ into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL CHARACTERISTICS



QUAD TIMER

NE/SA/SE558

DESCRIPTION

The 558 Quad Timers are monolithic timing devices which can be used to produce four entirely independent timing functions. The 558 output sinks current. These highly stable, general purpose controllers can be used in a monostable mode to produce accurate time delays, from microseconds to hours. In the time delay mode of operation, the time is precisely controlled by one external resistor and one capacitor. A stable operation can be achieved by using two of the four timer sections.

The four timing sections in the 558 are edge triggered; therefore, when connected in tandem for sequential timing applications, no coupling capacitors are required. Output current capability of 100mA is provided in both devices.

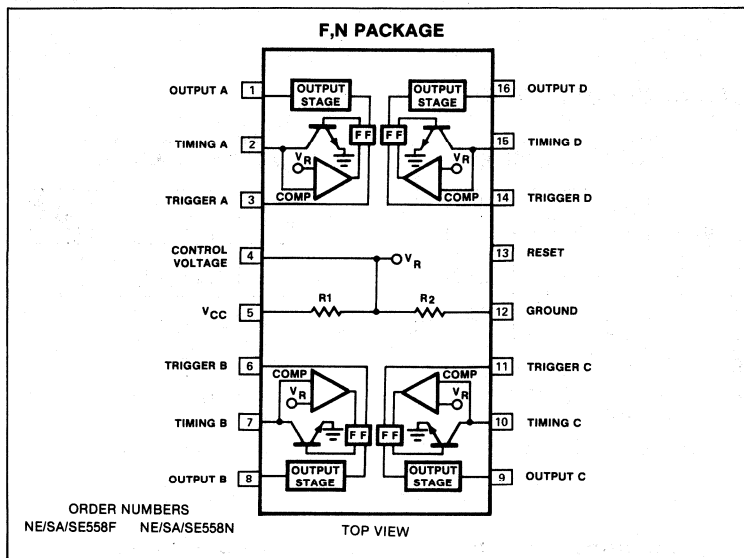
FEATURES

- 100mA output current per section
- Edge triggered (no coupling capacitor)
- Output independent of trigger conditions
- Wide supply voltage range 4.5V to 18V
- Timer intervals from microseconds to hours
- Time period equals RC
- Military qualifications pending

APPLICATIONS

- Sequential timing
- Time delay generation
- Precision timing
- Industrial controls
- Quad one-shot

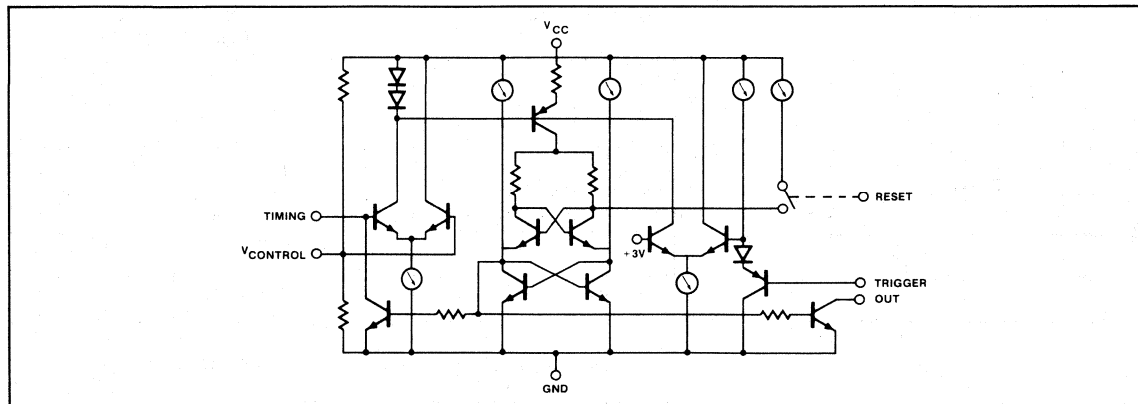
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
NE/SA558	+16	V
SE558	+18	V
Power dissipation	1.25	W
Operating temperature range		
NE558	0 to +70	°C
SA558	-40 to +85	°C
SE558	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

558 EQUIVALENT CIRCUIT



QUAD TIMER

NE/SA/SE558

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = +5\text{V}$ to $+15\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE558			NE/SA558			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage		4.5		18	4.5		16	V
Supply current	$V_{CC} = \text{Reset} = 15\text{V}$		21	32		27	36	mA
Timing accuracy (T = RC)	$R = 2\text{k}\Omega$ to $100\text{k}\Omega$ $C = 1\mu\text{F}$							
Initial accuracy			1.0	3		2		%
Drift with temperature			150			150		ppm/ $^\circ\text{C}$
Drift with supply voltage			0.1			0.1		%/V
Trigger voltage ¹	$V_{CC} = 15\text{V}$	0.8	1.5	2.4	0.8	1.5	2.4	V
Trigger current	Trigger = 0V		5	30		5	100	μA
Reset voltage ²		0.8	1.5	2.4	0.8	1.5	2.4	V
Reset current	Reset		50	300		50		μA
Threshold voltage			0.63			0.63		$\times V_{CC}$
Threshold leakage			15			15		nA
Output voltage ³	$I_L = 10\text{mA}$		0.1	0.2		0.1	0.4	V
	$I_L = 100\text{mA}$		0.7	1.5		1.0	2.0	V
Output leakage			10			10		nA
Propagation delay			1.0			1.0		μs
Risetime of output	$I_L = 100\text{mA}$		100			100		ns
Falltime of output	$I_L = 100\text{mA}$		100			100		ns

NOTES

1. The trigger functions only on the falling edge of the trigger pulse only after previously being high. After reset the trigger must be brought high and then low to implement triggering.
2. For reset below 0.8 volts, outputs set low and trigger inhibited. For reset above 2.4 volts, trigger enabled.
3. The 558 output structure is open collector which requires a pull up resistor to V_{CC} to sink current. The output is normally low sinking current.

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Section 6 Power Controllers

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Section 6 — Power Controllers

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VOLTAGE REGULATOR—SYMBOLS AND DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low

1 is logic level high

X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} (-V_{CC})

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Line Regulation

Sometimes referred to as "static regulation". This term refers to the changes in the output as the input is varied slowly from its rated minimum value to its rated maximum value (from 105 V_{ACRMS} to 125 V_{ACRMS}). Measured in mv/V.

Load Regulation

Sometimes referred to as "dynamic regulation". This term refers to the changes in the output when load conditions are suddenly changed (from no load to full load). Measured in mv/V.

Thermal Regulation

Referred to as changes due to ambient variations or thermal drift. Also referred to as temperature coefficient, measured in ppm/°C or mv/°C.

Transient Response

The ability of a regulator to respond to rapid changes in line variations, load variations, or intermittent transient input conditions. (Transient Response is often referred to as "recovery time"). Measured in milliseconds (ms).

Voltage Limiting

The ability of the regulator to "shut down" in the event that the internal reference sources fail to function properly. Measured in Volts.

Current Limiting

The ability of the amplified segment to limit the output current of the device when safe operating limits are exceeded. Measured in amperes (pre-determined).

Thermal Shutdown

The ability of the regulator to shut itself down when the maximum die temperature is exceeded. Measured in degrees Celsius (C).

Power Dissipation

The ability of the regulator to tolerate excessively high levels of input power while maintaining its operation within the safe operating area of its active devices. Measured in watts.

Efficiency

Regarding a regulator, the ratio of the total power input to the usable power output. Expressed as a percentage. (For example, if a regulator has a 50 watt input and a 40 watt output, its efficiency is 80 percent).

EMI/RFI

("Electromagnetic Interference/Radio Frequency Interference") regarding regulators, magnetic field disturbance and radio frequency interference signals generated especially by SMPS devices. Measurement is generally unspecified.

Safe Operating Area Restriction (SOAR)

Limits the output current of the amplifier to maintain safe (no thermal runaway) operating conditions. (Accomplished through internal sensor amplifiers).

NOTE

Refer to Section 4 of Analog Applications Manual for an in-depth explanation of Voltage Regulators

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT

NE/SE5560

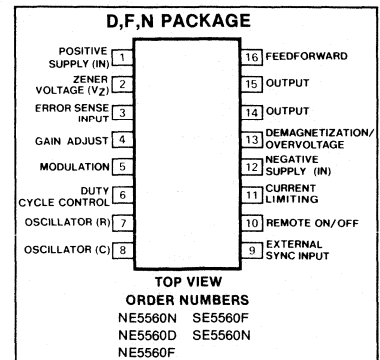
DESCRIPTION

The NE/SE5560 is a control circuit for use in switched mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched mode power supplies, including an internal temperature compensated reference source, internal Zener reference, sawtooth generator, pulse width modulator, output stage and various protection circuits.

FEATURES

- Stabilized power supply
- Temperature compensated reference source
- Sawtooth generator
- Pulse width modulator
- Remote on/off switching
- Current limiting
- Low supply voltage protection
- Loop fault protection
- Demagnetization/overvoltage protection
- Maximum duty cycle adjustment
- Feed forward control
- External synchronization

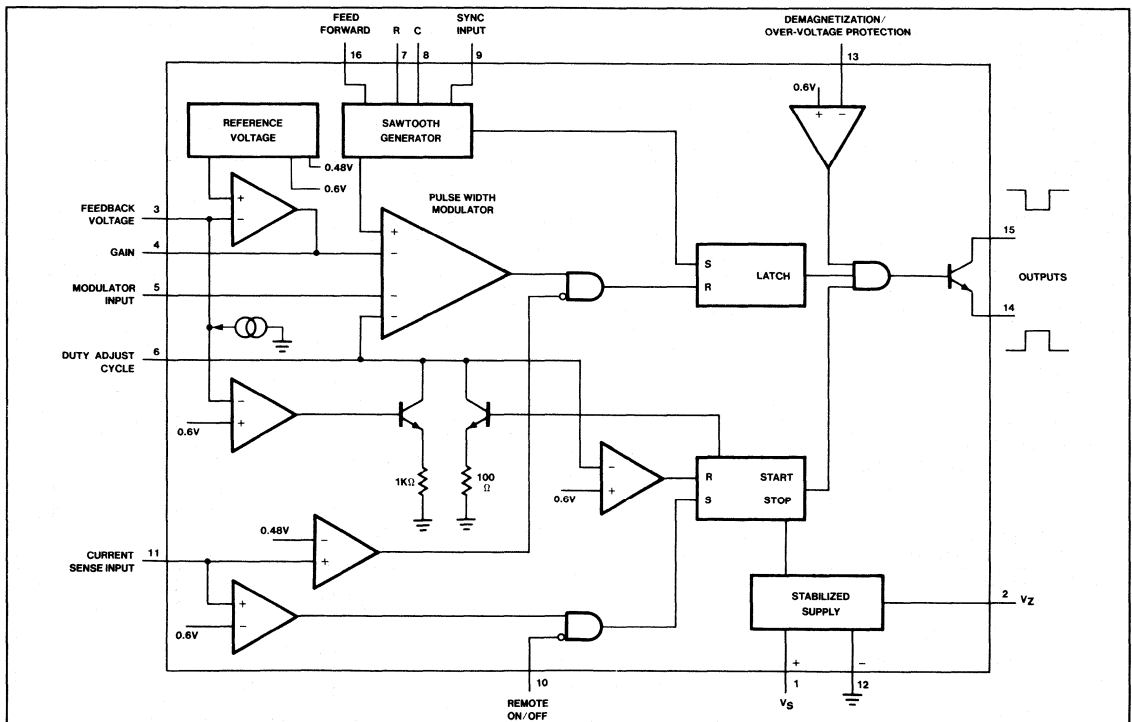
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply		
Voltage sourced	+18	V
Current sourced	30	mA
Output transistor		
Output current	40	mA
Collector voltage (Pin 15)	+18	V
Max. emitter voltage (Pin 14)	+5	V
Operating temperature (ambient)		
SE5560	-55 to +125	°C
NE5560	0 to 70	°C
Storage temperature range	-65 to +150	°C

BLOCK DIAGRAM



SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT

NE/SE5560

DC ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{V}$ unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Sections	Over temp.	3.65		3.85	3.53		4.00	V
Internal reference voltage (V_{ref})	25°C	3.69	3.76	3.81	3.57	3.76	3.95	V
Internal Zener reference (V_Z)	$I_L = 7\text{mA}$	7.8	8.4	9.0	7.8	8.4	9.0	V
Oscillator Section	Over temp.	50		100k	50		100k	Hz
Modulator								
Modulator input current	Voltage at Pin 5 = 1V over temp.		0.2	20		0.2	20	μA
Housekeeping Function	Over temp.		0.2	20		0.2	20	μA
*Pin 6, input current	(for 50% maximum duty cycle) 15kHz to 50kHz/41% of V_Z	40	50	60	40	50	60	% of duty cycle
*Pin 6, duty cycle limit control								V
*Pin 1, low supply voltage protection thresholds		$V_Z + 0.2$	$V_Z + 7\text{V}$	$V_Z + 1.7\text{V}$	$V_Z + 0.2$	$V_Z + 7\text{V}$	$V_Z + 1.7\text{V}$	mV
*Pin 3, feedback loop protection trip threshold		470	600	720	470	600	720	mV
*Pin 3, pull up current	Over temp.	470	-15	-35	470	-15	-35	μA
*Pin 13, demagnetization/over voltage protection trip on threshold			600	720		600	720	mA
*Pin 13, input current	25°C		0.6	10		0.6	10	μA
	Over temp.			20			20	μA
Pin 16, feed forward duty cycle ² control	Voltage at Pin 16 = $2V_Z$		0.4			0.4		original duty cycle
*Pin 16, feed forward input current	25°C		0.2	5		0.2	5	μA
	Over temp.			10			10	μA
External Synchronization								
Pin 9 off		0		0.8	0		0.8	V
on		2		V_Z	2		V_Z	V
sink current	Voltage at Pin 9 = 0V, 25°C							
	Over temp.		-65	-100		-65	-125	μA
				-125			-125	μA
Remote								
*Pin 10 off		0	0.8		0	0.8		V
on		2	V_Z		2	V_Z		V
sink current	25°C		-85	-100		-85	-125	μA
	Over temp.			-125			-125	μA
Current Limiting								
*Pin 11, I_{LN}	Voltage at Pin 11 = 250mV, 25°C		-2	-10		-2	-10	μA
	Over temp.			-20			-	
Trip Levels:								
Shut down, slow start		0.560	0.600	0.700	0.560	0.600	0.700	V
Current limit		0.400	0.48	0.500	0.400	0.48	0.500	V
Error Amplifier								
Output voltage swing (maximum)		6.2			6.2			V
Output voltage swing (minimum)				0.7		0.7		V
Open loop gain			60			60		dB
Feedback resistor		10k		10k				Ω
Small signal bandwidth			3			3		MHz
Output Stage								
$V_{CE(SAT)} I_C = 40\text{mA}$				0.5		0.5		V
Output Current (Pin 15)		40			40			mA
Max emitter voltage (Pin 14)		5	6		5	6		V

SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT

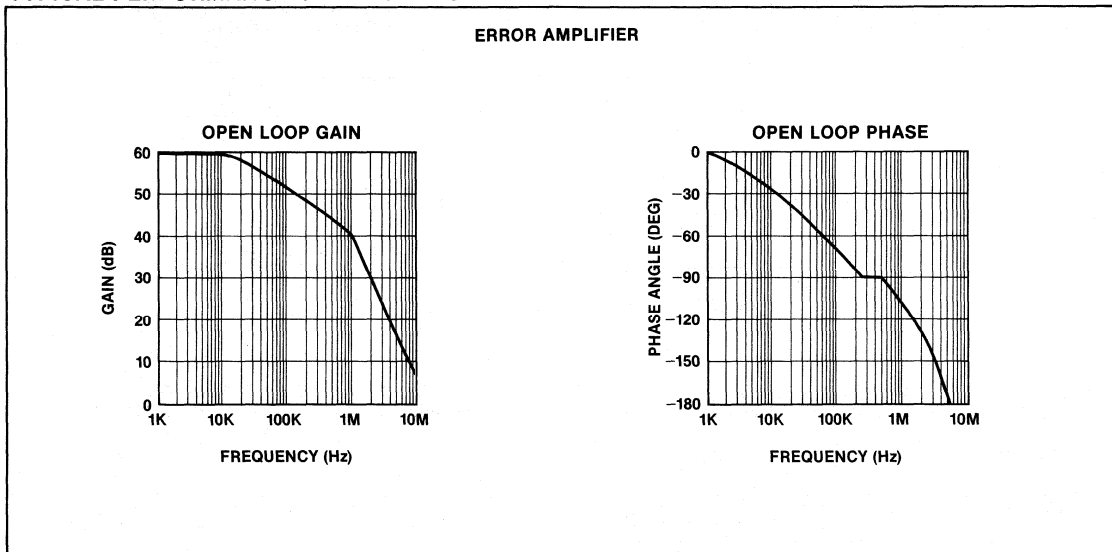
NE/SE5560

DC ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	TEST CONDITIONS	SE5560			NE5560			UNIT
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage/Current I_{CC}	$I_Z = 0$, voltage fed, $V_{CC} = 12V$, $25^\circ C$ Over temp. $I_{CC} = 10mA$, current feed $I_{CC} = 30mA$, current feed			10			10	mA
V_{CC}				15			15	mA
V_{CC}		20		23	19		24	V
Temperature coefficient of V_{ref}		20		30	20		30	V
Temperature coefficient of V_Z			+75			+75		ppm/ $^\circ C$
Initial accuracy	$R = 5k\Omega$		+150			+150		ppm/ $^\circ C$
Duty cycle range ¹	$f_o = 20kHz$	0	5	98	0	5	98	%
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at 40mA I_{OUT}		0.7	0.8		0.7	0.8	μs



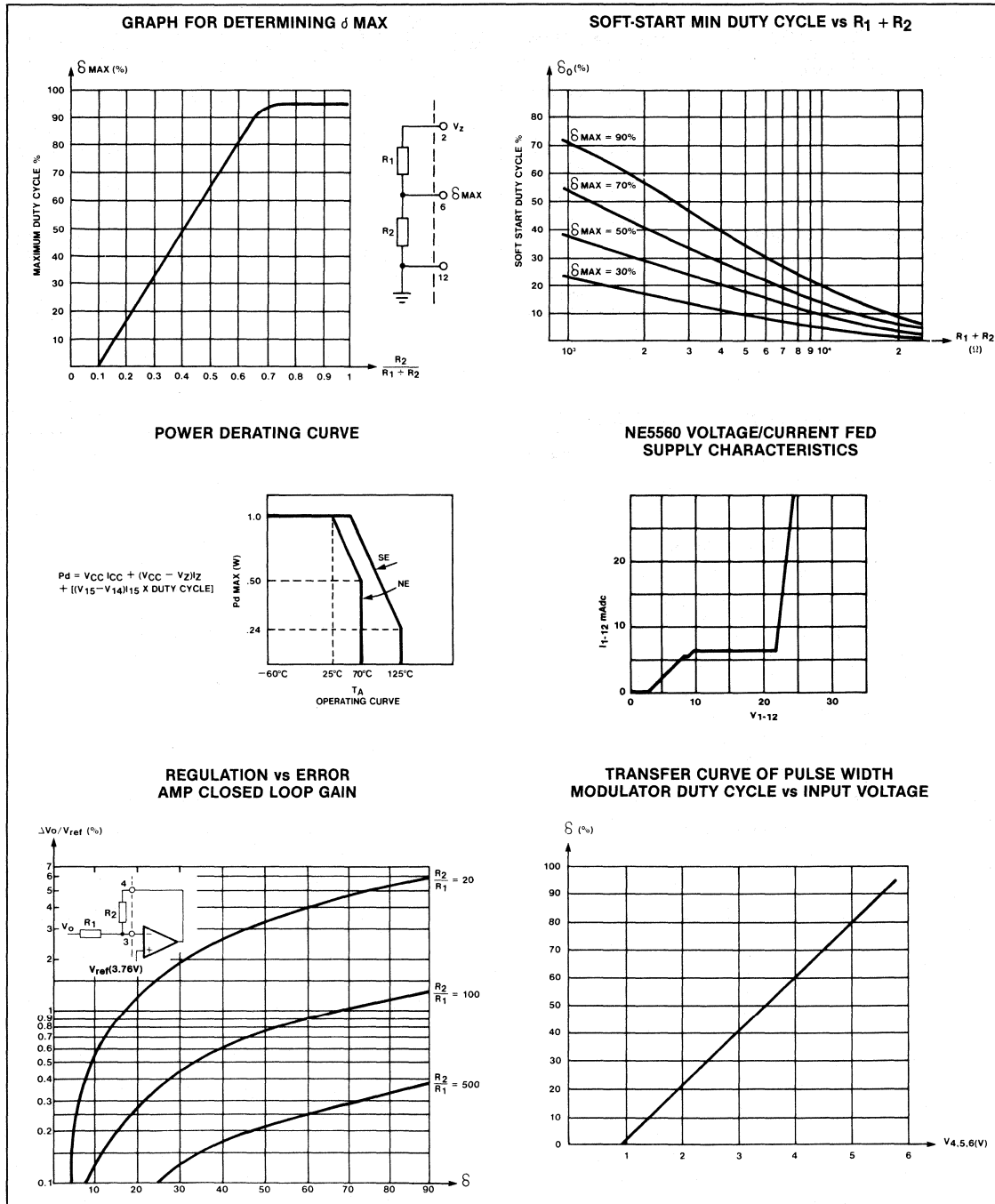
TYPICAL PERFORMANCE CHARACTERISTICS



SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT

NE/SE5560

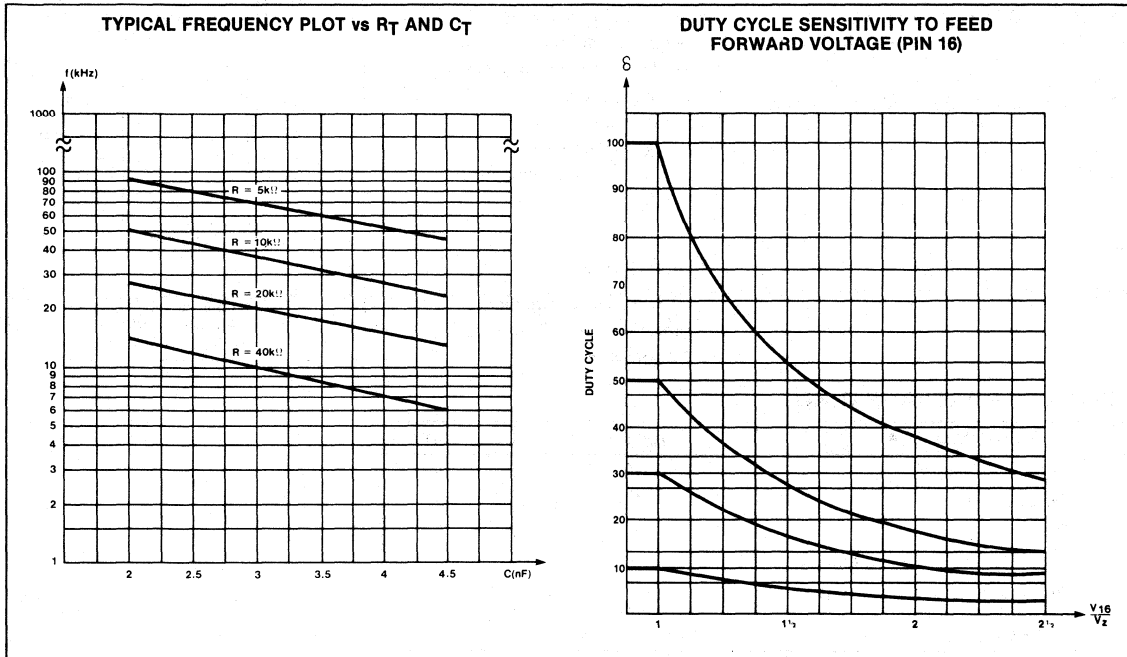
TYPICAL PERFORMANCE CHARACTERISTICS (continued)



SWITCHED-MODE POWER SUPPLY CONTROL CIRCUIT

NE/SE5560

TYPICAL PERFORMANCE CHARACTERISTICS (continued)



6

DESCRIPTION of the NE5560
BLOCK DIAGRAM

The following functions are incorporated:

- A temperature compensated reference source.
- An error amplifier with pin 3 as input. The output is connected to pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (pins 7,8,9).
- A pulse-width modulator with a duty-cycle range from 0 to 95%.

The PWM has two additional inputs:

Pin 6 can be used for a precise setting of δ max.

Pin 5 gives a direct access to the modulator, allowing for real constant current operation:

- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above-mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current

limit circuit, therefore pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.

- A TTL-compatible remote on/off input at pin 10, also operating via the start-stop circuit.
- An inhibit input at pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (pin 15) and the emitter (pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage or current driven (pins 1 and 12). The internally generated stabilized output voltage V_z is connected to pin 2.
- A special function is the so-called feed-forward at pin 16. The amplitude of the sawtooth generator is modulated in such a way that the duty cycle becomes inversely proportional to the voltage on this pin: $\delta \sim C/V_{16}$.
- Loop fault protection circuits assure that the duty-cycle is reduced to zero or a low value for open or short-circuited feedback loops.

Stabilized Power Supply
(Pins 1, 2, 12)

The power supply of the NE5560 is of the well known series regulation type and provides a stabilized output voltage of typically 8.5 volts.

This voltage V_z is also present at pin 2 and can be used for precise setting of δ max. and to supply external circuitry. Its maximum current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage; typical 23V for 10mA and maximum 30V for 30mA.

The low supply voltage protection is active when $V(1-12)$ is below 10.5V and inhibits the output pulse.

When the supply voltage surpasses the 10.5V level, the IC starts delivering output pulses via the slow-start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from V_z and $R(7-12) \geq 20k\Omega$.

SWITCHED MODE POWER SUPPLY CONTROLLER

NE/SE5561

DESCRIPTION

The NE5561/SE5561 is a control circuit for use in switched mode power supplies. It contains an internal temperature compensated supply, PWM, sawtooth oscillator, over-current sense latch, and output stage. The device is intended for low cost SMPS applications where extensive housekeeping functions are not required.

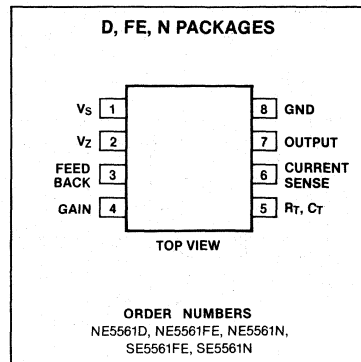
FEATURES

- Micro-miniature (D) package
- Pulse-width modulator
- Current limiting (cycle by cycle)
- Sawtooth generator
- Stabilized power supply
- Double pulse protection
- Internal temperature compensated reference

APPLICATIONS

- Switch mode power supplies
- D/C motor controller inverter
- DC/DC converter

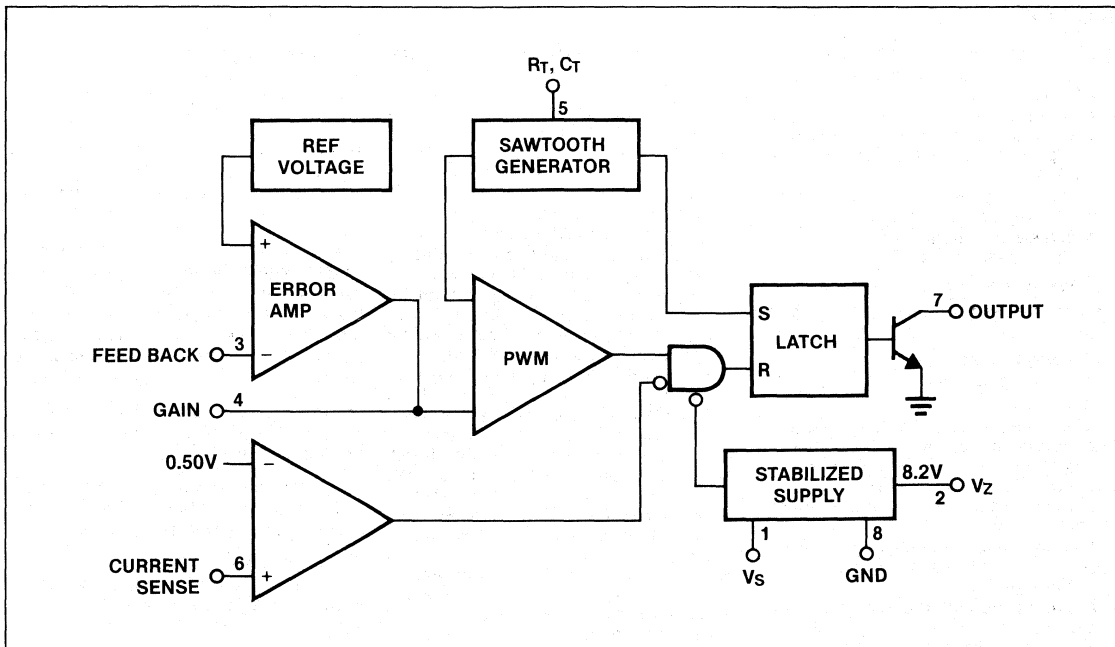
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V_S	18	V
Output Current	40	mA
Output duty cycle	98	%
Max total power dissipation	0.75	W
Operating temperature range		
NE5561	0 to 70	°C
SE5561	-55 to +125	°C

BLOCK DIAGRAM



SWITCHED MODE POWER SUPPLY CONTROLLER

NE/SE5561

DC ELECTRICAL CHARACTERISTICS $V_S = 12V, T_A = 25^\circ C$ unless otherwise specified

SYMBOL AND PARAMETER	TEST CONDITIONS	SE5561			NE5561			UNIT
		Min	Typ	Max	Min	Typ	Max	
OSCILLATOR SECTION: Frequency range	Over temp $f_o = 20kHz$	50		100k	50		100k	Hz
Initial accuracy			12			12		%
Duty cycle range		0		98	0		98	%
REFERENCE SECTION: V_{REF} , Internal ref voltage	Over temp $T_A = 25^\circ C$	3.65		3.88	3.55		3.98	V
		3.69	3.75	3.84	3.57	3.75	3.96	V
V_Z , internal zener ref	$I_L = 7mA$	7.8	8.2	8.8	7.8	8.2	8.8	V
Temp coefficient of V_{REF}			100			100		ppm/ $^\circ C$
Temp coefficient of V_Z			-175			-175		ppm/ $^\circ C$
CURRENT LIMITING (I_{IN})	Pin 6 = 250mV	$T_A = 25^\circ C$		-2		-2		μA
		Over temp			-20		-20	μA
Single pulse inhibit delay	Inhibit delay time for 20% overdrive at	$I_{OUT} = 40mA$		0.7	0.8	0.7	0.8	μs
		$I_{OUT} = 20mA$		0.88	1.10	0.88	1.10	μs
Current limit trip level		.400	.500	.600	.400	.500	.600	V
ERROR AMPLIFIER: Open loop gain			60			60		dB
Feedback resistor		10k			10k			Ω
Small signal bandwidth			3			3		MHz
Output voltage swing (pos)		6.2			6.2			V
Output voltage swing (neg)				0.7		0.7		V
OUTPUT STAGE: Output current	Over temp	20			20			mA
$V_{ce Sat}$	$I_C = 20mA$ Over temp			0.4		0.4		V
SUPPLY VOLTAGE/CURRENT: I_S	$I_Z = 0,$ voltage fed	$T_A = 25^\circ C$		10.0		10.0		mA
		Over temp			13.0		13.0	mA
V_S	$I_S = 10mA,$ current fed	20.0	21.0	22.0	19.0	21.0	24.0	V

6

REGULATION VS ERROR AMP CLOSED LOOP GAIN

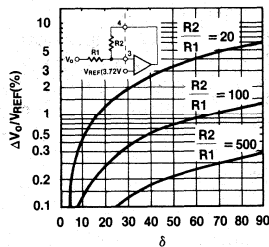


Figure 1

TRANSFER CURVE OF PULSE-WIDTH MODULATOR DUTY CYCLE VS INPUT VOLTAGE

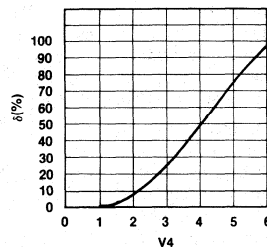


Figure 2

SWITCHED MODE POWER SUPPLY CONTROLLER

NE/SE5561

POWER DERATING CURVE

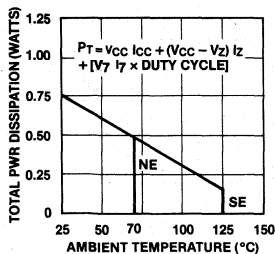


Figure 3

TYPICAL FREQUENCY PLOT VS RT AND CT

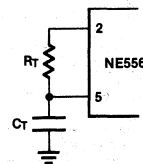
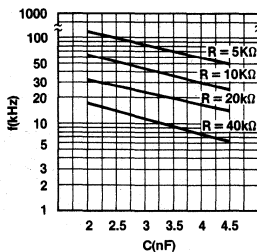


Figure 4

MAXIMUM DUTY CYCLE BASE VOLTAGE ON Q1

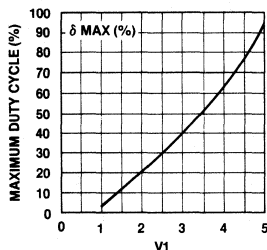
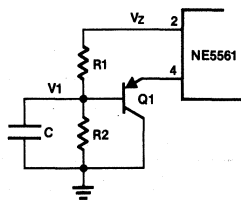


Figure 5a

START-UP CIRCUIT



$$\delta_{max} = f \left[\frac{R2}{R1 + R2} Vz + V_{BE Q1} \right]$$

Figure 5b

SLOW START VOLTAGE

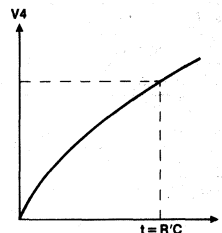


Figure 5c

NE5561 Start-Up

The start-up, or initial turn on, of this device requires some degree of external protective duty cycle limiting to prevent the duty cycle from initially going to the extreme maximum ($\delta > 90\%$). Either over-current limit or slow start circuitry must be employed to limit duty cycle to a safe value during start-up. Both may be used if desired.

To implement slow-start, the circuit of Figure 5b can be used. The divider R1 and R2 sets a voltage, buffered by Q1, such that the output of the error amplifier is clamped to a maximum output voltage, (Figure 5a) thereby limiting the maximum duty cycle. The addition of capacitor C will cause this voltage to ramp up slowly when power is applied, causing the duty cycle to ramp up simultaneously.

Over-current limit may be used also. To limit duty cycle in this mode, the switch current is monitored at pin 6 and the output of the 5561 is disabled on a cycle by cycle basis when current reaches the programmed limit. With current limit control of slow-start, the duty cycle is limited to that value just allowing maximum switch current to flow. (Approximately 0.50V measured at pin 6.)

5V, 0.5A Buck Regulator Operates from 15V

The converter design shows how simple it is to derive a TTL supply from a system supply of 15V (see Figure 6). The NE5561 drives a 2N4920 PNP transistor directly to provide switching current to the inductor.

Overall line regulation is excellent and covers a range of 12V to 18V with minimal change (< 10 mV) in the output operating at full load.

As with all NE5561 circuits, the auxiliary slow start and δ_{max} circuit is required, as evidenced by Q1. The δ_{max} limit may be calculated by using the relationship (Figure 5a, b).

$$\frac{R2}{R1 + R2} (8.2V) = V\delta_{(max)}$$

The maximum duty cycle is then determined from the pulse-width modulator transfer graph (see Figure 5a), and R1, R2 are defined from the desired conditions.

SWITCHED MODE POWER SUPPLY CONTROLLER

NE/SE5561

NE5561 Boost Converter with Output Variable (18V to 30V, 0.2A)

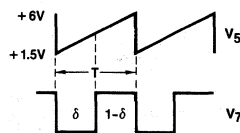
The circuit shown uses the NE5561 SMPS controller in a non-isolated boost converter operating from a 15V line. The addition of three transistors and one diode is necessary to complete the design (see Figure 7).

Operation is as follows. Q1 is a combination slow start and max duty cycle limit transistor. When power is first applied to the circuit, C7 in a discharged state begins to charge toward the divider voltage, V_{δ} . This $V_{\delta} + V_{BE}$ controls the voltage on pin 4, the error amp output, causing the duty cycle to be limited initially to δ_0 , then to gradually approach its normal operating range, δ . The base divider is fed from V_Z , which is nominally 8.2V.

Output regulation starts at the error amplifier, with gain set by R2 (adj) and R5 combination. The error amp is stable for closed loop gain in excess of 40 dB (X100), for which the regulation will be approximately 1%. C4 is added to the output to insure stability at gain below 40 dB. C4 creates a dominant pole at approximately 1 kHz, descending at 6 dB per octave to unity near 1 MHz. Input to the error amplifier is referenced to 3.76V and must reach this reference level for the output of the NE5561 to be active. Output voltage is then the quantity. (D_R) 3.7V

If R2 ratio is, for instance, 10:1, the output will be $\approx 37V$. If the ratio is 5:1, the output will be $\approx 18.5V$, etc.

Output to Q2 base is a square wave of variable duty cycle as determined by load demand. The internal transistor is open collector and must have a pull-up resistance, in this application the base circuit of Q2. The duty cycle δ is a fraction between 0 and 1. The actual on-time is proportional then to $\delta \cdot T$, where T is the period of the free-running frequency of the sawtooth generator internal the NE5561. Frequency is set by the RC combination, $R7 \cdot C5$ with charging current supplied from V_Z (8.2V). The stabilizing effect of the internal zener supply gives a constant frequency. The sawtooth waveform is related to duty cycle as shown below.



(V7 NOT TO SCALE)

Q3 is switched on during the saturated portion of the output waveform from pin 7 of the NE5561, termed δ , and is switched off during the remainder of the cycle (1- δ).

The sawtooth frequency is set at approximately 22 kHz in this example. The NE5561 is capable of operation to 100 kHz, however.

Pin 6 of the NE5561 operates an over-current protective feature which resets the output on pin 7 if the instantaneous pin 6 voltage exceeds 0.50V. In this case, R8 determines the peak current of Q3 emitter circuit prior to shutdown. The operation of the over-current circuit is on a pulse to pulse basis, returning to normal as soon as the pin 6 voltage falls below 0.50V. As is noted, a small degree of filtering is needed to eliminate short switching transient, allowing only the primary current waveform to be sensed.

Switching circuit operation proceeds as follows. Q3 turns on, causing magnetization current to begin increasing in L1, the switching inductor. After initial start up, C3 is charged to the output, thus with Q3 on, Diode D1 is reverse biased and does not conduct during the duty cycle, δ . C3, the output capacitor, sustains the full load current during this part of the cycle. When Q3 turns off, the magnetic field energy previously stored in L1 is discharged through

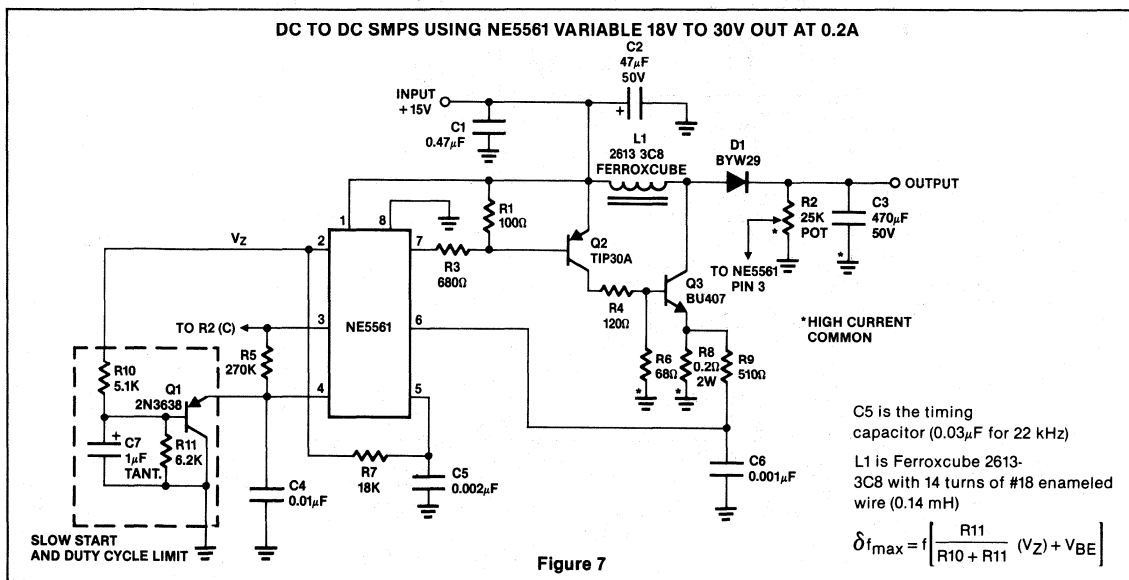


Figure 7

C5 is the timing capacitor (0.03 μ F for 22 kHz)

L1 is Ferroxcube 2613-3C8 with 14 turns of #18 enameled wire (0.14 mH)

$$\delta_{f_{max}} = f \left[\frac{R11}{R10 + R11} (V_Z) + V_{BE} \right]$$

SWITCHED MODE POWER SUPPLY CONTROLLER

NE/SE5561

D1 now forward biased. The output capacitor is incrementally charged, restoring its depleted voltage. The ripple voltage is a function of the size of C3 and its internal resistance. For minimum ripple, a low ESR (Equivalent Series Resistance) capacitor must be used, since previously mentioned peak load current flows in C3.

Single Transistor 100V, 250 mA Buck Converter

With a single 15V zener diode to limit package dissipation, the NE5561 controller may be operated directly from the rectified AC line. The following example shows the simplicity of such a converter which is capable of a nominal 100V output (see Figure 9). A base drive transformer is used to gain high voltage isolation between the NE5561 and the switching transistor, and to provide adequate base drive. A low power PNP transistor is used in an auxiliary slow

start and duty cycle limiting circuit to prevent over-excitation (Q1).

Operation is as follows. Drive from the NE5561 output is fed to the primary of T1, base drive transformer, with a pulse-width modulated signal causing Q2 (BU407) to switch current to inductor, L1. As the current builds up, energy is stored in L1, coincident with the saturation period (δ) of the NE5561 output stage. During this period, current also flows through L1 to C_o and the load. When Q2 cuts off, the choke field collapses and D1 conducts as the load is sustained by the inductor-stored energy.

V_{OUT} is sampled by the divider R7 and R8, rising until the junction of the output is forced to 3.75V. Load variations are thus translated to duty cycle variations to maintain constant voltage at the output. The measured constant efficiency at 0.5A load is in excess of 72%. Line regulation is good from approximately 93V to 120V.

The base current waveform driving Q2 is shown in Figure 8. This indicates that the BU407 base current rises initially to 60 mA to obtain fast turn-on, then settles to about 40 mA for the remainder of the duty cycle, δ . Reverse biasing of the emitter-base junction occurs to enhance turn-off.

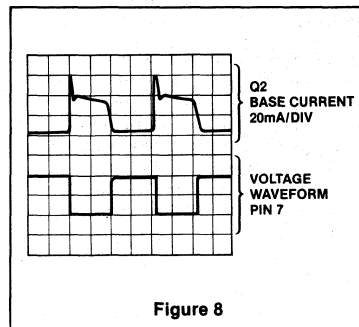


Figure 8

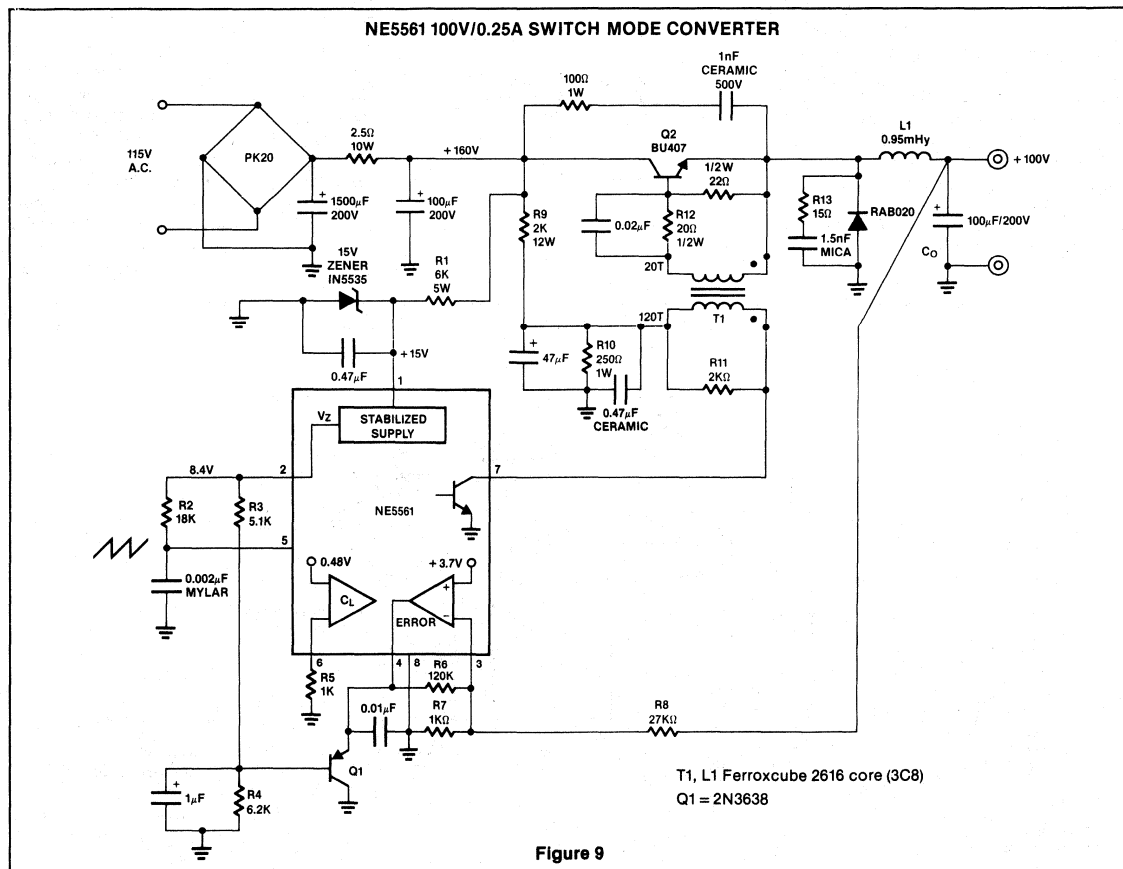


Figure 9

SWITCHED MODE POWER SUPPLY CONTROLLER

NE/SE5561

Snubber networks are necessary, as shown across Q2 and commutation diode, D1, to prevent component failure during fast switching. It is critical that these networks be placed physically adjacent to the respective components they protect, and that low inductance capacitors and resistors be used as snubbers (ceramic or dura mica caps and carbon resistors).

The base drive transformer is constructed using a Ferroxcube 2616-3C8 core, with primary of 120 turns of #26 wire, and 20 turns of #26 on secondary. The primary is wound in a simple solenoidal manner, first on the bobbin, followed by a layer of mylar tape to provide voltage isolation. Next, the secondary winding is added. Primary inductance measures 45 mH with a leakage inductance of 120 μ H. It is important to have sufficient primary inductance to prevent excessive droop in base drive current. Also, leakage reactance must be kept reasonably low to minimize ringing.

DC Motor Drive with Fixed Speed Control

The circuit shown in Figure 10b incorporates a simple switch mode approach to DC

motor control, which is efficient and free of the dissipation problems inherent in linear drives. The NE5561 provides pulse proportional drive and speed control based on DC tachometer feedback. A simple switching circuit consisting of one transistor (2N4920 PNP) and a commutation diode is used to deliver programmed pulse energy to the motor.

A frequency of approximately 20 kHz is used to eliminate audio noise present in some switching drives. The DC tach in this example delivers 2.7V/1000 RPM. Its output is such that negative feedback occurs when this voltage is applied to the error amplifier of the NE5561, pin 3, through a suitable divider. Note that the voltage to pin 3 must be 3.75V in order to obtain servo lock. Thus, the divider from the tach output must be appropriate to maintain the proper ratio for speed control to occur.

As shown in the waveform photo (Figure 10a), duty cycle varies directly with load torque demand. No load current is \approx 0.3A and full load is 0.6A. Current and voltage waveforms at 0.6A are shown in Figure 10. If desired, torque limiting may be set by feed-

ing a derivative of motor return current back to pin 6 of the NE5561.

Operating range is 12V to 18V input for a tach output nominal variation of less than 20 mV, and approximately 4.35V for the divider values shown. The motor is a Globe 100A 565 rated at 12V DC.

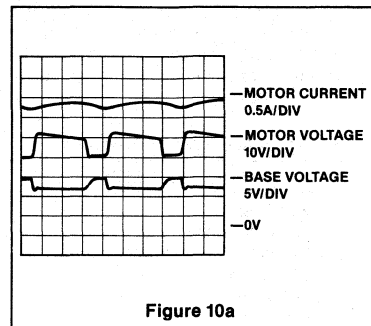


Figure 10a

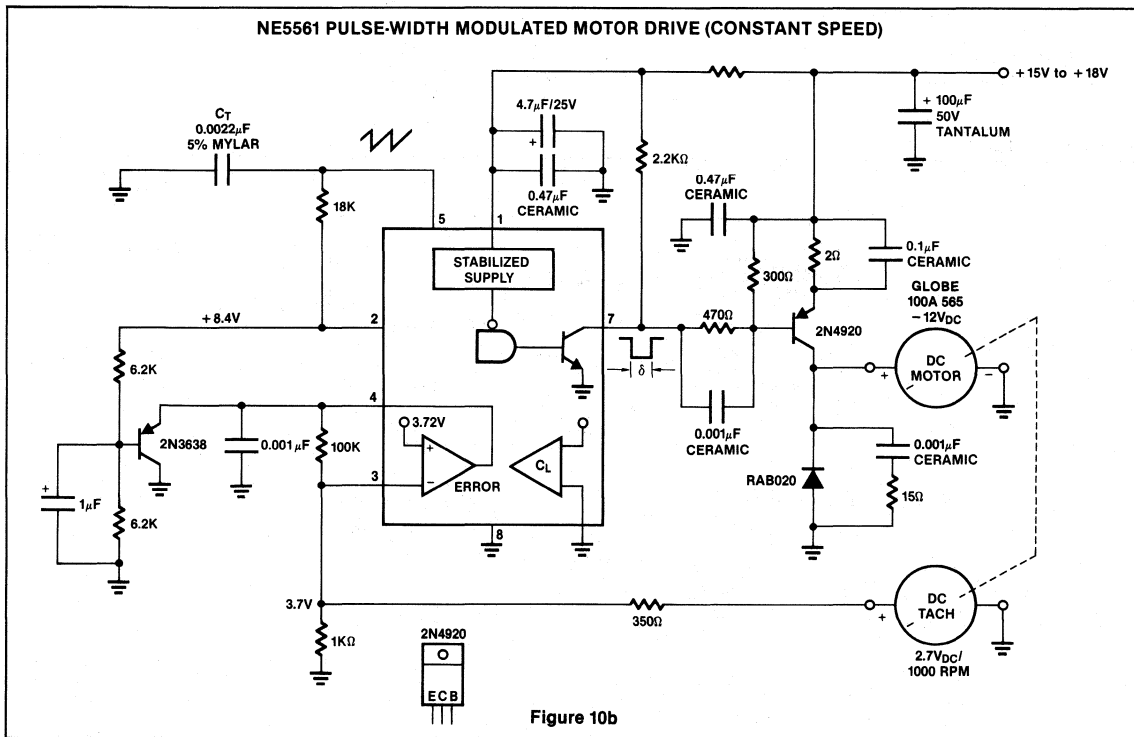
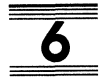


Figure 10b

REGULATING PULSE WIDTH MODULATOR

SG1524/SG2524/SG3524

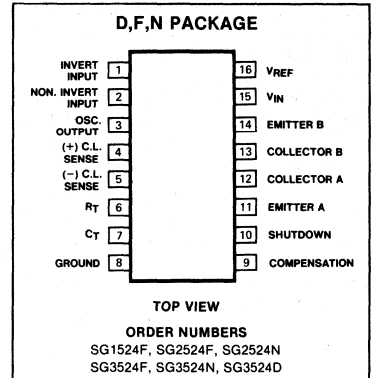
DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG1524 is specified for operation over the full military temperature range of -55°C to $+125^{\circ}\text{C}$, while the SG2524 and SG3524 are designed for commercial applications of 0°C to $+70^{\circ}\text{C}$.

FEATURES

- Complete PWM power control circuitry
- Single ended or push-pull outputs
- Line and load regulation of 0.2%
- 1% maximum temperature variation
- Total supply current is less than 10mA
- Operation beyond 100kHz

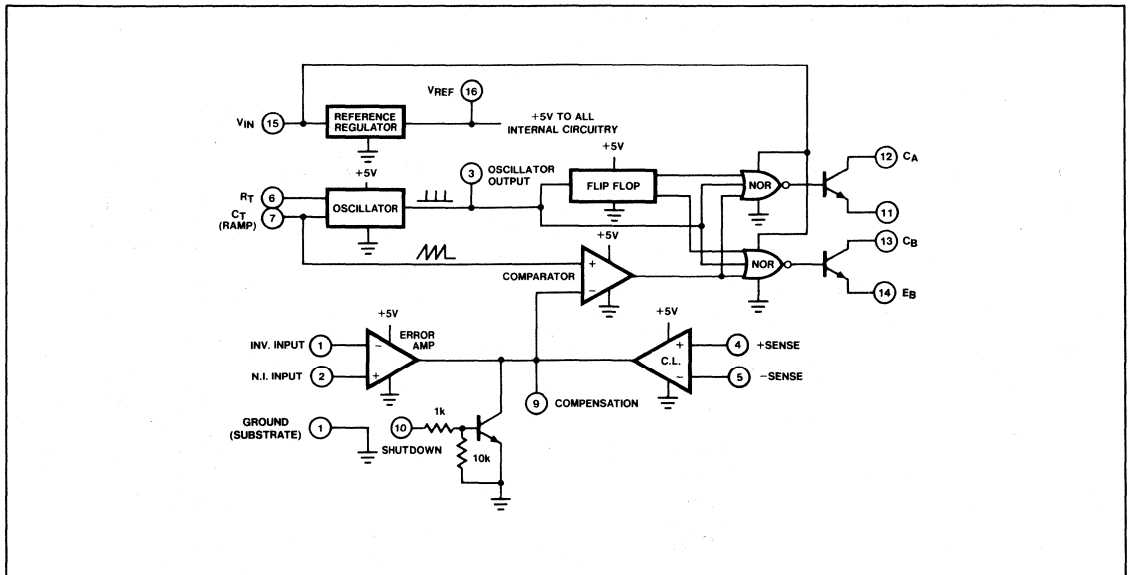
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage	40	V
Output current (each output)	100	mA
Reference output current	50	mA
Oscillator charging current	5	mA
Power dissipation		
Package limitation	1000	mW
Derate above 25°C	8	mW/ $^{\circ}\text{C}$
Operating temperature range		
SG1524	-55 to $+125$	$^{\circ}\text{C}$
SG2524/SG3524	0 to $+70$	$^{\circ}\text{C}$
Storage temperature range	-65 to $+150$	$^{\circ}\text{C}$

BLOCK DIAGRAM



REGULATING PULSE WIDTH MODULATOR

SG1524/SG2524/SG3524

DC ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the SG1524 and 0°C to $+70^\circ\text{C}$ for the SG2524 and SG3524, $V_{IN} = 20\text{V}$, and $f = 20\text{kHz}$)

PARAMETER	TEST CONDITIONS	SG1524 SG2524			SG3524			UNIT
		Min	Typ	Max	Min	Typ	Max	
REFERENCE SECTION								
Output voltage		4.8	5.0	5.2	4.6	5.0	5.4	V
Line regulation	$V_{IN} = 8$ to 40V		10	20		10	30	mV
Load regulation	$I_L = 0$ to 20mA		20	50		20	50	mV
Ripple rejection	$f = 120\text{Hz}$, $T_A = 25^\circ\text{C}$		66			66		dB
Short circuit current limit	$V_{REF} = 0$, $T_A = 25^\circ\text{C}$		100			100		mA
Temperature stability	Over operating temperature range		0.3	1		0.3	1	%
Long term stability	$T_A = 25^\circ\text{C}$		20			20		mV / kHr
OSCILLATOR SECTION								
Maximum frequency	$C_T = .001$ mfd, $R_T = 2\text{k}\Omega$		300			300		kHz
Initial accuracy	R_T and C_T constant		5			5		%
Voltage stability	$V_{IN} = 8$ to 40V , $T_A = 25^\circ\text{C}$			1			1	%
Temperature stability	Over operating temperature range						2	%
Output amplitude	Pin 3, $T_A = 25^\circ\text{C}$		3.5			3.5		V_P
Output pulse width	$C_T = .01$ mfd, $T_A = 25^\circ\text{C}$		0.5			0.5		μs
ERROR AMPLIFIER SECTION								
Input offset voltage	$V_{CM} = 2.5\text{V}$		0.5	5		2	10	mV
Input bias current	$V_{CM} = 2.5\text{V}$		2	20		2	10	μA
Open loop voltage gain		72	80		60	80		dB
Common mode voltage	$T_A = 25^\circ\text{C}$	1.8		3.4	1.8		3.4	V
Common mode rejection ratio	$T_A = 25^\circ\text{C}$		70			70		dB
Small signal bandwidth	$A_V = 0\text{dB}$, $T_A = 25^\circ\text{C}$		3			3		MHz
Output voltage	$T_A = 25^\circ\text{C}$	0.5		3.8	0.5		3.8	V
COMPARATOR SECTION								
Duty cycle	% each output "ON"	0		45	0		45	%
Input threshold	Zero duty cycle		1			1		V
Input threshold	Maximum duty cycle		3.5			3.5		V
Input bias current			1			1		μA
CURRENT LIMITING SECTION								
Sense voltage	Pin 9 = 2V with error amplifier set for maximum out, $T_A = 25^\circ\text{C}$	190	200	210	180	200	220	mV
Sense voltage T.C.			0.2			0.2		mV / $^\circ\text{C}$
Common mode voltage		-1		+1	-1		+1	V
OUTPUT SECTION (each output)								
Collector-emitter voltage (breakdown)		40			40			V
Collector-leakage current	$V_{CE} = 40\text{V}$		0.1	50		0.1	50	μA
Saturation voltage	$I_C = 50\text{mA}$		1	2		1	2	V
Emitter output voltage	$V_{IN} = 20\text{V}$	17	18		17	18		V

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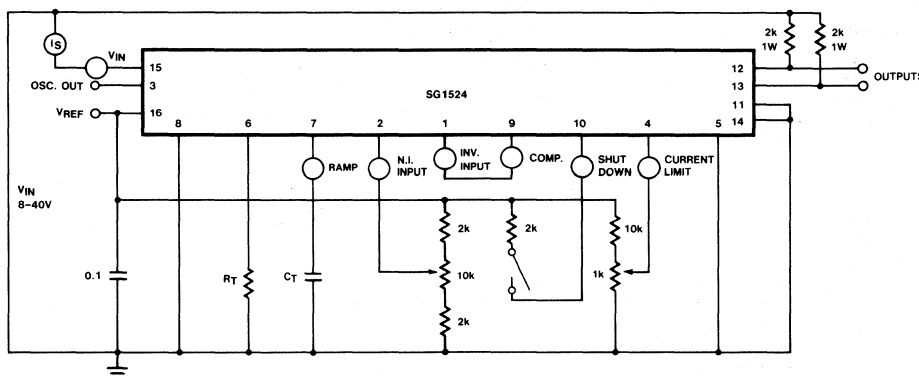
REGULATING PULSE WIDTH MODULATOR

SG1524/SG2524/SG3524

DC ELECTRICAL CHARACTERISTICS (Cont'd) (Unless otherwise stated, these specifications apply for $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ for the SG1524 and 0°C to $+70^\circ\text{C}$ for the SG2524 and SG3524, $V_{IN} = 20\text{V}$, and $f = 20\text{kHz}$)

PARAMETER	TEST CONDITIONS	SG1524 SG2524			SG3524			UNIT
		Min	Typ	Max	Min	Typ	Max	
Rise time	$R_C = 2\text{K ohm}, T_A = 25^\circ\text{C}$		0.2			0.2		μs
Fall time	$R_C = 2\text{K ohm}, T_A = 25^\circ\text{C}$		0.1			0.1		μs
TOTAL STANDBY CURRENT (excluding oscillator charging current, error and current limit dividers, and with outputs open)	$V_{IN} = 40\text{V}$		8	10		8	10	mA

OPEN LOOP TEST CIRCUIT



APPLICATIONS

Voltage Reference

An internal series regulator provides a nominal 5 volt output which is used both to generate a reference voltage and is the regulated source for all the internal timing and controlling circuitry. This regulator may be bypassed for operation from a fixed 5 volt supply by connecting pins 15 and 16 together to the input voltage. In this configuration, the maximum input voltage is 6.0 volts.

This reference regulator may be used as a 5 volt source for other circuitry. It will provide up to 50mA of current itself and can easily be expanded to higher currents with an external PNP as shown in Figure 1.

TYPICAL APPLICATION

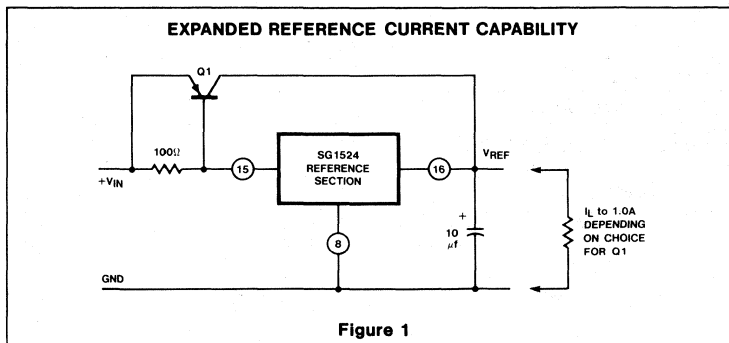


Figure 1

REGULATING PULSE WIDTH MODULATOR

SG1524/SG2524/SG3524

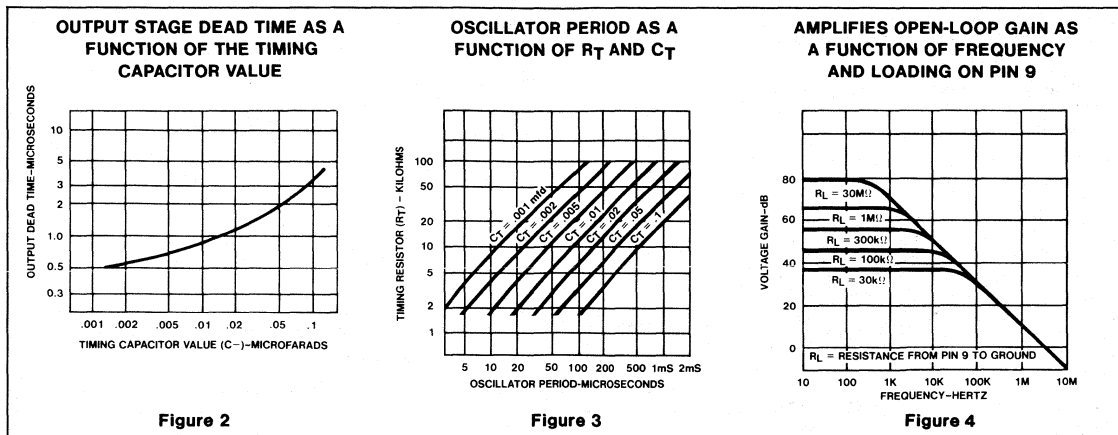


Figure 2

Figure 3

Figure 4



Oscillator

The oscillator in the SG1524 uses an external resistor (R_T) to establish a constant charging current into an external capacitor (C_T). While this uses more current than a series connected RC, it provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The

charging current is equal to 3.6V ÷ R_T and should be kept within the range of approximately 30μA to 2mA, i.e., 1.8K < R_T < 100K.

The range of values for C_T also has limits as the discharge time of C_T determines the pulse width of the oscillator output pulse. This pulse is used (among other things) as a blanking pulse to both outputs to insure that there is no possibility of having both outputs on simultaneously during transitions. This output dead time relationship is shown in Figure 2. A pulse width below approximately 0.5 microseconds may allow false triggering of one output by removing the blanking pulse prior to the flip-flops reaching a stable state. If small values of C_T must be used, the pulse width may still be expanded by adding a shunt capacitance (≈ 100pF) to ground at the oscillator output. (Note: Although the oscillator output is a convenient oscilloscope sync input, the cable and input capacitance may increase the blanking pulse width slightly.) Obviously, the upper limit to the pulse width is determined by the maximum duty cycle acceptable. Practical values of C_T fall between .001 and 0.1 microfarad.

The oscillator period is approximately $t = R_T C_T$ where t is in microseconds when R_T = ohms and C_T = microfarads. The use of Figure 3 will allow selection of R_T and C_T for a wide range of operating frequencies. Note that for series regulator applications, the

two outputs can be connected in parallel for an effective 0-90% duty cycle and the frequency of the oscillator is the frequency of the output. For push-pull applications, the outputs are separated and the flip-flop divides the frequency such that each outputs duty cycle is 0-45% and the overall frequency is one-half that of the oscillator.

External Synchronization

If it is desired to synchronize the SG1524 to an external clock, a pulse of ≈ +3 volts may be applied to the oscillator output terminal with R_TC_T set slightly greater than the clock period. The same considerations of pulse width apply. The impedance to ground at this point is approximately 2K ohms.

If two or more SG1524's must be synchronized together, one must be designated as master with its R_TC_T set for the correct period. The slaves should each have an R_TC_T set for approximately 10% longer period than the master with the added requirement that C_T (slave) = one-half C_T (master). Then connecting Pin 3 on all units together will insure that the master output pulse—which occurs first and has a wider pulse width—will reset the slave units.

Error Amplifier

This circuit is a simple differential-input, transconductance amplifier. The output is the compensation terminal, pin 9, which is a high impedance node (R_L ≈ 5MΩ). The gain is

$$A_v = gmR_L = \frac{8 I_C R_L}{2kT} \approx .002 R_L$$

and can easily be reduced from a nominal of 10,000 by an external shunt resistance from pin 9 to ground, as shown in Figure 4.

In addition to DC gain control, the compensation terminal is also the place for AC phase compensation. The frequency response curves of Figure 4 show the uncompensated amplifier with a single pole at approximately 200Hz and a unity gain cross-over at 5MHz.

Typically, most output filter designs will introduce one or more additional poles at a significantly lower frequency. Therefore, the best stabilizing network is a series R-C combination between pin 9 and ground which introduces a zero to cancel one of the output filter poles. A good starting point is 50kΩ plus .001 microfarad.

One final point on the compensation terminal is that this is also a convenient place to insert any programming signal which is to override the error amplifier. Internal shutdown and current limit circuits are connected here, but any other circuit which can sink 200μA can pull this point to ground thus shutting off both outputs.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and is stable in either the inverting or non-inverting mode. Regardless of the connections, however, input common-mode limits must be observed or output signal inversions may result. For conventional regulator applications, the 5 volt reference voltage must be divided down as shown in Figure 5. The error amplifier may also be used in fixed duty cycle applications by using the unity gain configuration shown in the open loop test circuit.

REGULATING PULSE WIDTH MODULATOR

SG1524/SG2524/SG3524

Current Limiting

The current limiting circuitry of the SG1524 is shown in Figure 6.

By matching the base-emitter voltages of Q1 and Q2, and assuming negligible voltage drop across R₁,

$$\begin{aligned} \text{Threshold} &= V_{BE}(Q1) + I_1 R_2 - V_{BE}(Q2) \\ &= I_1 R_2 \approx 200\text{mV} \end{aligned}$$

Although this circuit provides a relatively small threshold with a negligible temperature coefficient, there are some limitations to its use, the most important of which is the ± 1 volt common mode range which requires sensing in the ground line. Another factor to consider is that the frequency compensation provided by R₁C₁ and Q1 provides a roll-off pole at approximately 300Hz.

Since the gain of this circuit is relatively low, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, threshold is defined as the input voltage to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, pins 4 and 5 may also be used in transformer-coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur. (Refer to Figure 11). Another application is to ground pin 5 and use pin 4 as an additional shutdown terminal; i.e., the output will be off with pin 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 7. This circuit can reduce the short-circuit current (I_{SC}) to approximately one-third the maximum available output current (I_{MAX}).

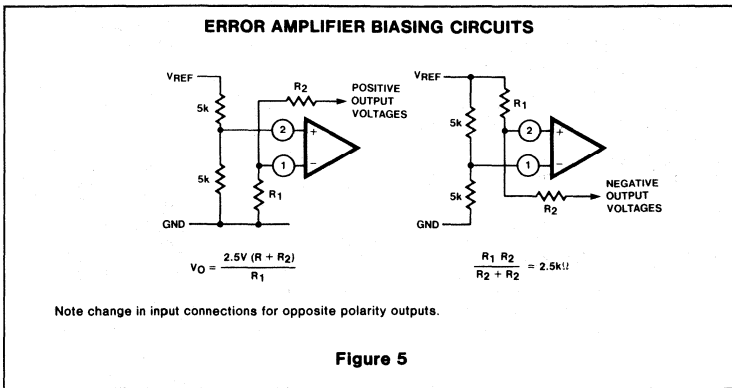


Figure 5

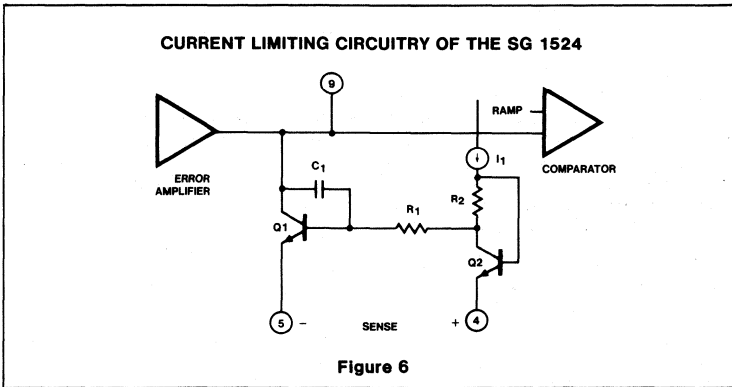


Figure 6

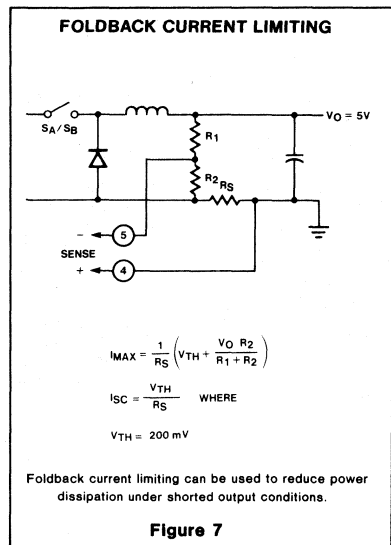
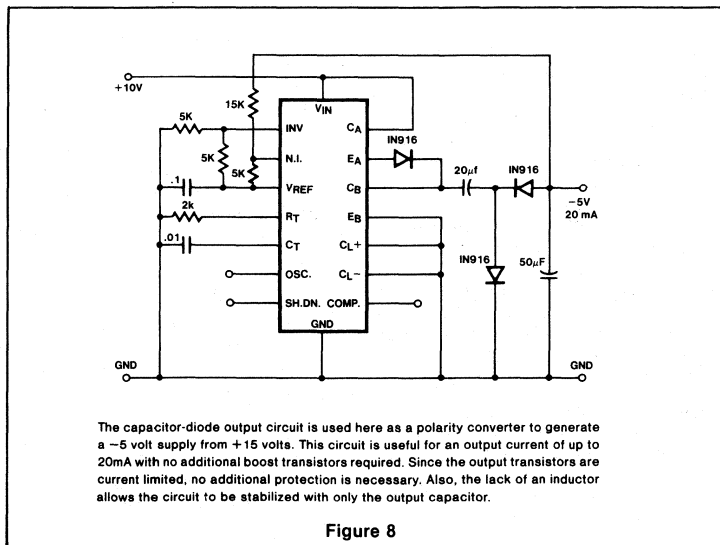


Figure 7

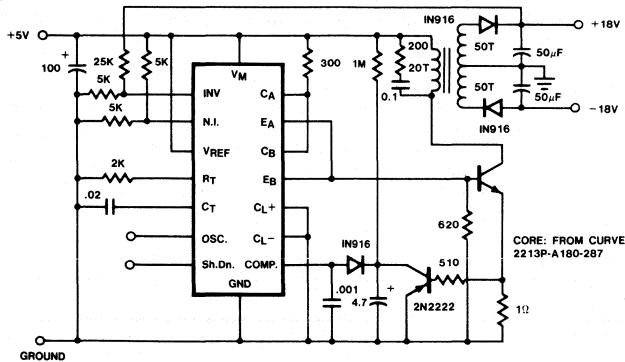


The capacitor-diode output circuit is used here as a polarity converter to generate a -5 volt supply from +15 volts. This circuit is useful for an output current of up to 20mA with no additional boost transistors required. Since the output transistors are current limited, no additional protection is necessary. Also, the lack of an inductor allows the circuit to be stabilized with only the output capacitor.

Figure 8

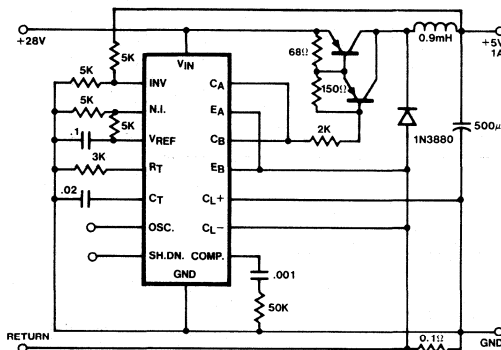
REGULATING PULSE WIDTH MODULATOR

SG1524/SG2524/SG3524



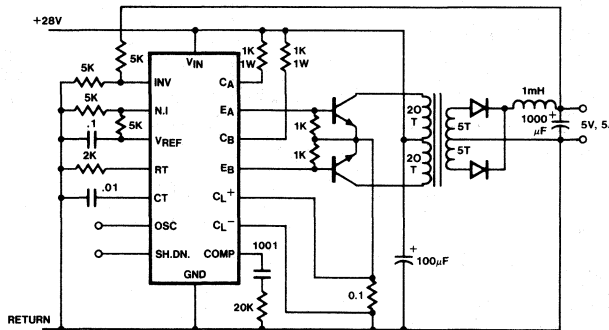
Another low-current supply is the flyback converter used here to generate ± 15 volts at 20mA from a +5 volt regulated line. The reference generator in the SG1524 is unused with the input voltage providing the reference. Current limiting in a flyback converter is difficult and is accomplished here by sensing current in the primary line and resetting a soft-start circuit.

Figure 9



In this conventional single-ended regulator circuit, the two outputs of the SG1524 are connected in parallel for effective 0-90% duty-cycle modulation. The use of an output inductor requires an R-C phase compensation network for loop stability.

Figure 10



Push-pull outputs are used in this transformer-coupled DC-DC regulating converter. Note that the oscillator must be set at twice the desired output frequency as the SG1524's internal flip-flop divides the frequency by 2 as it switches the P.W.M. signal from one output to the other. Current limiting is done here in the primary so that the pulse width will be reduced should transformer saturation occur.

Figure 11

6

PRECISION VOLTAGE REGULATOR

μ A723/723C/SA723C

DESCRIPTION

The μ A723/SA723C is a Monolithic Precision Voltage Regulator capable of operation in positive or negative supplies as a series, shunt, switching or floating regulator. The 723 contains a temperature compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

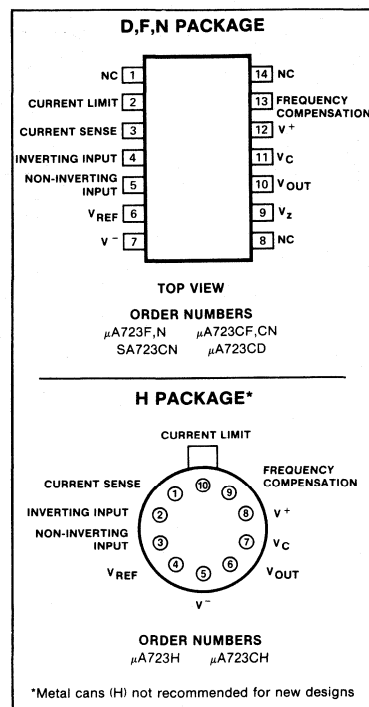
FEATURES

- Positive or negative supply operation
- Series, shunt, switching or floating operation
- .01% line and load regulation
- Output voltage adjustable from 2 to 37 volts
- Output current to 150mA without external pass transistor
- μ A723 MIL STD 88 3A, B, C available

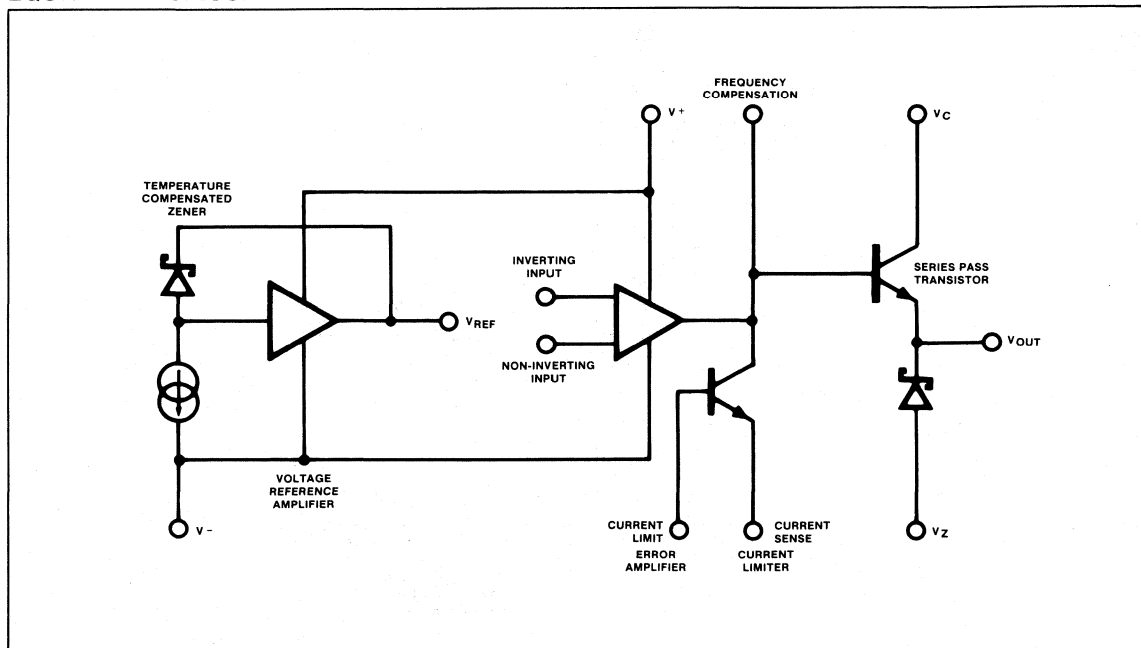
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Pulse voltage from $V+$ to $V-$ (50 ms)	50	V
Continuous voltage from $V+$ to $V-$	40	V
Input-output voltage differential	40	V
Maximum output current	150	mA
Current from V_{REF}	15	mA
Current from V_Z	25	mA
Internal power dissipation ¹	800	mW
Operating temperature range		
μ A723	-55 to +125	$^{\circ}$ C
μ A723C	0 to 70	$^{\circ}$ C
SA723C	-40 to +85	$^{\circ}$ C
Storage temperature range	-65 to +150	$^{\circ}$ C
Lead temperature	300	$^{\circ}$ C

PIN CONFIGURATIONS



EQUIVALENT CIRCUIT



PRECISION VOLTAGE REGULATOR

μA723/723C/SA723C

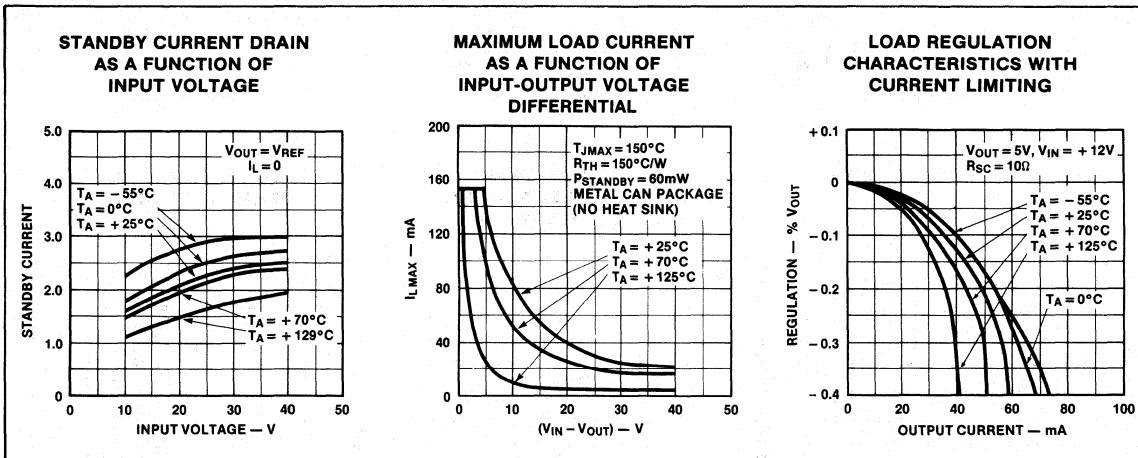
DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.¹

PARAMETER	TEST CONDITIONS	μA723			μA723C/SA723C			UNIT
		Min	Typ	Max	Min	Typ	Max	
Line regulation ²	$V_{IN} = 12\text{V to } V_{IN} = 15\text{V}$ $V_{IN} = 12\text{V to } V_{IN} = 40\text{V}$		0.01 0.02	0.1 0.2		0.01 0.1	0.1 0.5	% V_{OUT} % V_{OUT}
Load regulation ²	$I_L = 1\text{mA to } I_L = 50\text{mA}$ $f = 50\text{Hz to } 10\text{kHz}, C_{REF} = 0$ $f = 50\text{Hz to } 10\text{kHz}, C_{REF} = 5\mu\text{F}$		0.03 74 86	0.15		0.03 74 86	0.2	% V_{OUT} dB dB
Short circuit current limit	$R_{SC} = 10\Omega, V_{OUT} = 0$		65			65		mA
Reference voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output noise voltage	$BW = 100\text{Hz to } 10\text{kHz}, C_{REF} = 0$ $BW = 100\text{Hz to } 10\text{kHz}, C_{REF} = 5\mu\text{F}$		20 2.5			20 2.5		μVrms μVrms
Long term stability			0.1			0.1	0.1	%/1000hrs.
Standby current drain	$I_L = 0, V_{IN} = 30\text{V}$		2.3	3.5		2.3	4.0	mA
Input voltage range		9.5		40	9.5		40	V
Output voltage range		2.0		37	2.0		37	V
Input-output voltage differential		3.0		38	3.0		38	V
The following specifications apply over the operating temperature ranges								
Line regulation				0.3			0.3	% V_{OUT}
Load regulation				0.6			0.6	% V_{OUT}
Average temperature coefficient of output voltage	$V_{IN} = 12\text{V to } V_{IN} = 15\text{V}$ $I_L = 1\text{mA to } I_L = 50\text{mA}$		0.002	0.015		0.003	0.015	%/ $^\circ\text{C}$

NOTES

- $V_{IN} = V^+ = V_C = 12\text{V}, V^- = 0\text{V}, V_{OUT} = 5\text{V}, I_L = 1\text{mA}, R_{SC} = 0, C_1 = 100\mu\text{F}, C_{REF} = 0$ and divider impedance as seen by error amplifier $\leq 10\text{k}\Omega$ when connected as shown in Figure 3.
- The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

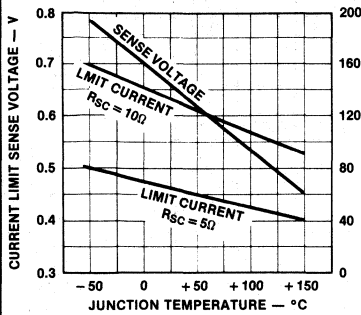


PRECISION VOLTAGE REGULATOR

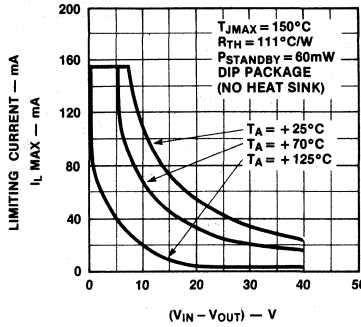
μ A723/723C/SA723C

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

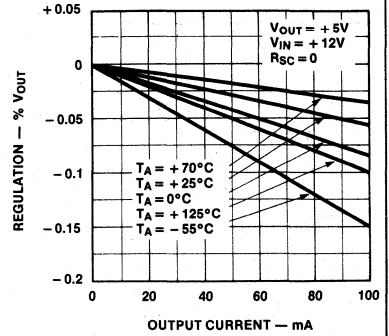
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



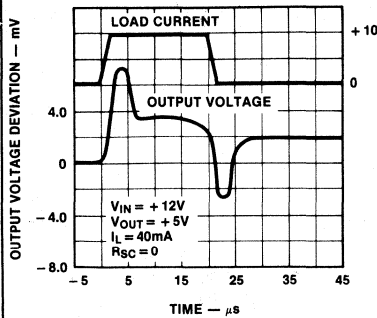
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



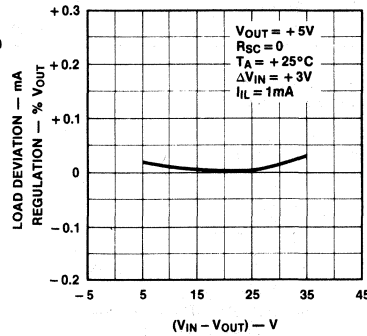
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



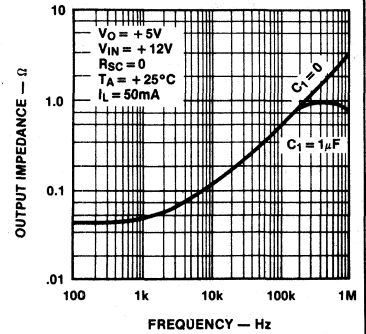
LOAD TRANSIENT RESPONSE



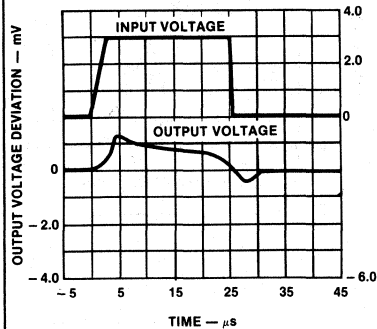
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



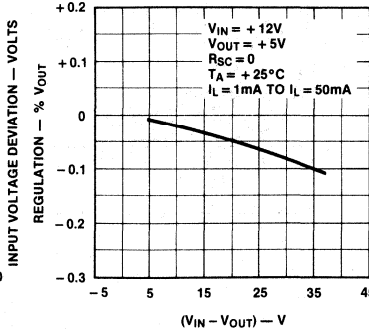
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



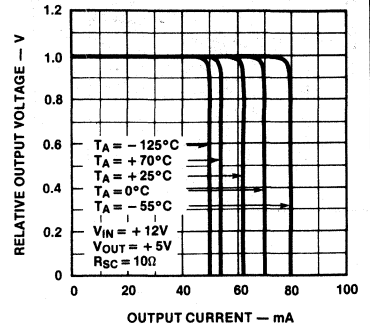
LINE TRANSIENT RESPONSE



LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



CURRENT LIMITING CHARACTERISTICS

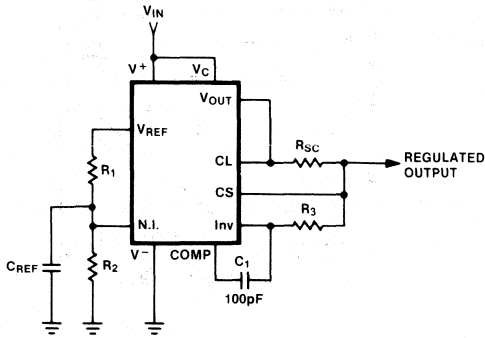


PRECISION VOLTAGE REGULATOR

μ A723/723C/SA723C

TYPICAL APPLICATIONS

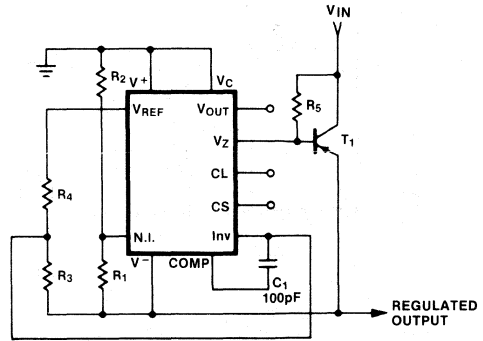
LOW VOLTAGE REGULATOR
($V_{OUT} = 2$ TO 7 VOLTS)



$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2} \right]$$

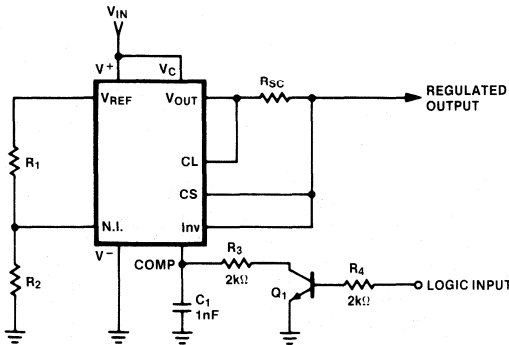
$$R_3 = \frac{R_1 R_2}{R_1 + R_2} \text{ for minimum temperature drift}$$

NEGATIVE VOLTAGE REGULATOR



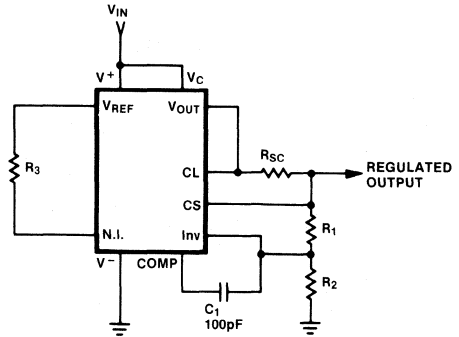
$$V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1} \right]; R_3 = R_4$$

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING
($V_{OUT} = 2$ TO 7 VOLTS)



$$V_{OUT} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2} \right]$$

HIGH VOLTAGE REGULATOR
($V_{OUT} = 7$ TO 37 VOLTS)



$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2} \right]$$

$R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift

R3 may be eliminated for minimum component count

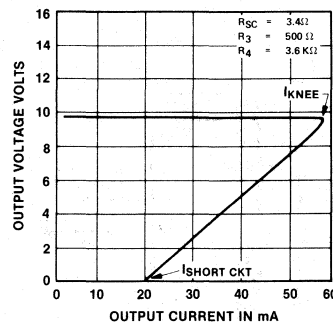
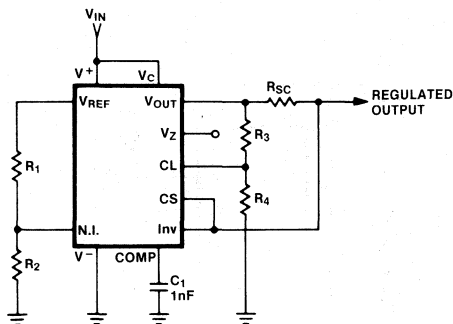
6

PRECISION VOLTAGE REGULATOR

μ A723/723C/SA723C

TYPICAL APPLICATIONS (Cont'd)

FOLDBACK CURRENT LIMITING REGULATOR ($V_{OUT} = 2$ TO 7 VOLTS)



$$I_{KNEE} = \left[\frac{V_{OUT} R_3 + V_{SENSE} (R_3 + R_4)}{R_{SC} R_4} \right]$$

$$V_{OUT} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2} \right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE} \times (R_3 + R_4)}{R_{SC} R_4} \right]$$

$$\frac{R_4}{R_3} = \frac{V_{OUT} I_{SC}}{V_{SENSE} (I_{KNEE} - I_{SHORT\ CKT})} - 1$$

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}} \left[1 + \frac{R_3}{R_4} \right]$$

Section 7 Motor Control and Sensor Circuits

INDEX

Section 7 — Motor Control and Sensor Circuits

Index	7-1
Product Data	7-3
NE544/644 Servo Amplifier	7-3
NE5044 Programmable Seven Channel RC Encoder	7-9
NE5045 Seven Channel RC Decoder	7-12
NE5046 Two Channel RC Decoder	7-15
NE5520 LVDT Signal Conditioner	7-17

SERVO AMPLIFIER

NE544/644

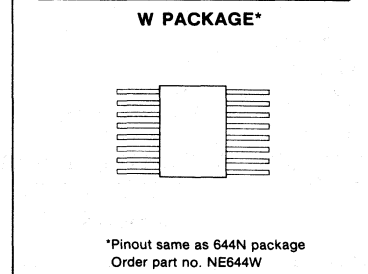
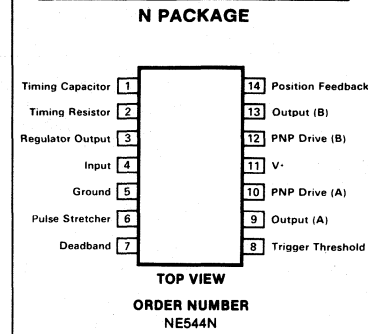
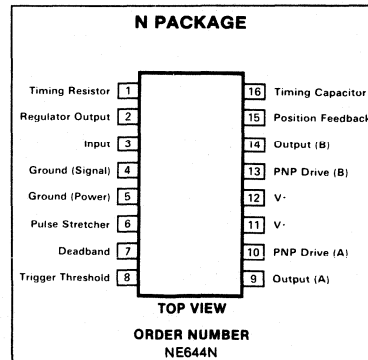
DESCRIPTION

The NE544 is a servo amplifier and pulse-width demodulator with internal motor drive transistors. It is designed for remote control applications in digital proportional systems but can be used in many other closed loop position control applications. It incorporates a linear one shot for improved positional accuracy and outputs for external pnp motor drive transistors.

FEATURES

- 500mA load current capability
- Bidirectional bridge output with single power supply
- Low standby power drain
- Adjustable deadband and trigger thresholds
- High linearity, 0.5% maximum error
- Output drive for external PNP transistors (optional)
- Wide supply voltage range

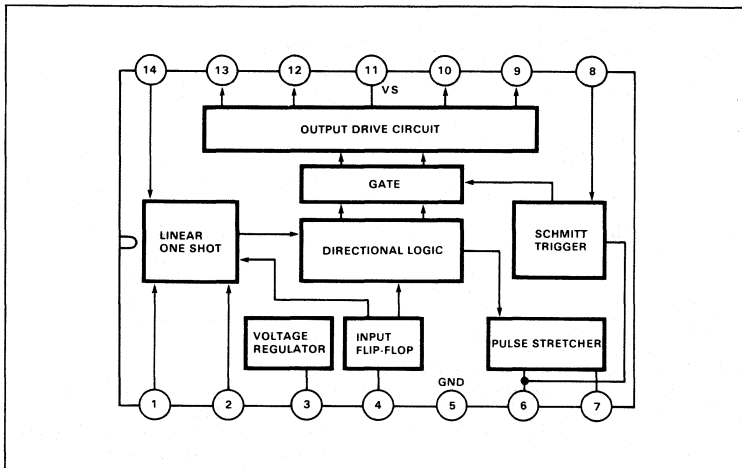
PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	RATING	UNIT	
V+	Supply voltage	6.0	V
I _O	Output current	500	mA
T _A	Operating temperature	-20 to +75	°C
T _{stg}	Storage temperature	-65 to +150	°C

BLOCK DIAGRAM

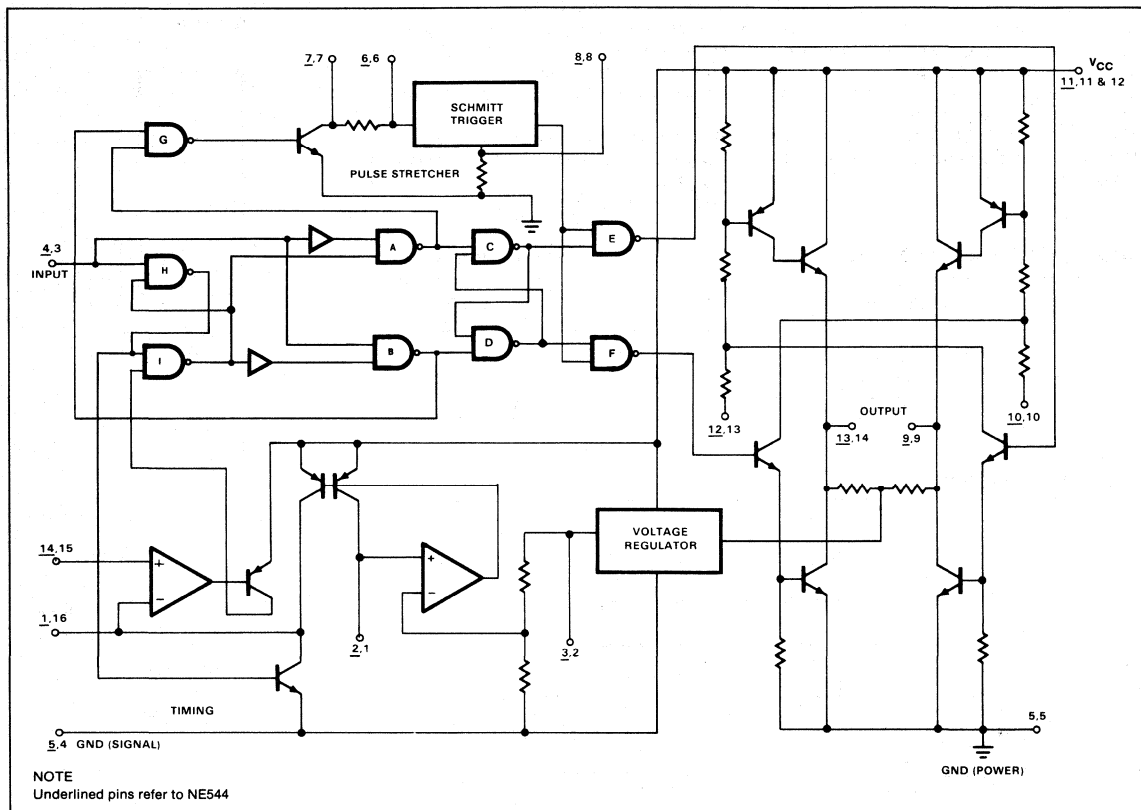


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SERVO AMPLIFIER

NE544/644

EQUIVALENT CIRCUIT SCHEMATIC



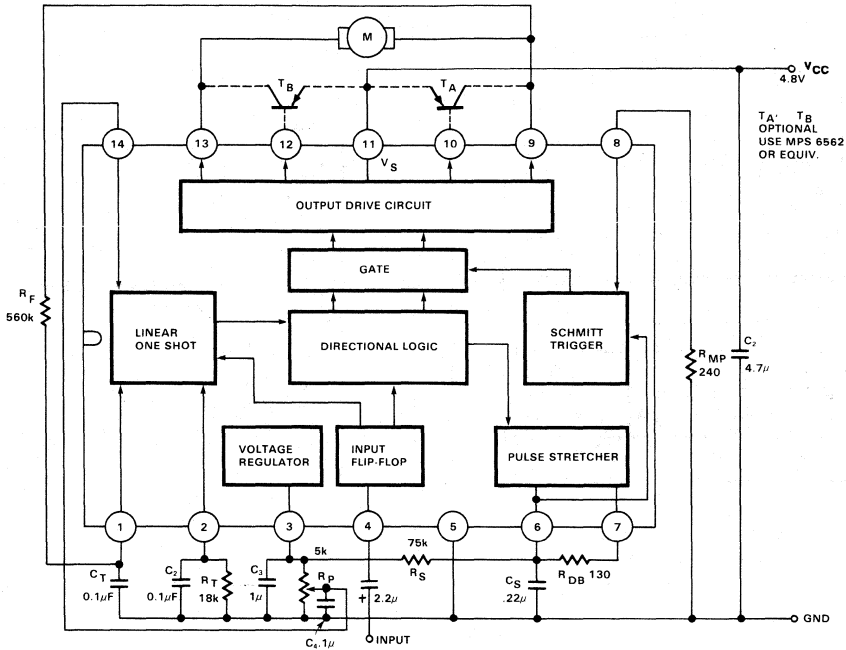
DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_S = 4.8\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{CC} Supply voltage		3.2	4.8	6	V
I_{CC} Supply current	Pin 11 Quiescent	4.2	5.5	10	mA
V_{TH} Input threshold	Pin 4		1.5		V
	On		1.4		
	Off		18		k Ω
Z_{IN} Input resistance	Pin 4				
V_{OL} Output voltage			0.3		V
V_{OH} Output voltage	Pin 9 or 13, $I_L = 400\text{mA}$		3.9		
V_{REG} Regulated voltage	Pin 3	2.1	2.5	2.9	V
ΔV_{REG} Regulation	Pin 3 $3.5\text{V} \leq V_{CC} \leq 6\text{V}$ $R_{DB} = 0$		10		mV/V
	Pin 7 Minimum dead band		1		μs
	One shot temperature coefficient		.01		%/ $^\circ\text{C}$
Standby output voltage	Pin 9 and 13		2.5		V
PNP drive current	Pin 10 and 12		20		mA

SERVO AMPLIFIER

NE544/644

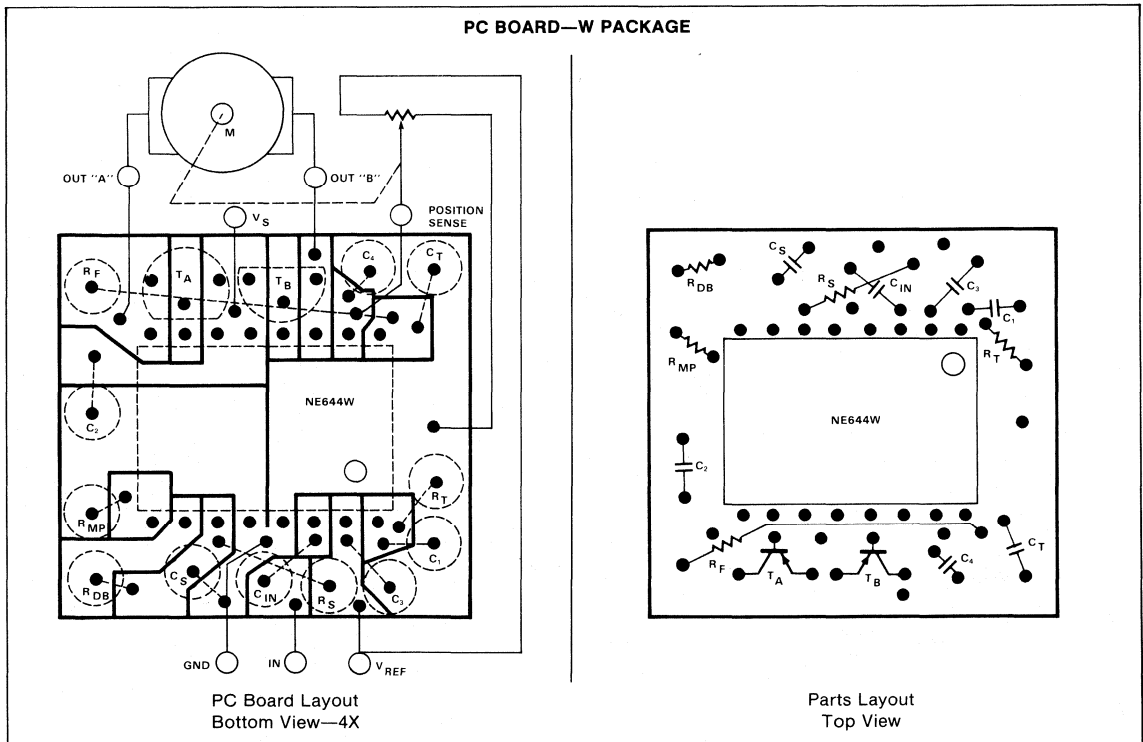
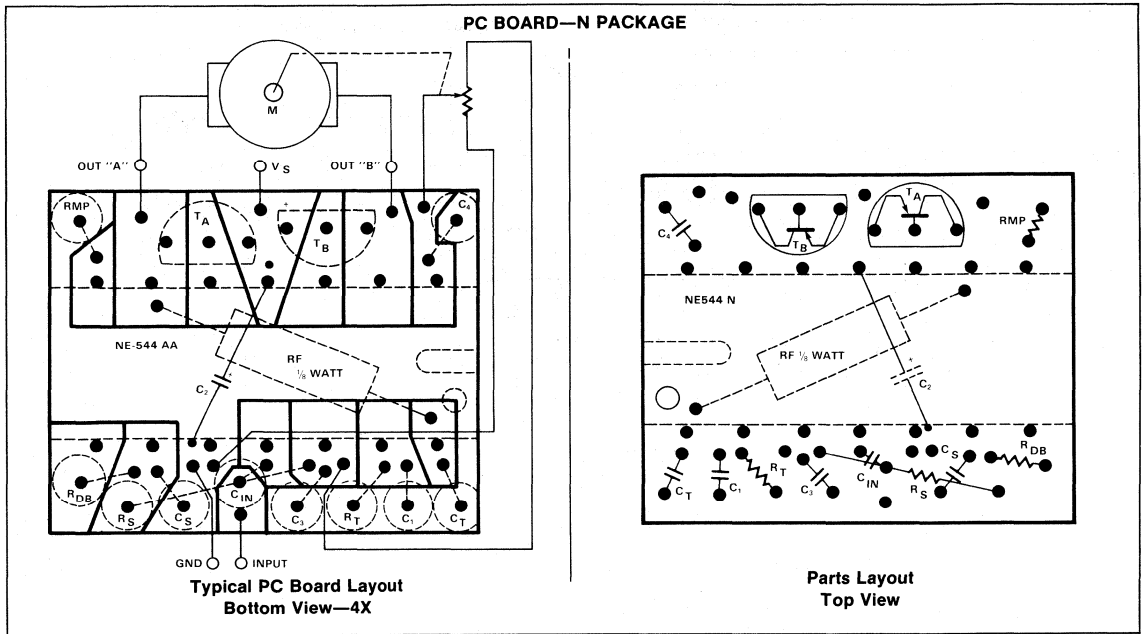
TYPICAL CONNECTION OF NE544N FOR LINEAR ONE SHOT TIMING



7

SERVO AMPLIFIER

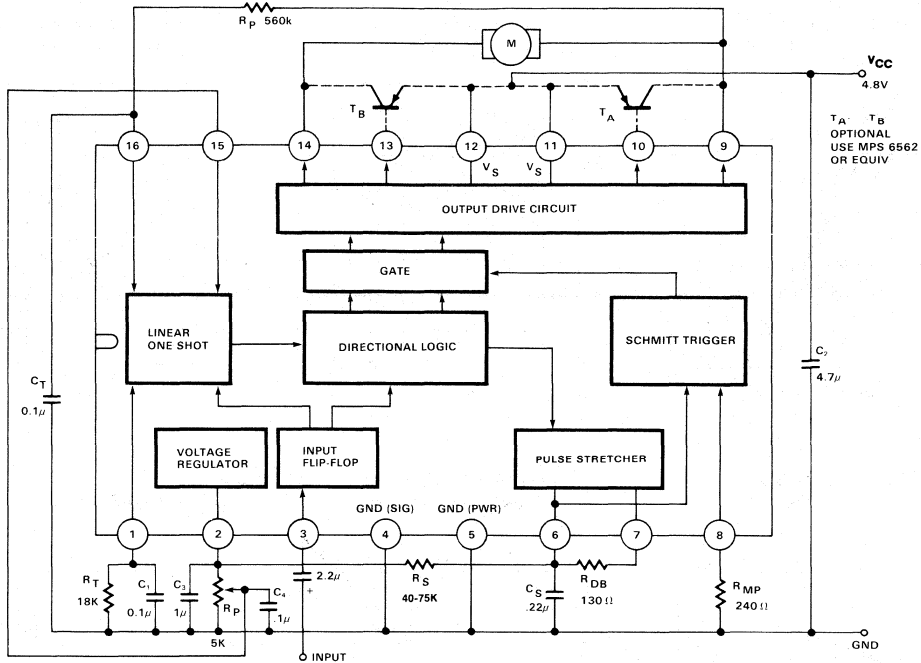
NE544/644



SERVO AMPLIFIER

NE544/644

TYPICAL CONNECTION OF NE644W AND NE644N FOR LINEAR ONE SHOT TIMING



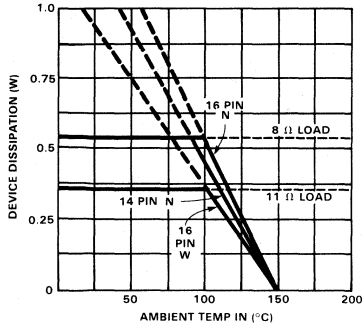
7

SERVO AMPLIFIER

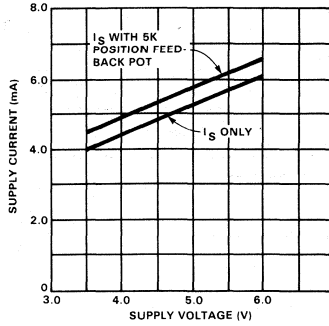
NE544/644

TYPICAL PERFORMANCE CHARACTERISTICS

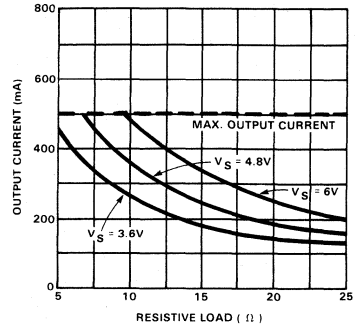
MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



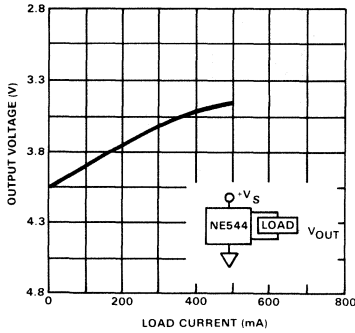
SUPPLY CURRENT vs SUPPLY VOLTAGE



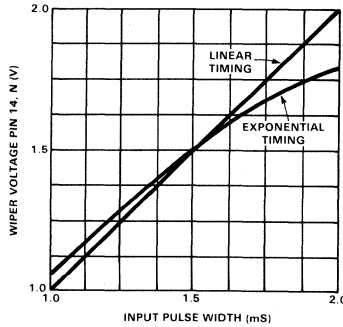
OUTPUT CURRENT vs LOAD RESISTANCE



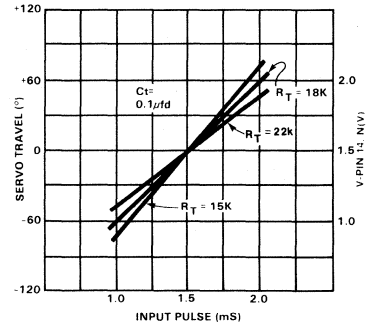
OUTPUT VOLTAGE vs LOAD CURRENT



INPUT PULSE WIDTH vs FEEDBACK POT OUTPUT



INPUT PULSE vs SERVO TRAVEL



PROGRAMMABLE SEVEN CHANNEL RC ENCODER

NE5044

DESCRIPTION

The NE5044 is a programmable parallel input, serial output pulsewidth encoder. A multiplexed dual linear ramp technique is used to allow up to 7 inputs to be converted to a serial pulsewidth modulated signal with excellent linearity and minimal crosstalk. Fixed or variable frame rates can be used, externally controlled, for ease of demodulation. An onboard 5V regulator eliminates power supply sensitivities and provides up to 20mA current capability for driving external loads.

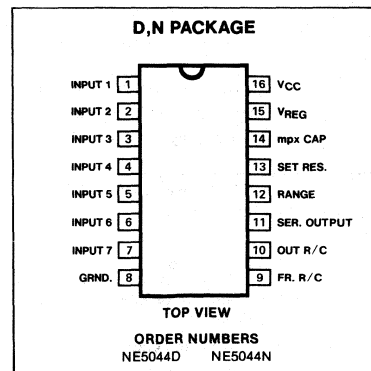
FEATURES

- 3 to 7 channels, externally selectable
- Constant current dual linear ramp for linearity better than .3%
- Internal voltage regulator for low drift
- Wide supply range 4.5 - 16V
- Fixed or variable frame rate set by external R-C
- External control for channel gain or range
- Versatile applications; exponential rates, mixing, dual rate, reversing etc.
- Compatible with all transmission mediums

APPLICATIONS

- Radio controlled aircraft, cars, boats, trains
- Industrial controllers
- Remote controlled entertainment systems
- Security systems
- Instrumentation recorders/controls
- Remote Analog/digital data transmission
- Automotive sensor systems

PIN CONFIGURATION



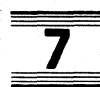
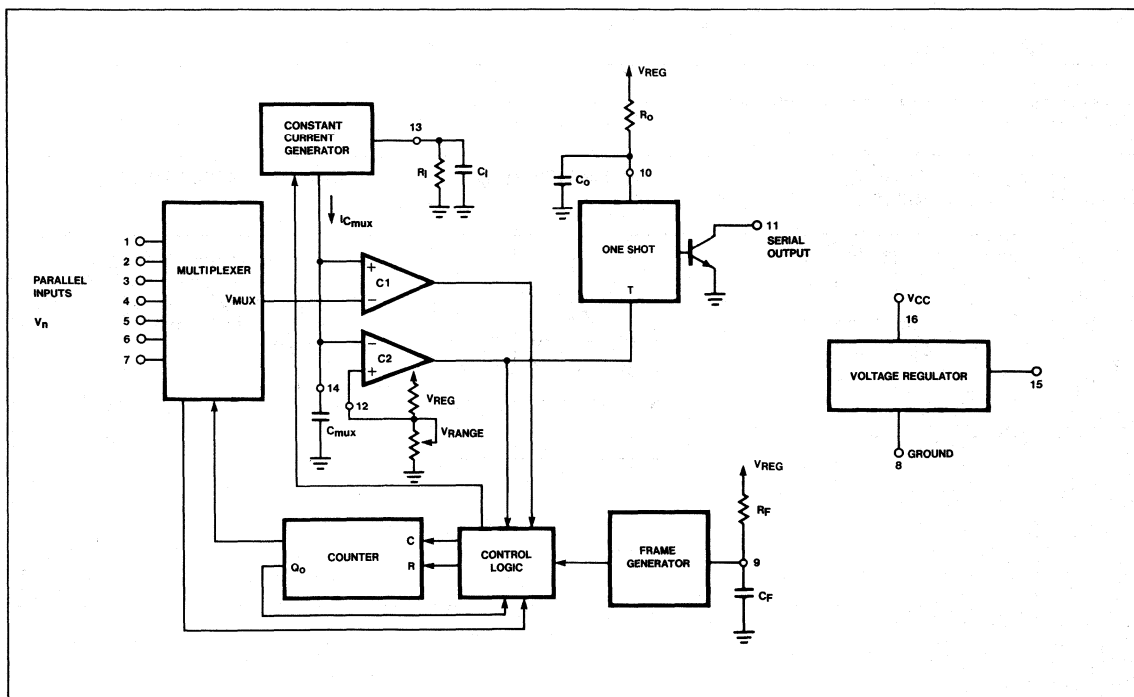
ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
V _{CC} , Supply voltage	17	V
Regulator output current	-25	mA
Serial output peak current	30	mA
Constant current generator	-1	mA
Parallel inputs, range input	0-V _{REG}	V
One shot input, frame generator input	0-V _{REG}	V
Operating temperature	-20 to +75	°C
Storage temperature	-65 to +150	°C

NOTE

1. T_A = 25° unless otherwise stated.

BLOCK DIAGRAM



PROGRAMMABLE SEVEN CHANNEL RC ENCODER

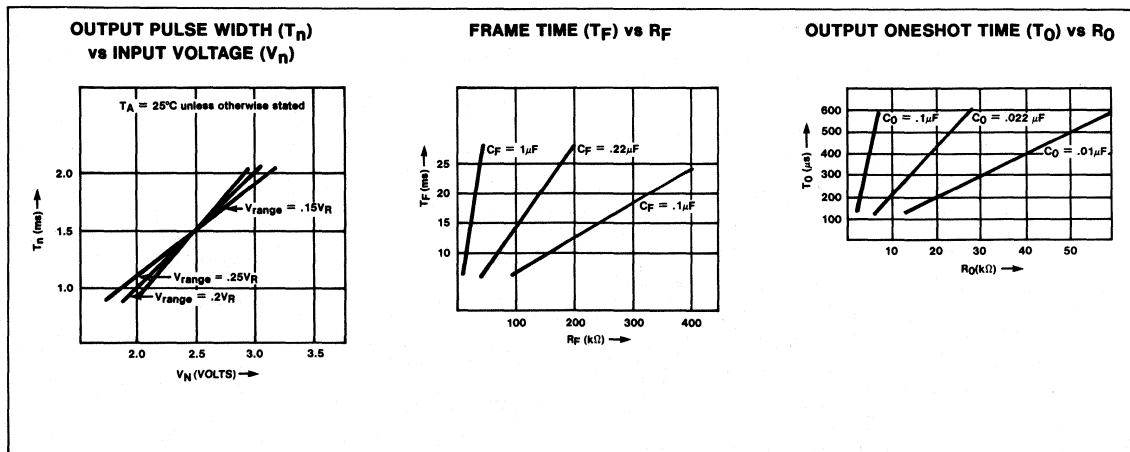
NE5044

DC ELECTRICAL CHARACTERISTICS Test conditions $T_A = 25^\circ\text{C}$, $V_{CC} = 10\text{V}$ using Test Circuit A unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE 5044			UNIT
		Min	Typ	Max	
POWER SUPPLY REQUIREMENTS ¹ Power supply voltage range Power supply current	Excluding control pots and serial output currents	4.5		16	V
			.11	15	mA
V _{REG} VOLTAGE REGULATOR Output voltage Output current Line regulation	$V_R \geq 4.5\text{V}$ $7 \leq V_{CC} \leq 16$	4.5	5.0	5.5	V
				-20	mA
			.005	0.2	V/V
MULTIPLEXER Input current Input voltage range Crosstalk	$V_n = 2.5\text{v}$ $V_n - V_{\text{Range}} \geq .75\text{V}$		± 30	± 200	nA
		1.5		5	V
			± 1	± 5	μs
T _n OUTPUT PULSE Position Position linearity error Position tempco Position PSR	$R_I \cdot C_{\text{mux}} = 1.25\text{ms}$ $V_n = .5V_{\text{REG}}; V_{\text{RANGE}} = .2V_{\text{REG}}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ $6\text{V} \leq V_{CC} \leq 16\text{V}$	1350	1500	1650	μs
			5		μs
			.15		$\mu\text{s}/^\circ\text{C}$
			.5	1	$\mu\text{s}/\text{V}$
T ₀ I ₁₁ Width Saturation voltage Leakage current Range input voltage Frame time (Fixed) Inhibit threshold	$R_0C_0 = 300\mu\text{s}$ $I_0 = 25\text{mA}$ $R_I = 50\text{k}\Omega$ $R_I = 25\text{k}\Omega$ $R_F C_F = 30\text{ms}$	240	285	330	μs
			.6	1	V
			.05	50	μA
			.75		V
			1.00		V
	17	20	23	ms	
		.4		V	

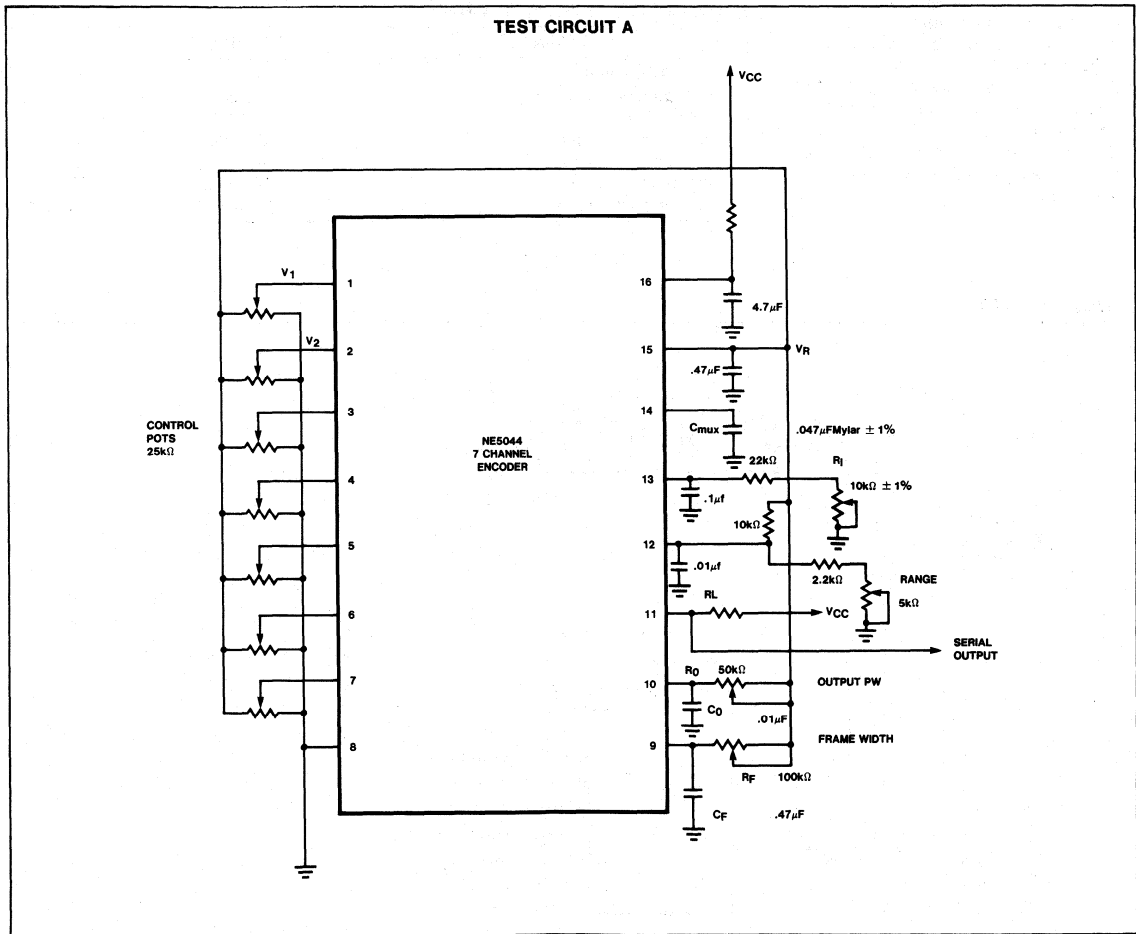
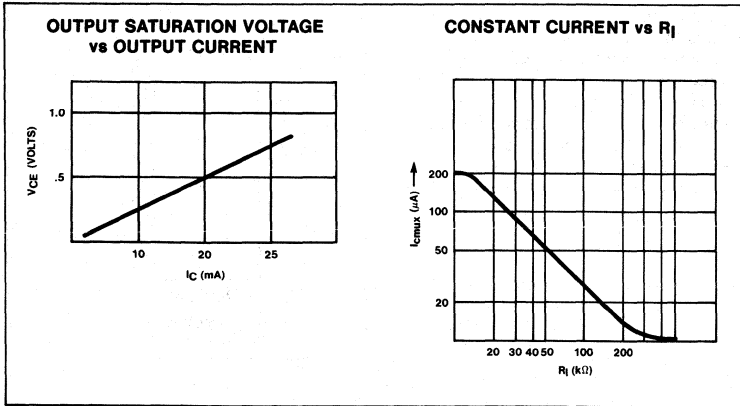
NOTE

1. At supply voltages exceeding 12 V, a current limiting resistor of 20 to 50 Ω in series with V_{CC} is recommended.



PROGRAMMABLE SEVEN CHANNEL RC ENCODER

NE5044



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SEVEN CHANNEL RC DECODER

NE5045

DESCRIPTION

The NE5045 is a serial input, parallel output, decoder intended for applications in pulse width or pulse position modulation systems. The serial input pulse, either positive or negative, is shaped and amplified before being fed to the counter/decoder. An integrating type sync. separator detects pulses greater than $T_w = R_3C_3$. The amplified input pulse triggers an internal one-shot (minimum pulse) which in turn clocks the counter-decoder, thereby enhancing system noise rejection. A missing pulse detector resets the decoder during the sync. pause. An internal voltage regulator supplies power for the radio receiver providing excellent isolation from the power supply as well as the decoder logic.

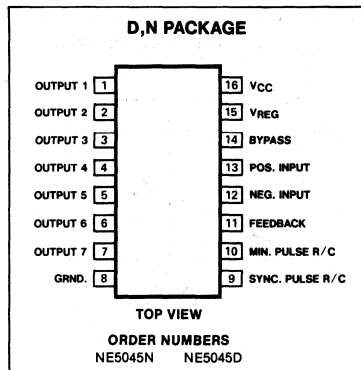
FEATURES

- Decodes up to 7 channels
- High gain input amplifier
- Externally set sync. pause and minimum pulse
- Wide supply voltage range, 3.6V-8V.
- Positive or negative pulse inputs
- Noise and flutter rejection
- Outputs reset to zero without inputs
- Compatible with all transmission mediums

APPLICATIONS

- Radio controlled aircraft, cars, boats, trains
- Industrial controllers
- Remote controlled entertainment systems
- Security systems
- Instrumentation recorders/controls
- Remote Analog/digital data transmission
- Automotive sensor systems

PIN CONFIGURATION

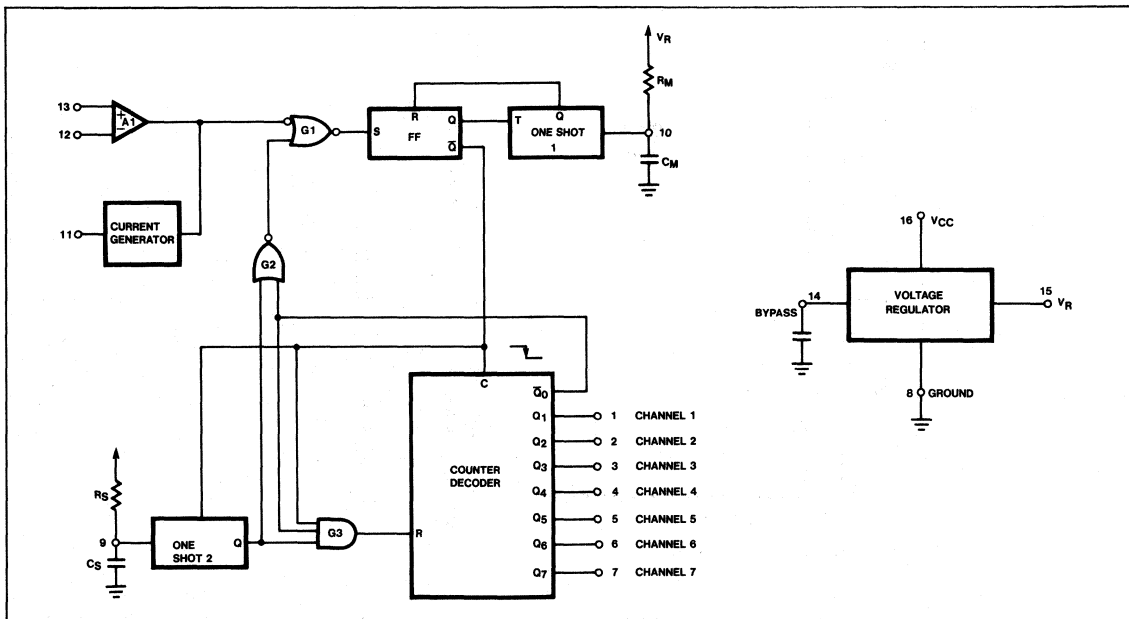


ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
V _{CC} , Supply voltage	10	V
Regulator output current	-25	mA
Decoded output current	±5	mA
Pause input voltage	0 to V _R	V
Input amplifier voltage	0 to V _R	V
Operating temperature	-20 to +75	°C
Storage temperature	-65 to +150	°C

NOTE
1. T_A = 25°C unless otherwise stated

BLOCK DIAGRAM



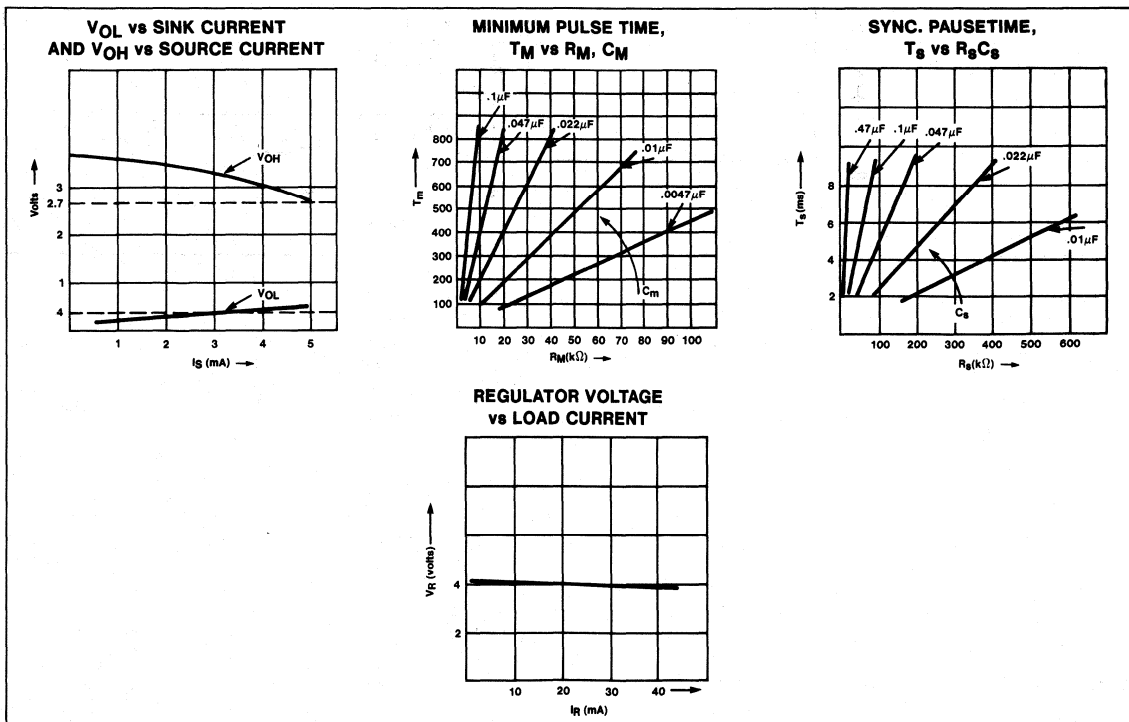
SEVEN CHANNEL RC DECODER

NE5045

DC ELECTRICAL CHARACTERISTICS Standard conditions: ($T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$ unless otherwise stated), using Test Circuit #1

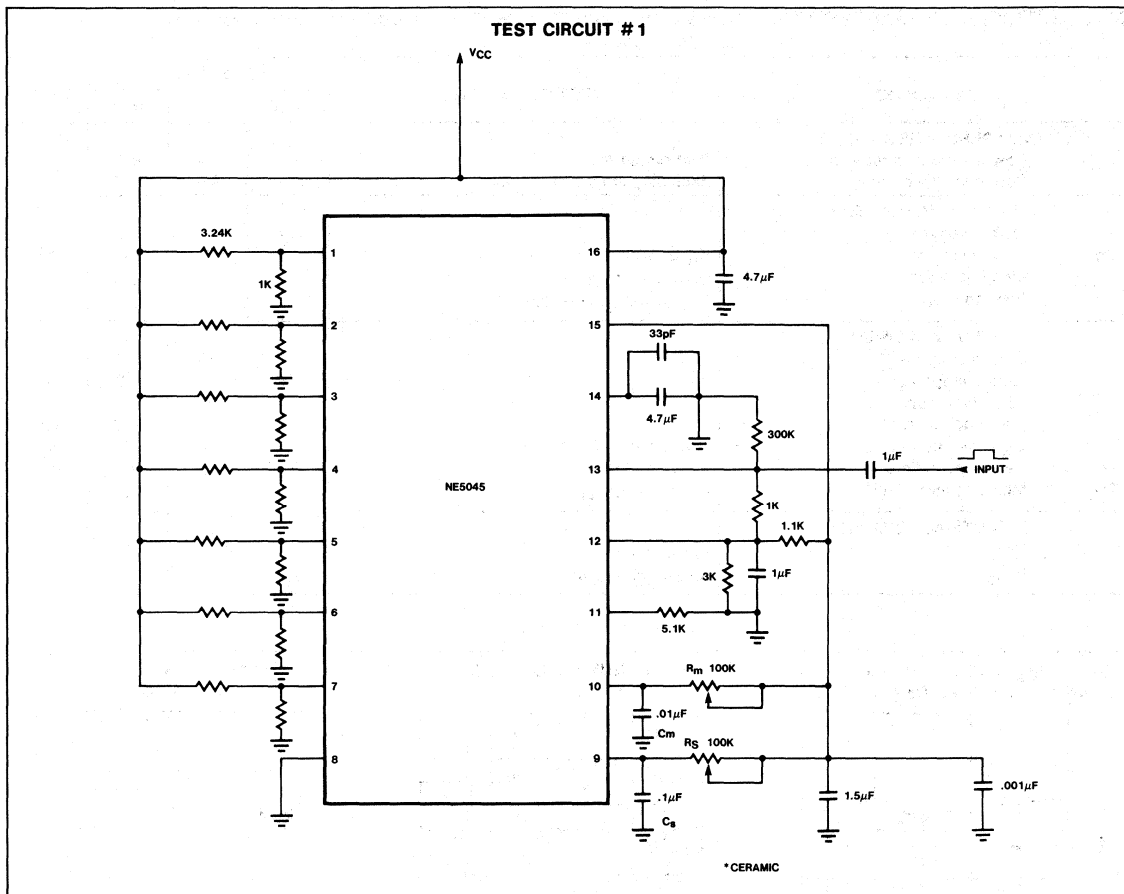
PARAMETER	TEST CONDITIONS	NE5045			UNIT
		Min	Typ	Max	
POWER SUPPLY REQUIREMENTS Power supply voltage range Power supply current	Test circuit #1 Excluding input bias current	3.6		8.0	V mA
V_R VOLTAGE REGULATOR Output voltage Output current Line regulation Voltage drop	$V_R \geq 3.7\text{V}$ $V_{CC} = 6\text{V to } 8\text{V}$ $V_{CC} = 4\text{V}$, $I_R = -10\text{mA}$	3.7	4.1	4.5 -15 .01 .05 1.3	V mA V/V V
T_S T_M INPUT AMPLIFIER Input bias current Input voltage range Open loop gain Feedback current Detection threshold Sync. pause time Minimum pulse time	Test circuit #1, $\Delta V_{12} \& 13$ $R_S C_S = 6.0\text{ms}$ $R_m C_m = 500\mu\text{s}$	2.0 100 5.1 405	10 60 200 8 6.0 475	100 4.0 400 20 6.9 545	nA V dB μA mV ms μs
OUTPUTS-ALL CHANNELS V _{OL} V _{OH}	I _{SINK} = 1mA I _{SOURCE} = 2mA	2.7	.25	.5	V V

7



SEVEN CHANNEL RC DECODER

NE5045



2 CHANNEL RC DECODER

NE5046

DESCRIPTION

The NE5046 is a serial input parallel output decoder designed for 2 channel digital proportional pulse width or pulse position modulation systems. The detection threshold is internally set and has hysteresis to prevent false triggering on noise. In a typical application, the serial input from the receiver is processed through an amplifier and pulse shaper, then converted to parallel output with a shift register. An internal sync separator detects the sync pause and clears the shift register. An internal voltage regulator provides power for the decoder and can be used to supply power for a radio receiver.

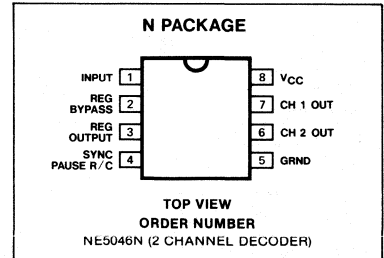
FEATURES

- High gain input amplifier with hysteresis
- Externally adjustable sync separator
- Wide supply voltage range 3.6V-8V
- Noise and flutter rejection
- Outputs reset to zero without input
- Compatible with all transmission mediums

APPLICATIONS

- Radio-controlled aircraft, cars, boats, trains
- Industrial controllers
- Remote-controlled entertainment systems
- Security systems
- Instrumentation recorders/controls
- Remote Analog/digital data transmission
- Automotive sensor systems

PIN CONFIGURATION

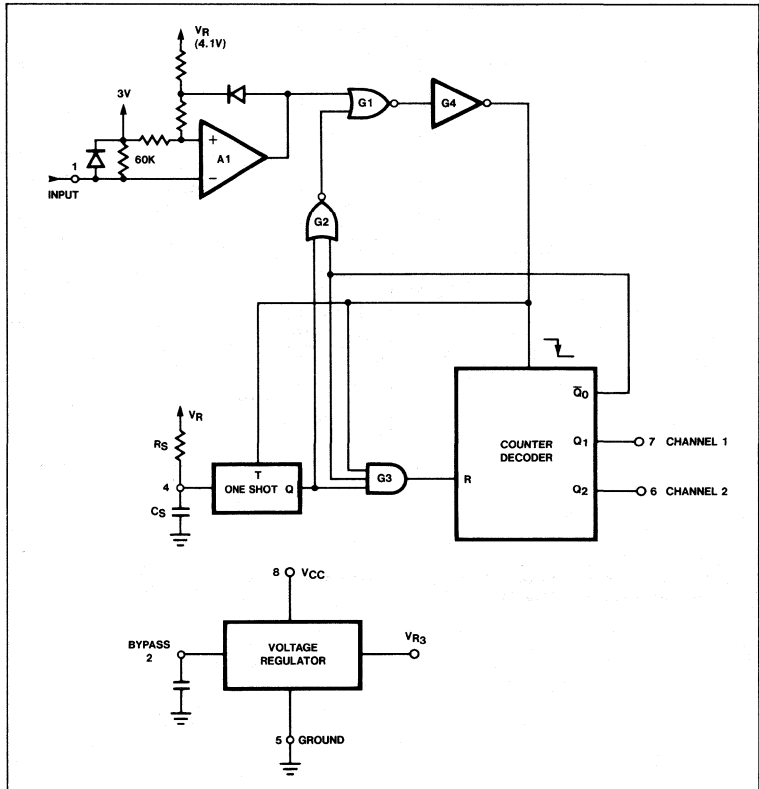


ABSOLUTE MAXIMUM RATINGS¹

PARAMETER	RATING	UNIT
V _{CC} , Supply voltage	10	V
Regulator output current	-25	mA
Decoded output current	±5	mA
Sync pause input	0 to V _R	V
Input amplifier voltage	0 to V _R	V
Input amplifier current	±1	mA
Operating temperature	-20 to +75	°C
Storage temperature	-65 to +150	°C

NOTE
1. T_A = 25°C unless otherwise stated.

BLOCK DIAGRAM



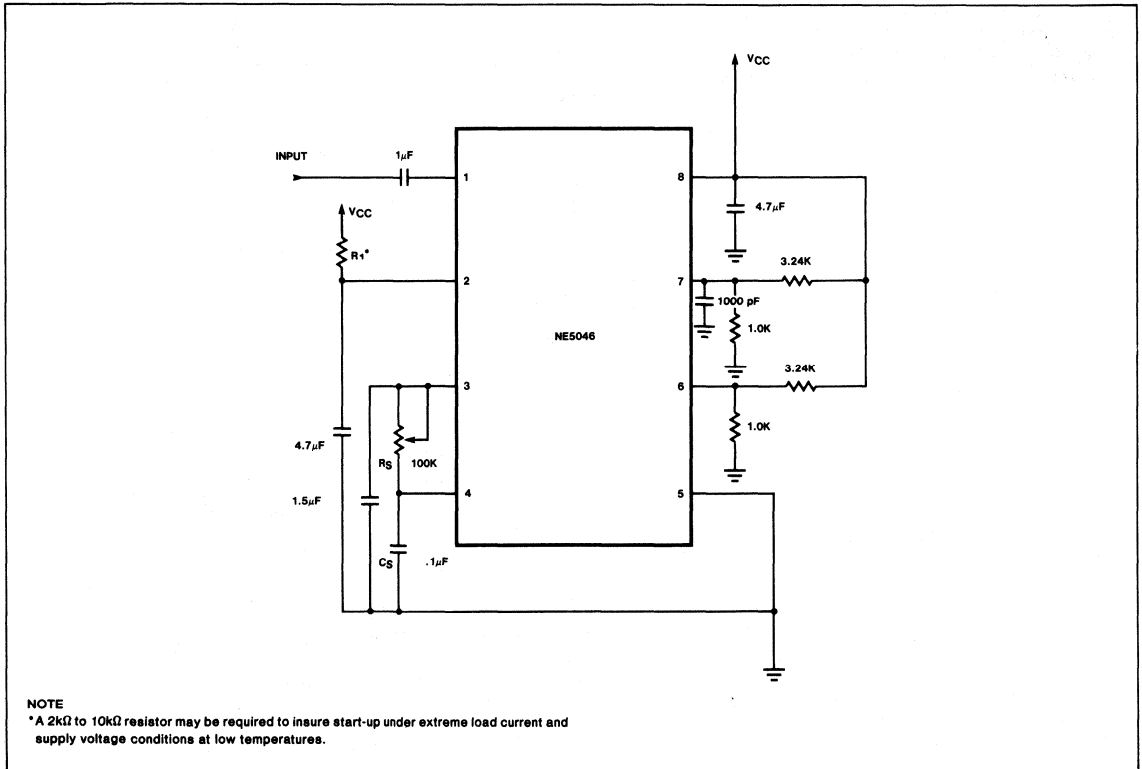
2 CHANNEL RC DECODER

NE5046

DC ELECTRICAL CHARACTERISTICS Test Conditions: $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, Test Circuit 1, unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE5046			UNIT
		Min	Typ	Max	
V_{CC} supply voltage		3.6	5.0	8.0	V
Power supply current			6.0	9.0	mA
Regulator output voltage	$V_R \geq 3.6\text{V}$	3.0	4.1	4.5	V
Regulator output current					-15
Regulator line regulation	$V_{CC} = 6\text{V to } 8\text{V}$ $V_{CC} = 4\text{V}$, $I_R = -10\text{mA}$.01	.05	V/V
Regulator voltage drop					1.0
Input threshold voltage	$R_S C_S = 6\text{ms}$.15			V
Sync. pause time			5.1	6.0	6.9
Output voltage both channels	$I_{\text{SINK}} = 1\text{mA}$ $I_{\text{SOURCE}} = 2\text{mA}$.25		V
V_{OL}				.5	V
V_{OH}			2.7		

TEST CIRCUITS



LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

DESCRIPTION

The NE/SE5520 is a signal conditioning circuit for use with Linear Variable Differential Transformers (LVDT). The chip includes a low distortion amplitude stable sine wave oscillator with programmable frequency to drive the primary of the LVDT; a synchronous demodulator to convert the LVDT output amplitude and phase to position information; and an output amp to provide gain and filtering.

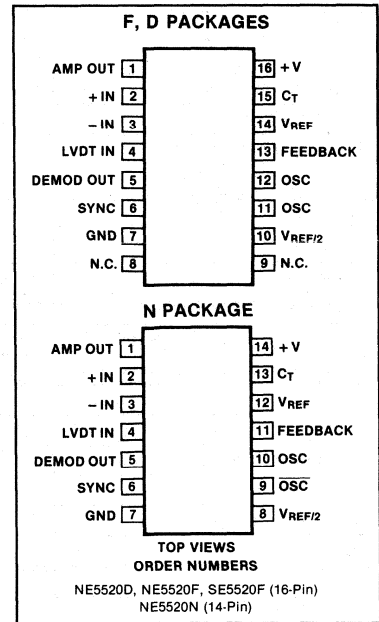
FEATURES

- Oscillator frequency: 1kHz to 20kHz
- Low distortion < 5%
- Capable of ratiometric operation
- Single supply operation 5 to 25V or dual supply ± 5 to $\pm 12V$
- Low power consumption

APPLICATIONS

- LVDT signal conditioning
- RVDT signal conditioning

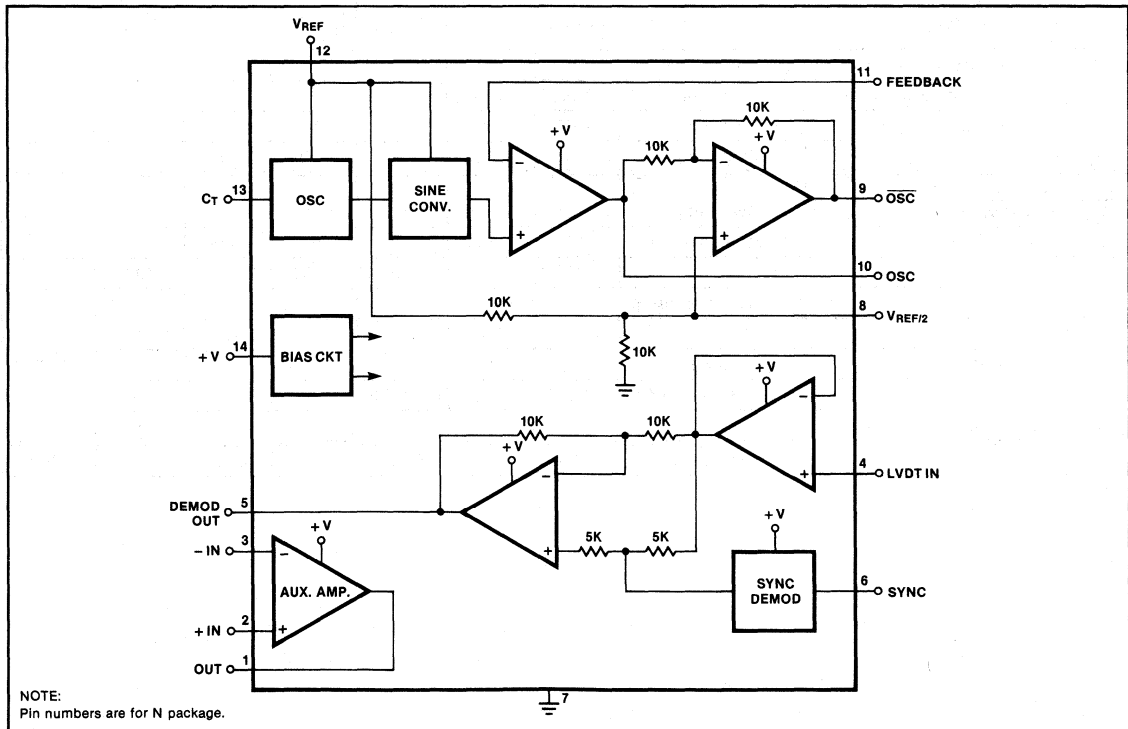
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+ 30	V
Split supply voltage	(± 15)	V
Operating temperature range		
SE5520	- 55 to + 125	$^{\circ}C$
NE5520	0 to + 70	$^{\circ}C$
Storage temperature range	- 65 to 150	$^{\circ}C$

BLOCK DIAGRAM



LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_R = V_+ = 10\text{V}$ unless otherwise specified.

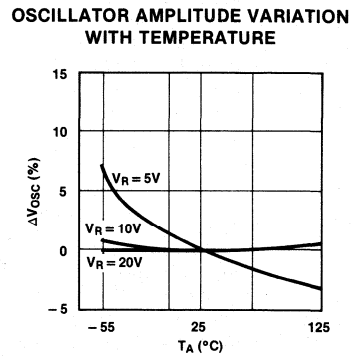
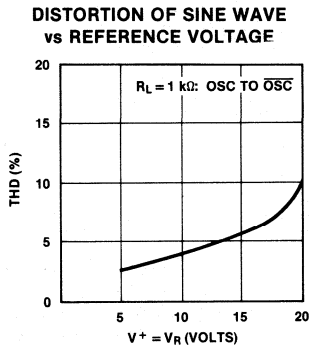
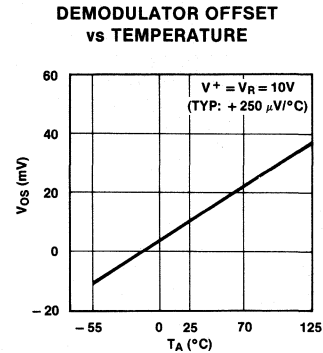
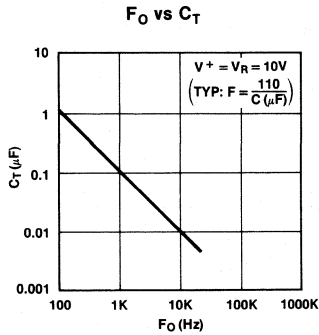
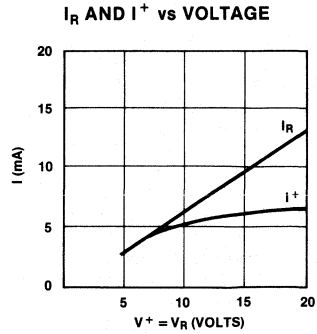
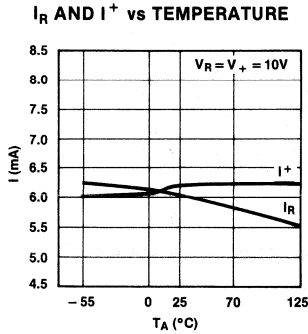
PARAMETER	TEST CONDITIONS	SE5520			NE5520			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage range	Over temp.	5		25	5		25	V
Supply current	Over temp.		7.0	9		7.0	8.5	mA
Reference current	Over temp.		5.5	8.0		5.5	7.0	mA
Reference voltage range	Over temp.	5		V+	5		V+	V
Oscillator section								
Oscillator output			$\frac{V_R}{8}$			$\frac{V_R}{8}$		Vrms
Sine wave distortion	Over temp.		3.5	5		3.5	5	%
Initial amplitude error			0.5	1.0		0.5	1.0	%
Tempco of amplitude error				0.05			0.05	%/°C
Voltage coef. of amplitude error				0.05			0.05	%/V
Voltage coef. of ratiometric error	Over temp.	0.99		1.01	0.995		1.005	V/V
Initial accuracy of osc. frequency			10	20		10		%
Tempco of frequency error			0.05	0.1		.05		%/°C
Voltage coef. of frequency			10	15		10		%/(V _R)
Frequency range	$C_T = 0.005$ to $0.1\mu\text{F}$	1		20	1		20	kHz
Oscillator output load		1			1			kΩ
Demodulator section								
Linearity error	Over temp.		0.05	0.1		.05		%
Maximum demodulator input	Over temp. range	$\frac{V_R}{2} - 0.5$		$\frac{V_R}{2} + 0.5$	$\frac{V_R}{2} - 0.5$		$\frac{V_R}{2} + 0.5$	V
Demodulator offset voltage	Over temp. range			50			65	mV
Tempco of demodulator offset	Over temp.	0.20	0.25	0.30		0.25		mV/°C
Demodulator input current	Over temp.	-500	-300		-500	-300		nA
$V_R/2$ accuracy	Over temp.	-3	± 0.5	+3	-3	± 0.5	+3	%
Output amplifier								
Input offset voltage	Over temp.	-7.5		+7.5	-10		10	mV
Input bias current	Over temp. range	-500	-300		-500	-300		nA
Input offset current		-100		100	-100		100	nA
Gain	$R_L = 10\text{k}\Omega$ over temp.	90	108			100		dB
Slew rate			1.5			1.5		V/ μsec
Gain bandwidth	$A_V = 1$		1			1		MHz
Output voltage swing	$R_L = 10\text{K}$ over temp.	1.5		V+ - 1.5	1.5		V+ - 1.5	V
Output short circuit current				25			25	mA
Oscillator current	Over temp.	0.095	0.12	0.15		0.12		mA/V-V _R

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

TYPICAL PERFORMANCE CHARACTERISTICS



7

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

ALL PIN NUMBERS REFER TO N PACKAGE

INTRODUCTION

An LVDT is an electromechanical transducer which makes possible the measurement of very small motion in a structure or mechanical device. Mechanical motion is translated to an electrical signal which contains position information much as a radio frequency carrier contains sound information. The position information from the LVDT is contained in the phase and amplitude of the output AC waveform. In order to remove the position information (demodulation), a system such as is shown in block form in Figure 1 must be used. Once signal demodulation is achieved the position data may be read out on a meter or digital display in addition to being processed by microprocessor or computer. The Signetics NE5520 is a new *Monolithic LVDT Driver-Demodulator* designed to interface with most LVDT's presently being used in the industry.

Uses will range over a large number of potential applications including the accurate measurement of position, pressure, load weight, angular position and even acceleration. Historically, LVDT's have been used in the following applications:

- Load cell
- Linear motion
- Torque cell
- Vibration
- Fluid pressure
- Accelerometer
- Inclinator
- Seismic load cell

MOTION MAY-BE

- Linear
- Rotary

The NE5520 provides sinusoidal drive to the Linear Variable Differential Transformer (LVDT), the output of which is buffered, rectified and phase demodulated to obtain both direction and displacement information in the form of a DC output signal (Figure 2).

LVDT LOADING

Due to the loosely coupled characteristics of the typical LVDT, loading effects versus frequency may be critical to a successful design. The graph (Figure 3A) shows this relationship in the form of a family of curves relative to LVDT core displacement for 400Hz and 2500Hz. From the curves it is obvious that the linearity and output level versus displacement is superior for an LVDT operated at 2000Hz with a very high impedance load (0.5 meg ohm). The

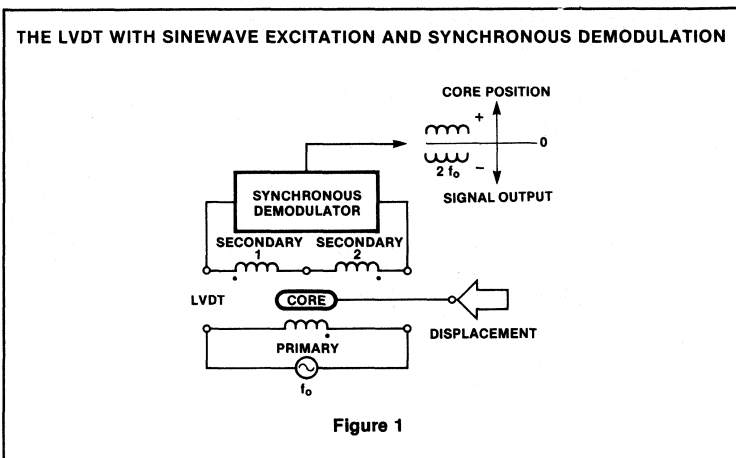


Figure 1

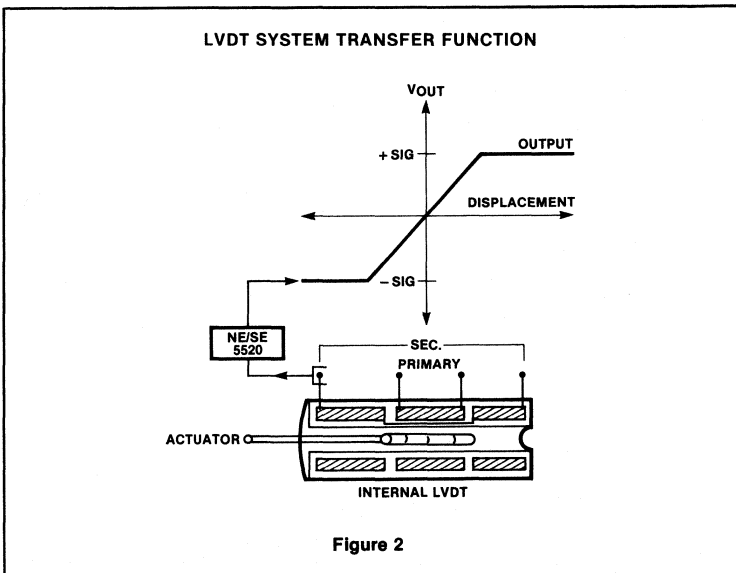


Figure 2

NE/SE5520 demodulator presents a very high input impedance to the LVDT secondary for maximum linearity. (Fig. 3B)

LVDT INTERFACING: SIGNAL CONDITIONING IS REQUIRED

In order to obtain usable information from the LVDT a series of signal conditioning circuit operations are required. First, a stable source of constant frequency ex-

citation voltage must be applied to the primary of the LVDT.

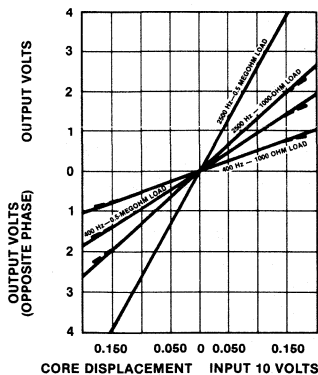
Next some form of demodulator is needed to extract position information from the LVDT secondary output signal. A full wave rectifier will provide usable amplitude information when adequately filtered, however, relative phase information is lacking. In order to obtain both phase and amplitude information synchronous demodulation is needed. This type of demodulator

LVDT SIGNAL CONDITIONER

NE/SE5520

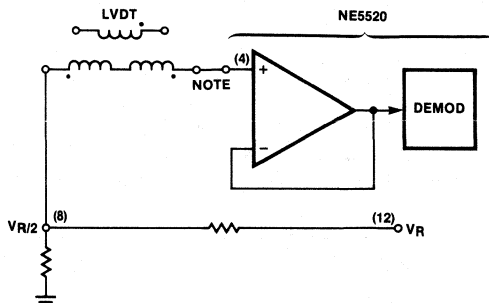
Preliminary

OUTPUT CHARACTERISTICS OF A TYPICAL LVDT FOR VARIOUS LOADS AND EXCITATION FREQUENCIES



BY PERMISSION SCHAEVITZ ENGINEERING
"HANDBOOK OF MEASUREMENT AND CONTROL" BY HERCEG.

Figure 3a



NOTE: INTERNAL BUFFER AMP PROVIDES HIGH IMPEDANCE LOAD TO SECONDARY.

Figure 3b

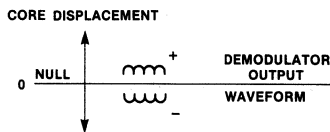


Figure 3c

exists in the Signetics NE5520. Once phase and amplitude information is obtained in the form of a polar full wave rectified signal (see Figure 3C) from the synchronous demodulator, the carrier component (actually 2nd harmonic of the carrier plus higher order spectral components) must be filtered out leaving only the true position information. This is accomplished by passing the demodulated signal through a low-pass active filter. An auxiliary operational amplifier is provided for this purpose within the NE5520, in addition to adjustable signal gain for proper full scale output (span adjustment). In addition, DC offsets are nulled by a simple offset adjustment at the auxiliary amplifier. The resulting system is a complete LVDT signal conditioner. Figure 4 shows a block diagram of the NE5520. The device

will operate in a single supply range from 5 to 25 volts DC or with split supplies of ± 5 to ± 12 volts DC. A device current, I_{CC} , of 10 milliamperes at an operating voltage of 10 volts is typical.

DESCRIPTION OF THE NE5520 (Figure 4)

The NE5520 oscillator consists of a triangle wave generator, a current source-sink circuit which switches when the capacitor voltage reaches discrete levels at $1/4$ and $3/4 V_{REF}$. The total swing being $V_{REF/2}$ volts p-p. The triangle wave is fed into a non-linear load which generates a sinusoidal waveform with low distortion. The sine wave output is then buffered by two op amps, the output of which appear on pins 9 and 10 in phase opposition. This

then is the excitation signal for the LVDT primary.

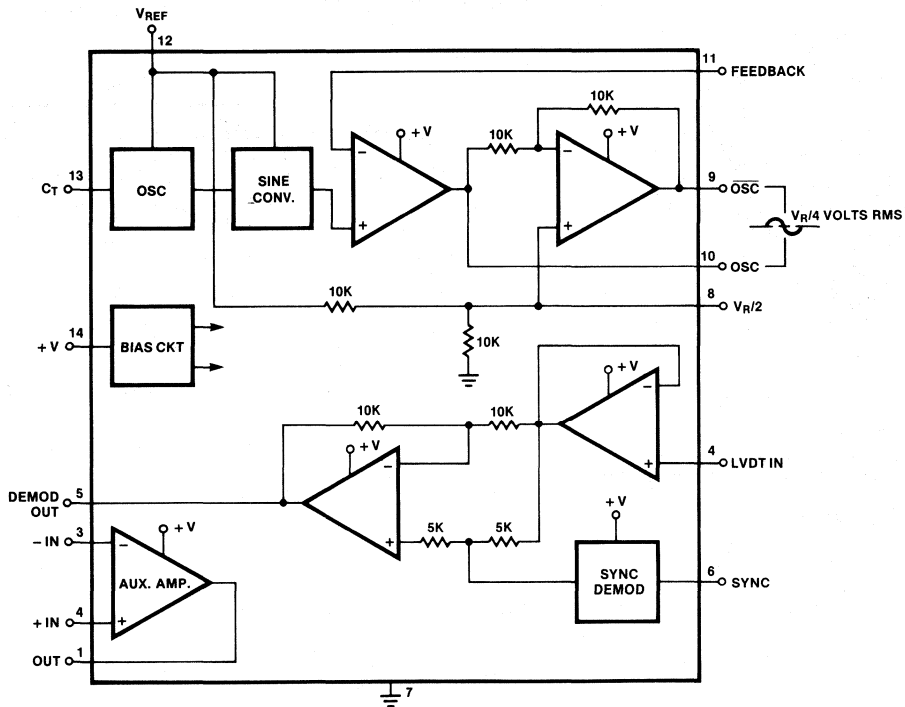
The second major functional portion of the NE5520 is the synchronous demodulator and this section performs full wave rectification in phase synchronism (pin 6) with the above oscillator output. In order to extract true position information, the phase relationship of the LVDT secondary must be obtained. This means that as the LVDT core passes through null an abrupt 180° phase change occurs. Once full wave rectification is accomplished, the resulting signal carrier frequency must be removed by filtering. Demodulator output appears on pin 5. This is accomplished by an active filter incorporating the auxiliary op amp (pins 1, 2, 3). The original position information then appears ripple free on pin 1 of the auxiliary amplifier.

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

BLOCK DIAGRAM



NOTE:
Pin numbers for N package.

Figure 4

Other functions include buffer amplifier feedback in the oscillator circuit. The loop is closed with negative feedback around both amplifiers (pin 10 to 11) operating at unity gain.

The oscillator timing capacitor controls the frequency as shown in the graph, Figure 5. The frequency is related by the equation $f_{OSC} = 110/C_{t\mu F}$. Absolute output frequency will vary slightly with supply voltage.

BIASING THE REFERENCE VREF (PIN 12)

The manner in which the V_R pin is biased will effect the output voltage function of the NE5520 and consideration must be given to this in order to arrive at an optimum system design. There are two basic modes of operation involved as listed below:

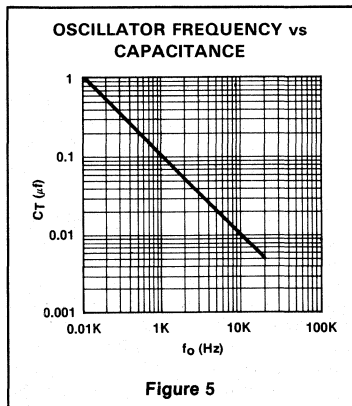


Figure 5

- 1) Ratiometric
- 2) Fixed Reference

With the *ratiometric mode*, pin 12 (V_{REF}) is

connected to pin 14 (+V). Since V_R controls the DC common mode voltage of the demodulator and the oscillator rms output, these magnitudes will now change with supply voltage. The DC output from pin 1, using a single ground referenced supply, will be ratiometric with the supply voltage and centered within the common mode range of the output amplifier when the LVDT transducer is at null. Single or dual supply operation will be ratiometric when +V is connected to V_R .

The alternate method of biasing is the *fixed reference* mode with pin 12 (V_R) connected to a fixed reference voltage such as +10 volts and pin 14 (+V) allowed to vary with an incoming poorly regulated supply. This might occur in automotive applications where battery voltage may vary from 10 to 14 volts. However, with a fixed reference driving V_R , DC voltage at the output will not vary with supply but will vary within the common mode limits

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

of the amplifier as the LVDT core traverses its path. Output voltage of pin 1 at LVDT null will be $V_R/2$. Thus, for the case mentioned with $V_R = 10$ volts, the null voltage will be +5 volts. The maximum linear swing would be 1.5-8.5 volts around this value. The fixed reference mode may be used with single or dual supply operation.

DUAL SUPPLY OPERATION

When connected to a typical LVDT transducer as shown in Figure 6, the NE5520 will exhibit an extremely linear transfer function. Very important to precision position measurement is the inherent repeatability of the system. The graphs in Figure 7A, B illustrate the highly linear transfer function and its repeatable accuracy with different supply voltages, in this case ± 6 and ± 10 volts. The transducer motion was over a range of ± 150 milli-inches each side of the LVDT null. Typical DC output signal is shown with an output amplifier gain of X10 in both cases. Note that linearity remains constant, however, full scale output varies with supply voltage. This is due to the increased excitor drive to the LVDT with increased supply voltage. LVDT output is a linear function of excitor amplitude on the primary winding. The addition of a single gain control may easily be added between pins 1 and 3 to reduce gain in order to retain constant output for different supply voltages (see Figure 8) or V_R may be connected to a fixed voltage. (See 'Biasing.')

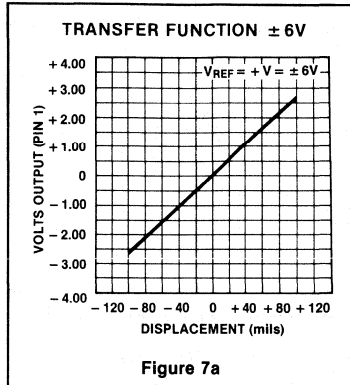


Figure 7a

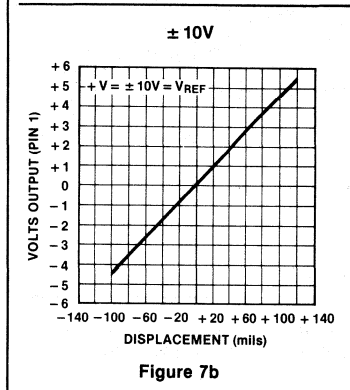


Figure 7b

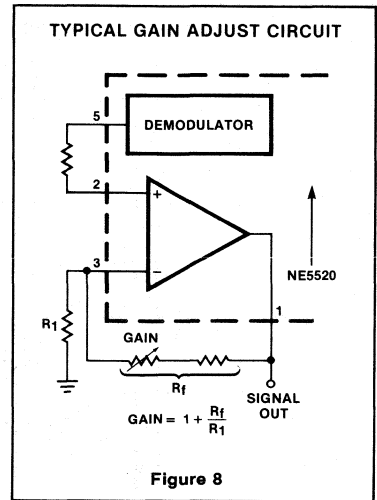


Figure 8

It is strongly recommended that dual output tracking regulated supplies be used in this type of application in order to minimize system DC offset and impaired measurement accuracy due to power supply unbalance. An optional circuit capable of automatically tracking and nulling power supply offset is shown in Figure 9. The bipolar output signal is referenced to ground.

7

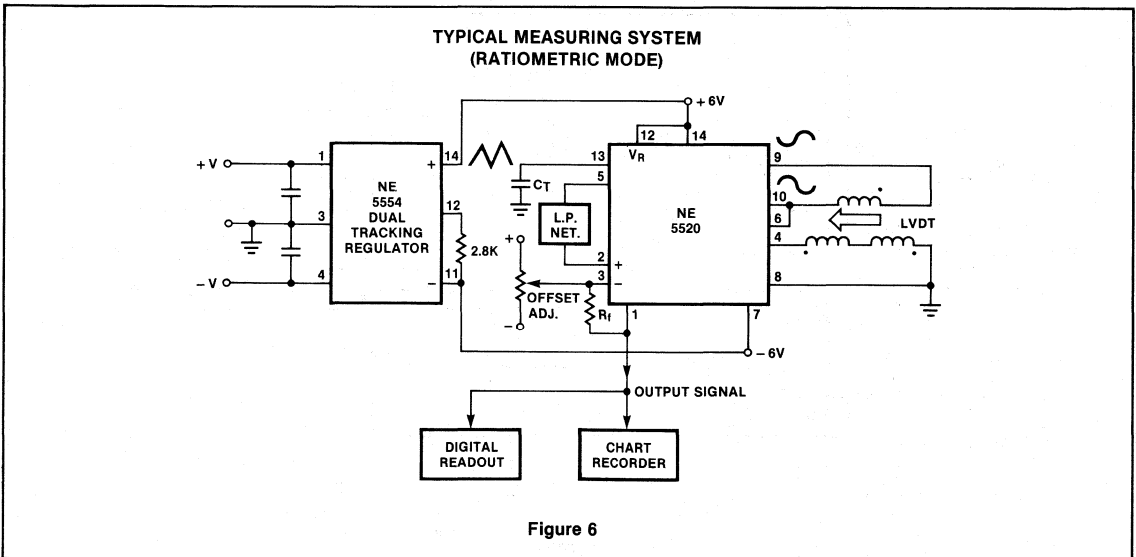
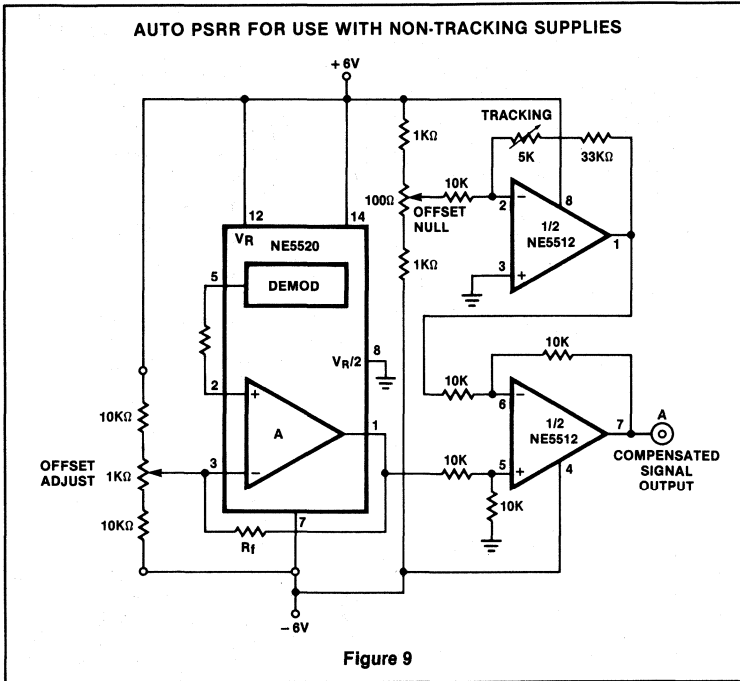


Figure 6

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

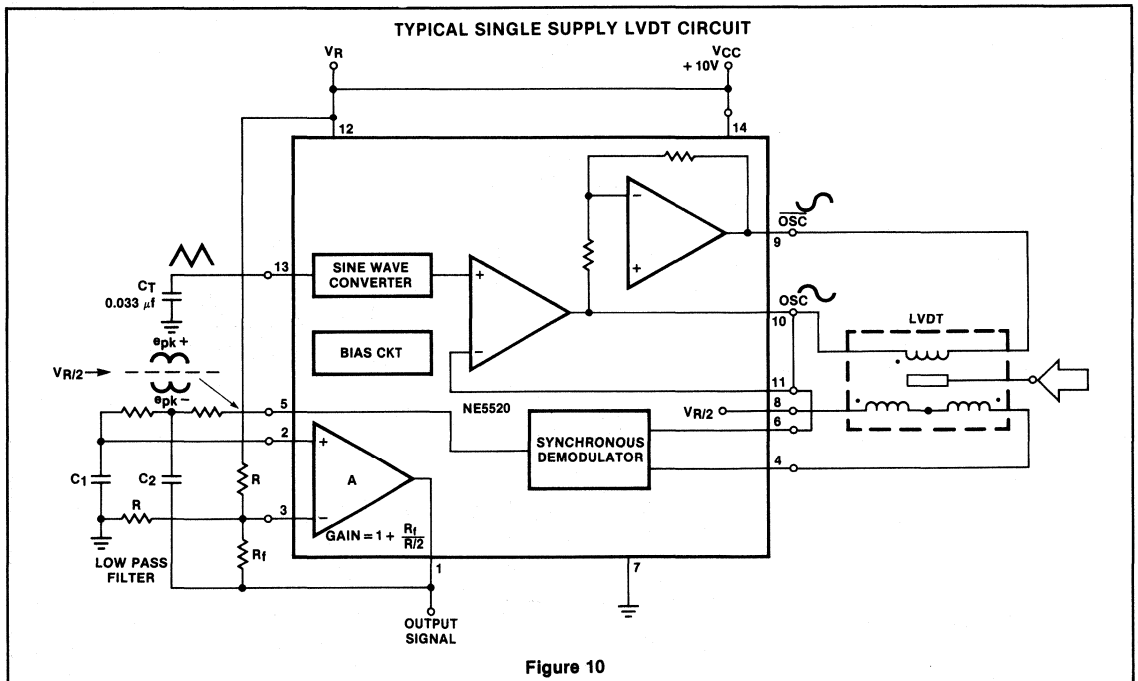


NULLING PROCEDURE (Ref Fig. 9)

1. Null transducer position by observing pin 4 waveform. Set supply voltage for ± 6.00 volts.
2. Set offset adjust pot (feeds pin 3 of NE5520) for 0.00 volts and DC at pin 1 of NE5520.
3. Adjust offset null pot (NE5512) for zero output on Terminal A.
4. Check for equal voltage \pm deflection when transducer is displaced equal distances from physical null position.
5. Adjust tracking control for minimum DC output change when either supply is varied over operating range at 'A'.

SINGLE SUPPLY OPERATION

Single ended supply operation requires a different circuit approach to obtain measurement system interface. Figure 10 shows a typical circuit using a single 10-volt supply. Note that the output (pin 1) of the NE5520 is now floating above ground at approximately $V_R/2$. Simple measuring circuits may be realized (Figures 11A, B, C) by placing a DC microammeter between pin 1 and a resistive divider



LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

creating a bridge readout which is ratio-metric with supply voltage variations. In case more precision is necessary, a buffer amplifier may be added between the voltage divider or $V_R/2$ and the readout circuit in order to minimize offset due to measuring circuit loading. DC offset due to internal tracking error in the NE5520 may be reduced by using the nulling circuit shown in Figure 12. Offset sensitivity and its effect on system accuracy will be inversely proportional to full scale signal output of the NE5520 which is a function of the DC gain of the auxiliary amplifier and LVDT output. A typical full scale output with 10-volt supply operation is $V_R/2 \pm 3.5$ volts with gain equal to 10.

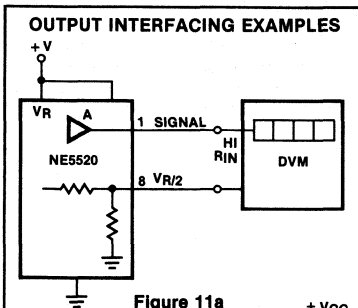


Figure 11a

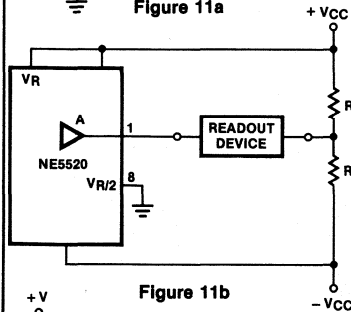


Figure 11b

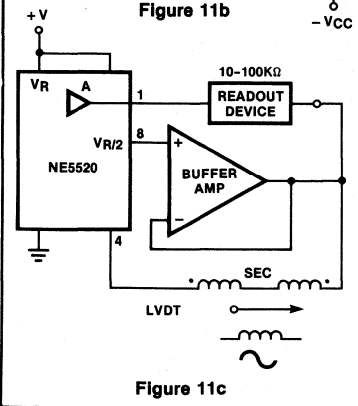


Figure 11c

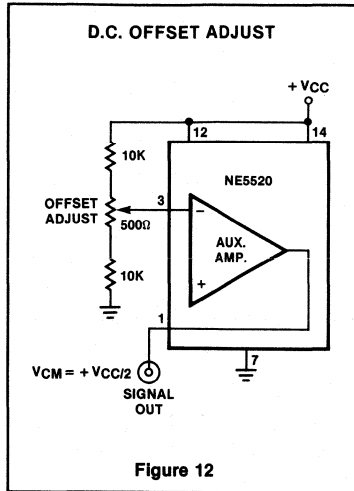


Figure 12

MATCHING THE NE/SE5520 TO LOW IMPEDANCE LVDT'S

The NE5520 exciter output is capable of driving LVDT primary windings with a minimum impedance of 1K ohm. When a significantly lower impedance primary is driven by the device some form of step-down impedance matching or a power buffer is recommended. Figure 13 shows a step-down matching transformer approach. A transformer with primary impedance of approximately 1K ohm (audio type) with the proper secondary impedance to match the LVDT primary is used to couple

oscillator excitation. Depending on the output efficiency of the LVDT, output signal losses may occur with a corresponding loss in measuring sensitivity. The auxiliary amplifier gain may be increased to offset this loss.

A second approach makes use of a power buffer amplifier constructed from discrete transistors (2N2222, 2N3644). This circuit (Figure 14) results in less signal loss and is inexpensive. A DC decoupling capacitor must be used to prevent DC offset currents from flowing in the LVDT primary winding. A 3dB signal reduction is noted when driving a 15-ohm load to 6 volts peak to peak (10-volt operation); and 12 volts peak to peak for 20-volt supply.

NE5520 TEMPERATURE COMPENSATION

Internal offset voltages originating in the NE5520 synchronous demodulator require external compensation to obtain best measurement accuracy when operating over the full temperature range. The circuits shown (Figures 15A, B) give a simple approach using a thermistor inserted in series with the offset null resistors to reduce voltage drift to a reasonable level. These tolerances are based on ± 3.5 volts full scale output for LVDT displacements each side of physical null. A thermistor having a positive coefficient of $+0.7\%/^{\circ}\text{C}$ is used. Obviously, if the total divider resistance is changed a different thermistor resistance will be required.

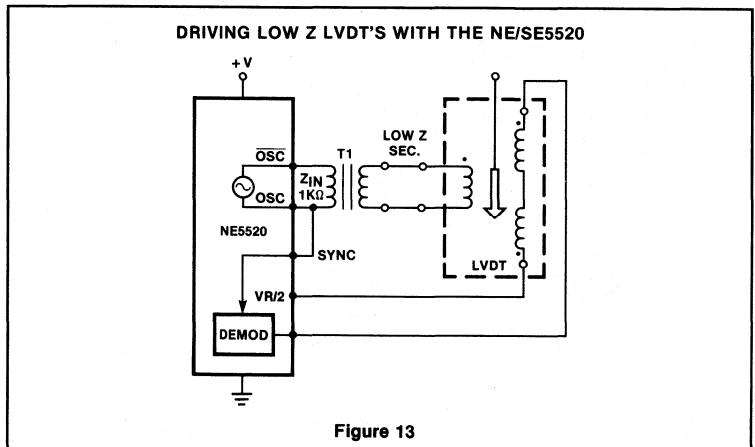
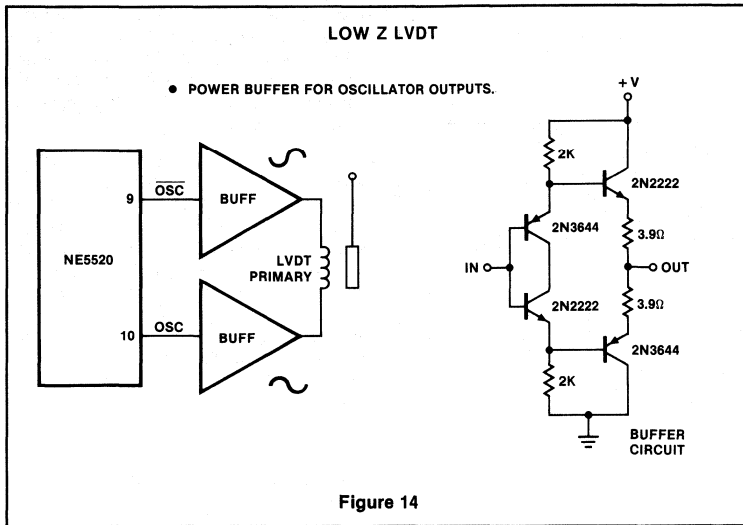


Figure 13

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

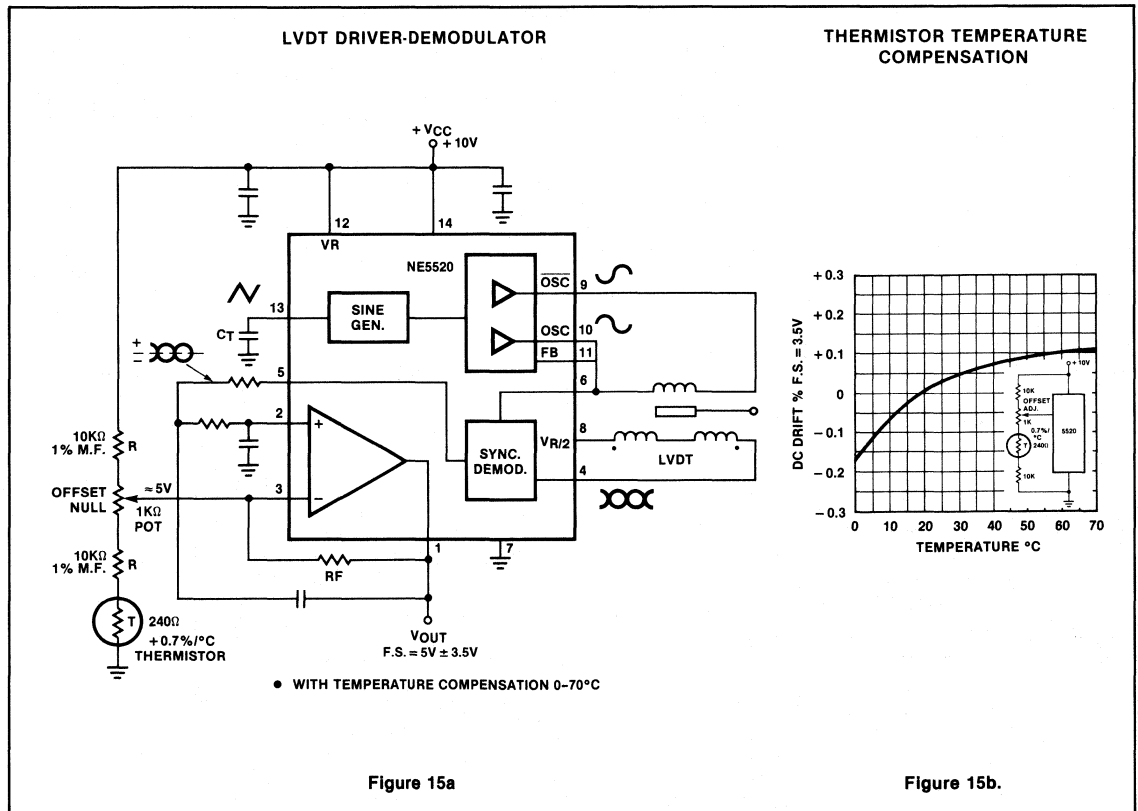


DEMODULATOR DISTORTION (OVERDRIVE)

When the demodulator input exceeds 2 volts peak to peak clipping distortion will increase and must be avoided by controlling oscillator drive to the primary of the LVDT. Figure 16 shows an example of a circuit for attenuating primary excitation using a 1K ohm potentiometer.

The procedure for adjusting the level is simply to:

1. Set LVDT core position for maximum output from the secondary.
2. Monitor the waveform on (pin 5 demodulator output) and adjust oscillator level for the amplitude just below clipping. Normally this should result in a maximum of 2 volts peak to peak at pin 4 of the NE5520 (25°C).



LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

LVDT MEASURING GAUGE

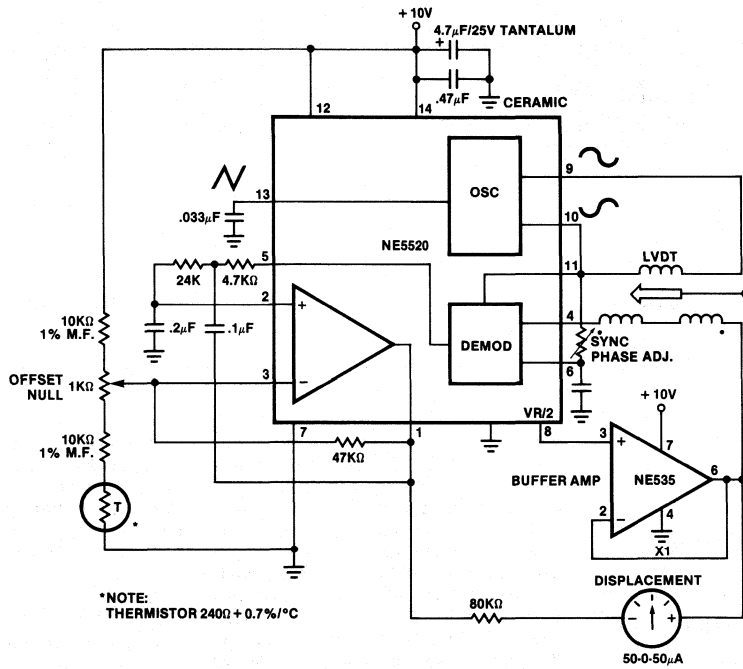


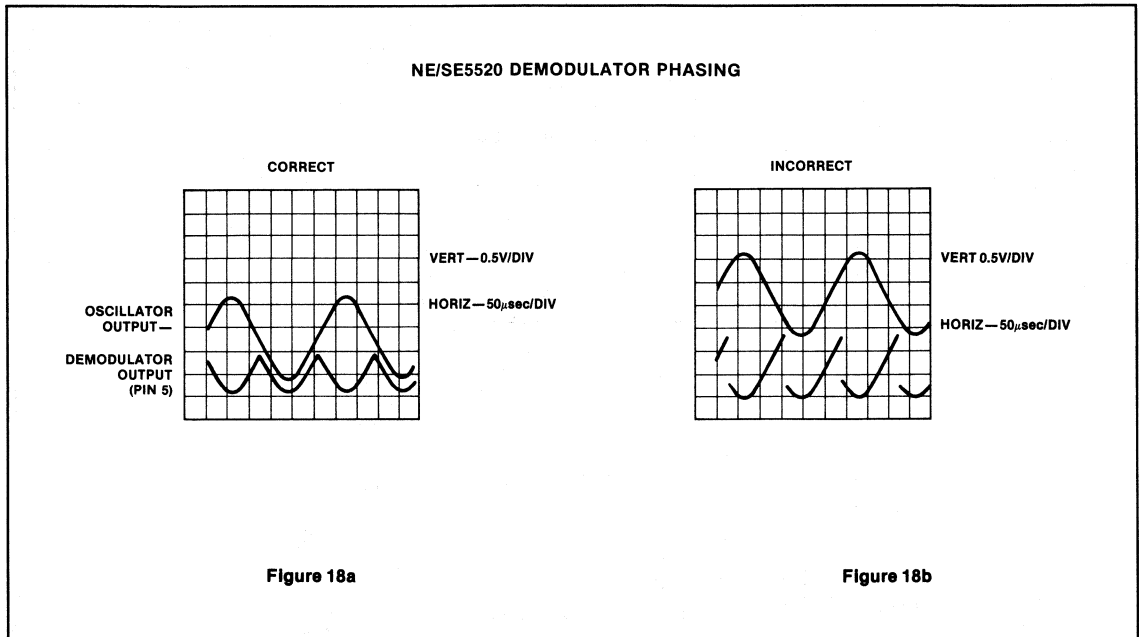
Figure 19a

7

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary



NE5520 LVDT DRIVER DEMODULATOR APPLICATIONS

OPERATED WITH A SINGLE POWER SUPPLY

The NE5520 may be operated with a single ended power supply ranging from +5 to 25 volts.

A very simple motion transducer may be constructed using the circuit shown in Figure 19A, B. The output is biased to one-half the supply voltage. This requires special interface circuitry for the signal readout. One simple method is to use a zero center meter in a bridge configuration as shown. Displacement now may be measured as a positive or negative meter reading. Readout sensitivity is a function of the particular LVDT and of the gain of the error amplifier. DC offsets may be nulled by using a simple offset adjustment circuit as indicated.

The transducer is centered in its displacement and the *offset adjust* pot set for a zero meter reading. Once this procedure is completed, the circuit is capable of making measurements based on transducer displacement. Displacement sensitivity is

a function of the LVDT transducer rated in volts-per-inch in addition to the transfer gain of the NE5520 demodulator. The input excitation is generally a fixed level as is the LVDT transducer transformer ratio. However, the auxiliary gain stage may be used to adjust the overall system sensitivity. This section of the device is also used to obtain a low-pass active filter for the smoothing of demodulator ripple. The design examples use a simple VCVS low-pass filter which allows gain and cut-off frequency to be adjusted independently. Gain equals ten in the example.

Note that using a single supply results in a DC common mode voltage at the output of one-half the reference voltage on pin 12. *This voltage V_B may be equal to but not greater than the supply voltage on pin 14.*

LVDT MEASURING CIRCUIT USING A DUAL SUPPLY

A second mode of operation makes use of dual power supply. A common choice may be ± 5 , ± 6 , or ± 10 volts. Special consideration must be made in properly biasing the internal circuitry to operate under these conditions. Figure 20 shows a simple design for working with ± 6 -volt supplies. Special provisions for minimizing

DC power supply offsets may be made by using the NE5512 dual op amp as a tracking voltage source and difference amplifier-output buffer (see Figure 9). A second method is to use a dual tracking regulator to supply the NE5520.

LVDT IN CLOSED LOOP SERVO

The LVDT provides an excellent method of obtaining position information for closed loop servo drive systems. Pressure rollers, hydraulic drivers, and motor driven linear motion transducers are a few of the general applications which may benefit from the accuracy and speed of response inherent in the LVDT sensor.

A simple block diagram (Figure 21A) shows one possible application in which the NE5520 with LVDT sensor provides accurate position control in a closed loop servo. Linear motion from millimeters to inches of translational motion are possible using the LVDT technique.

In practice the position voltage may be the output of a D/A converter which in turn is activated digitally from a controlling microprocessor. Keyboard information or software commands are translated directly into mechanical motion (Figure 21B).

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

LVDT SECONDARY PHASE ANGLE COMPENSATION BY EXCITATION FREQUENCY

The LVDT has a frequency dependent phase shift associated with the particular characteristics of the device and its excitation frequency. This phase shift is in addition to the 180° shift which occurs when passing through null position.

By adjusting the frequency of the sine wave excitation a condition results which causes secondary voltage to be in phase with primary excitation. The adjustment of relative primary and secondary phase angles has several effects. First, if the primary excitation is referenced to the synchronous demodulator, as in the NE5520, optimum rectification occurs at zero phase differential between secondary AC phase and demodulator switching relative to the waveform zero crossings. Second, "Exciting an LVDT at its zero phase angle frequency results in minimum sensitivity to frequency and temperature variations" (Schaevitz Handbook of Measurement and Control, 1976).

DEMODULATOR SYNC PHASE

A second method of phase compensation of the NE5520 versus the LVDT is to use a variable phase shift network between the oscillator output and the sync input to the NE5520. This is shown in Figure 17. The oscillator frequency remains fixed and the pot is tuned for optimum demodulator phasing.

It is emphasized that an external phasing adjustment as outlined above is not always necessary. Some LVDT's operating in the 1-5kHz range will be near zero phase and will need no phase compensation. Experimental evaluation of the prototype design combined with system specifications will be the best means of making this decision.

Waveform photo in Figure 18A-B, shows the demodulator output signal when phasing of the synchronous demodulator is correct (A) and improperly adjusted (B).

Proper phasing of the sync signal to the demodulator results in optimum sensitivity and linearity.

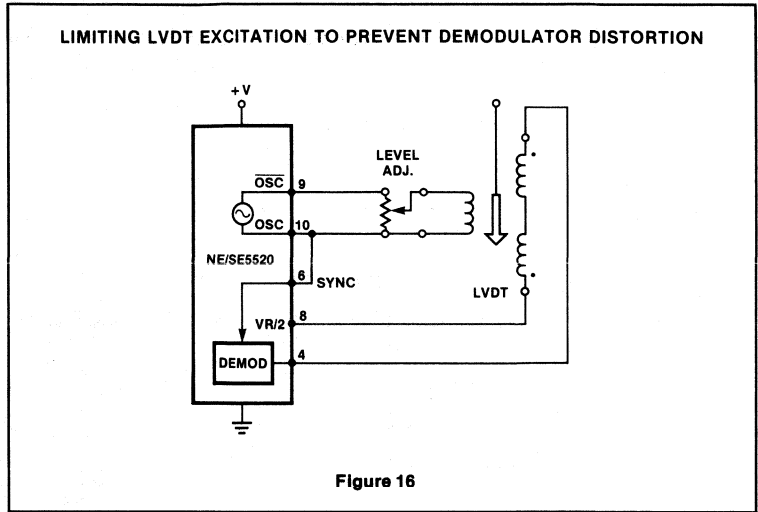


Figure 16

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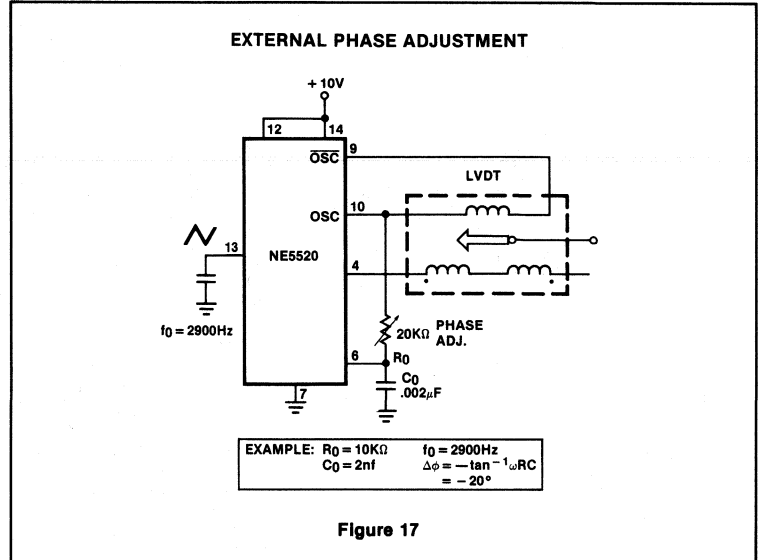


Figure 17

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

NE5520 LVDT MEASURING CIRCUIT WITH LIMIT DETECTOR

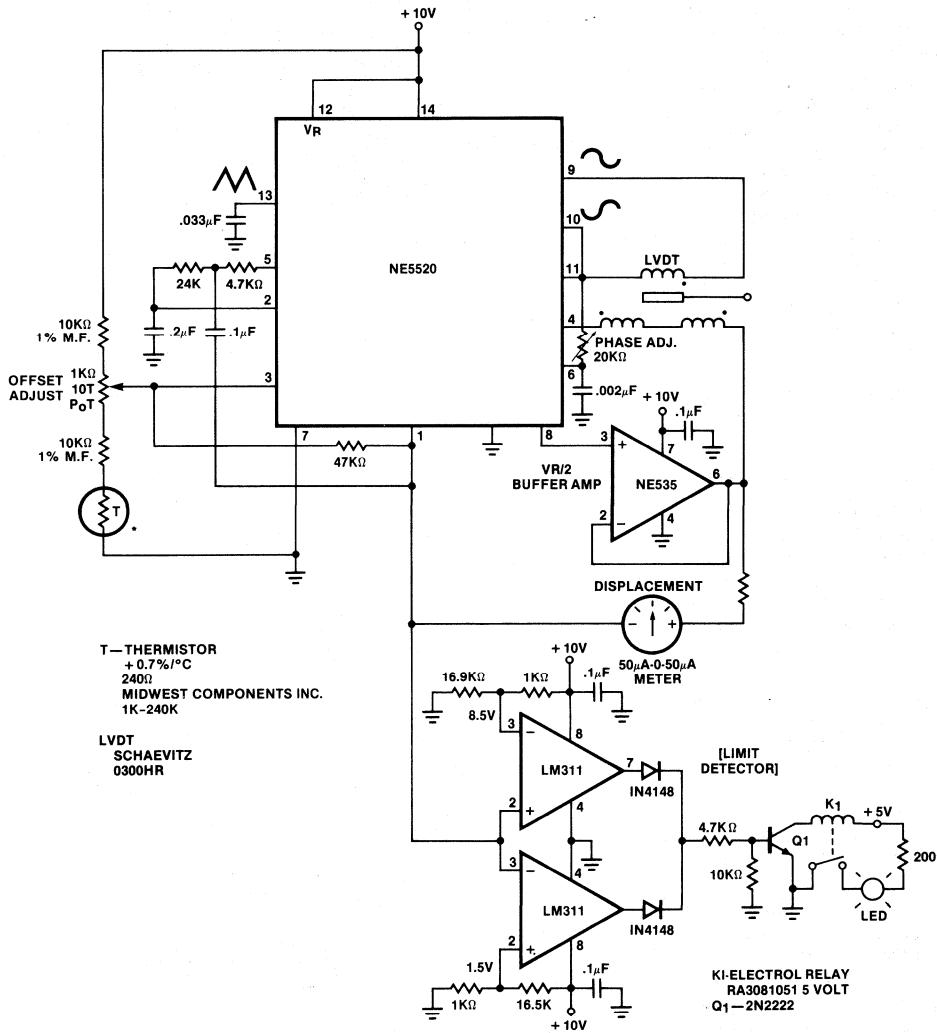


Figure 19b

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

NE5520 LVDT DRIVER-DEMODULATOR $\langle f_o = 2900\text{Hz} \rangle$

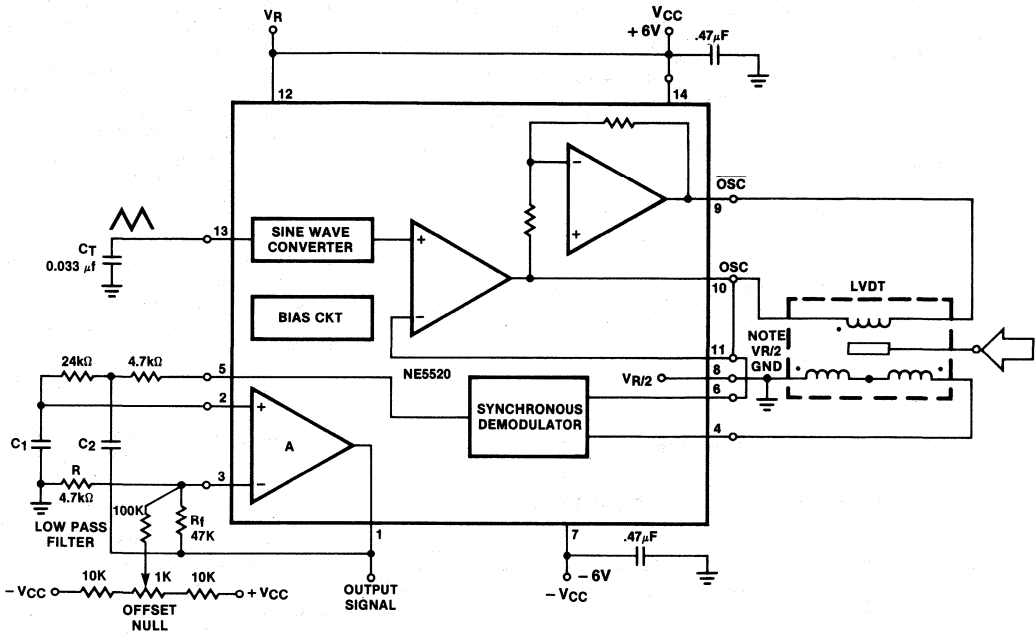


Figure 20

7

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

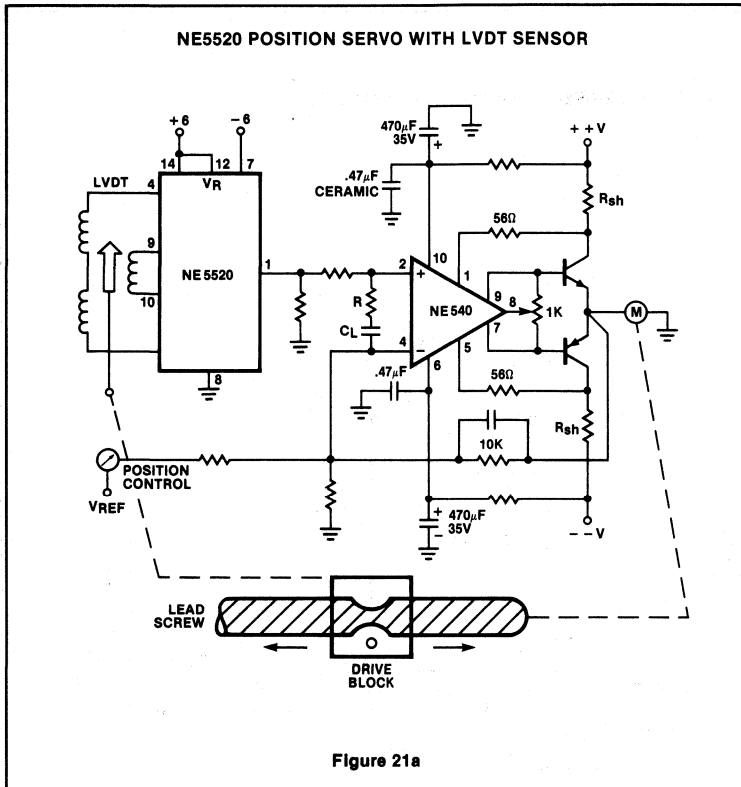


Figure 21a

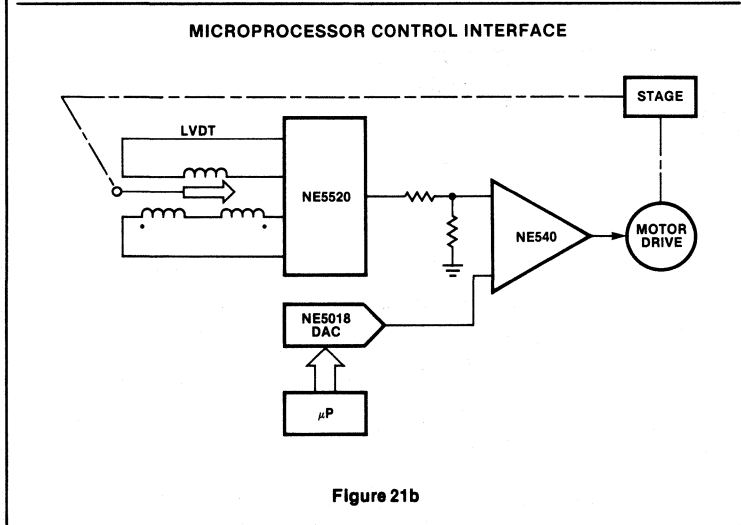


Figure 21b

LVDT SIGNAL TRANSMISSION BY CURRENT LOOP

In certain situations the demodulated output signal must be transmitted over long wires or cables before reaching the signal monitoring equipment. The receiver end may consist of chart recorders, digital panel meters and computers or microprocessors. In some systems many LVDT signals must be monitored from different locations thus requiring variable wire length between transmitter and receiver, thus a different line resistance in each case. If voltage feed were used, signal accuracy would be affected by line resistance. This need for accurate signal transmission necessitates the use of a current loop. A current loop develops a current exactly in proportion to the demodulated LVDT output voltage. It is not affected by line resistance within certain limits governed by the current generator.

The conversion to current loop output may facilitate a bipolar output from a dual supply system as in Figure 22. A third method uses the $V_{R/2}$ common mode reference to create a null balance signal circuit which is converted to a bipolar current signal corresponding to the LVDT transducer null (i.e. physical displacement center null position at which zero current occurs). This method is shown in Figure 23 and requires the use of an external dual op amp, half of which is used to provide a buffered reference ($V_{R/2}$) voltage return for the current loop. With $R_2 = 200$ ohms the current loop sensitivity is 5 milliamperes per volt of input signal. In all cases, the current output to the loop receiver will remain constant with fixed input voltage (LVDT demodulator) even for varying line resistance up to 600 ohms. This resistance must include all wire and load drops in the loop. Various full scale current limits require different supply voltages and without external supplies will be limited by op amp swing characteristics. That is in order to force a given current across $R_L + R_2$ results in an ultimate voltage limit from the op amp output in the current converter as total resistance increases.

A fourth method uses an external supply and discrete transistor controlled by the closed loop op amp referenced to shunt resistor R_{SH} in the emitter return circuit. This of course is a unipolar current loop. See Figure 24.

LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

NE5520 LVDT SYSTEM WITH BIPOLAR CURRENT LOOP USING NE540 POWER DRIVER

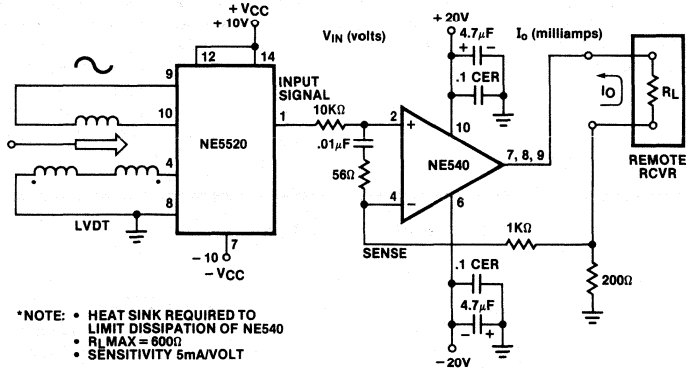


Figure 22

NE5520 WITH BIPOLAR CURRENT LOOP OUTPUT ± 10mA F.S. — SINGLE SUPPLY OPERATION

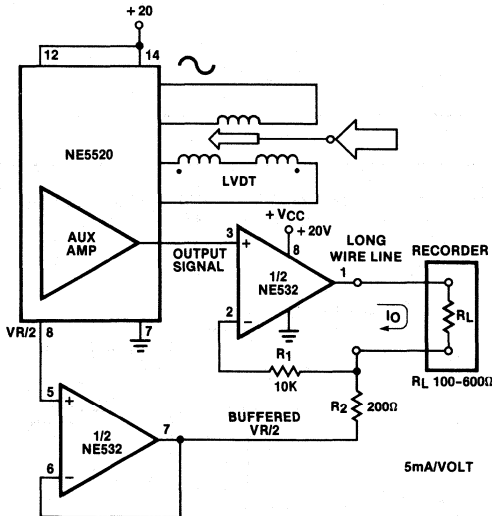


Figure 23

7

LVDT SIGNAL CONDITIONER

NE/SE5520

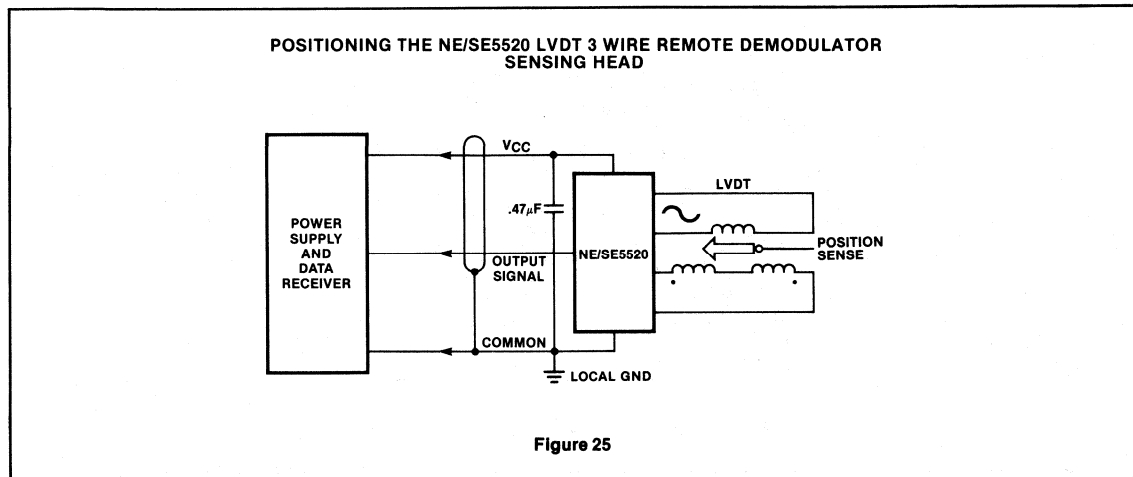
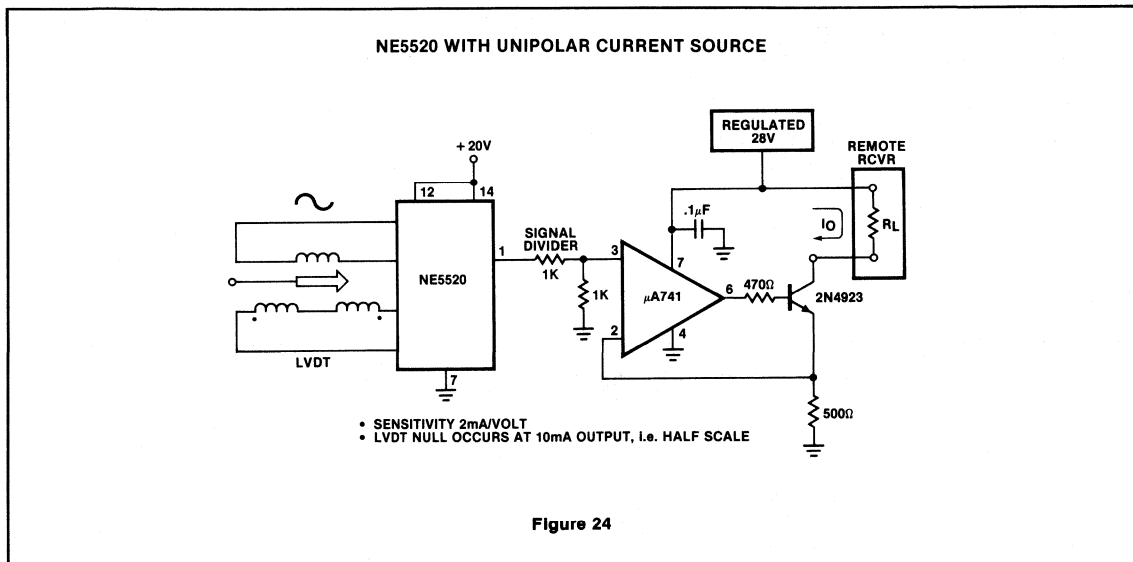
Preliminary

Some systems in common use require two wire source to include both the device operating current and the signal loop current. Thus the quiescent device current must be nulled out at the receiver end leaving the residual signal loop current. The NE5520 is not well suited to this particular design since the device standby current is approximately 10 milliamperes.

A current loop operated from supply voltage sources at the transducer location is a better choice for the operation of an output signal loop where long lines must carry locally generated LVDT signals after demodulation back to the monitor site. Supply voltages in the range from 20 to 48 volts will fill nearly every loop requirement.

POSITIONING THE NE/SE5520 LVDT 3-WIRE REMOTE DRIVER DEMODULATOR SENSING HEAD

The NE5520 may be placed in close proximity to the LVDT transducer provided the environment stays within device specifications. This physical arrangement allows only DC supply and low frequency signal lines (3 wires) being run between the transducer-conditioner unit and the signal processing station as shown in Figure 25.



LVDT SIGNAL CONDITIONER

NE/SE5520

Preliminary

MULTIPLE TRANSDUCER OPERATION — SYNCHRONOUS OSCILLATOR MODE

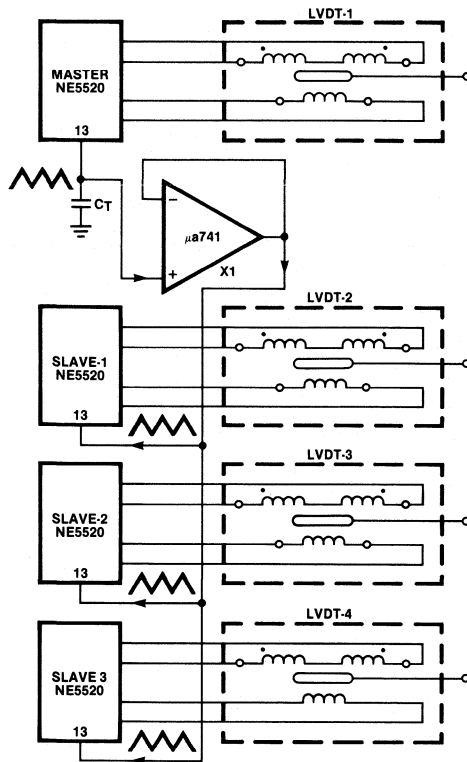


Figure 26

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Handbook of Integrated-Circuit Operational Amplifiers, by George B. Rutkowski, Prentice Hall 1975, Englewood Cliffs, New Jersey.

Signetics Analog Applications Manual, 1979 Edition, Signetics Corporation, Sunnyvale, California.

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7

Section 8 Comparators

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Section 8 — Comparators

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VOLTAGE COMPARATOR

LM111/211/311

DESCRIPTION

The LM111 series are voltage comparators that have input currents approximately a hundred times lower than devices like the μ A710. They are designed to operate over a wider range of supply voltages; from standard $\pm 15V$ op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL, and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50mA.

Both the inputs and the outputs of the LM111 series can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the μ A710 (200ns response time vs 40ns) the devices are also much less prone to spurious oscillations. The LM111 series has the same pin configuration as the μ A710 series.

FEATURES

- Operates from single 5V supply
- Maximum input bias current: 150nA (LM311 - 250nA)
- Maximum offset current: 20nA (LM311 - 50nA)
- Differential input voltage range: $\pm 30V$
- Power consumption: 135mW at $\pm 15V$
- High sensitivity—200V/mV

PIN CONFIGURATIONS

N PACKAGE

TOP VIEW
ORDER NUMBERS
LM211N/LM311N
LM311D

F,N-14 PACKAGE

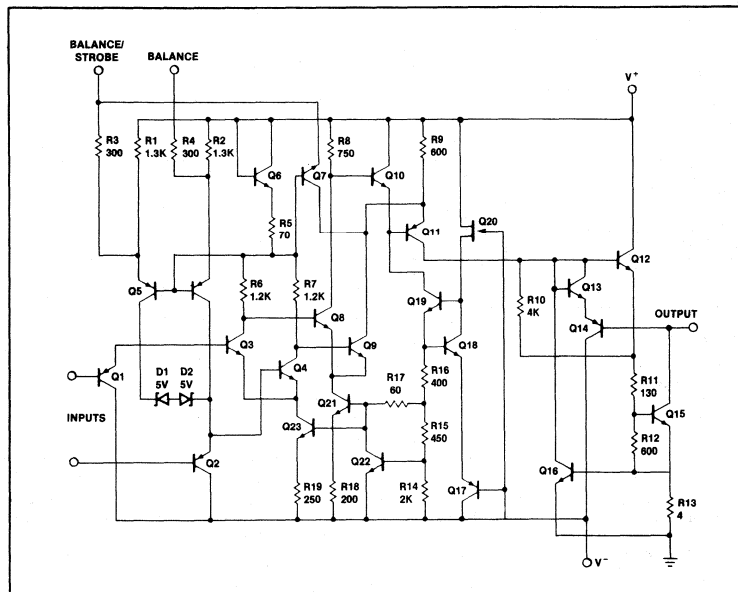
TOP VIEW
ORDER NUMBERS
LM111F/LM211F/LM211N-14
LM311F/LM311N-14

H PACKAGE*

ORDER NUMBERS
LM111H/LM211H/LM311H

*Metal cans (H) not recommended for new designs

EQUIVALENT SCHEMATIC



VOLTAGE COMPARATOR

LM111/211/311

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage:		
LM111/LM211	50	V
LM311	40	V
Ground to negative supply voltage	30	V
Differential input voltage	±30	V
Input voltage ¹	±15	V
Power dissipation ²	500	mW
Output short circuit duration	10	sec
Operating temperature range		
LM111	-55 to +125	°C
LM211	-25 to +85	°C
LM311	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

DC ELECTRICAL CHARACTERISTICS 1,2,3

PARAMETER	TEST CONDITIONS	LM111/LM211			LM311			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ⁴	$T_A = 25^\circ\text{C}$, $R_S \leq 50\text{k}\Omega$		0.7	3.0		2.0	7.5	mV
Input offset current ⁴	$T_A = 25^\circ\text{C}$		4.0	10		6.0	50	nA
Input bias current	$T_A = 25^\circ\text{C}$		60	100		100	250	nA
Voltage gain	$T_A = 25^\circ\text{C}$		200			200		V/mV
Response time ⁵	$T_A = 25^\circ\text{C}$		200			200		ns
Saturation voltage	$V_{IN} \leq -5\text{mV}$, $I_{OUT} = 50\text{mA}$ $T_A = 25^\circ\text{C}$		0.75	1.5		0.75	1.5	V
Strobe on current	$T_A = 25^\circ\text{C}$		3.0			3.0		mA
Output leakage current	$V_{IN} \geq 5\text{mV}$, $V_{OUT} = 35\text{V}$ $T_A = 25^\circ\text{C}$, $I_{STROBE} = 3\text{mA}$		0.2	10		0.2	50	nA
Input offset voltage ⁴	$R_S \leq 50\text{k}\Omega$			4.0			10	mV
Input offset current ⁴				20			70	nA
Input bias current				150			300	nA
Input voltage range	$V_+ \geq 4.5\text{V}$, $V_- = 0$		±14			±14		V
Saturation voltage	$V_{IN} \leq -6\text{mV}$, $I_{SINK} \leq 8\text{mA}$		0.23	0.4		0.23	0.4	V
Output leakage current	$V_{IN} \geq 5\text{mV}$, $V_{OUT} = 35\text{V}$		0.1	0.5				μA
Positive supply current	$T_A = 25^\circ\text{C}$		5.1	6.0		5.1	7.5	mA
Negative supply current	$T_A = 25^\circ\text{C}$		4.1	5.0		4.1	5.0	mA

NOTES

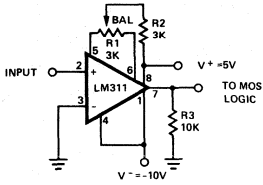
- This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
- The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, in the N package, a thermal resistance of 162°C/W, and °C/W for the Ceramic package. The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient. The thermal resistance of the Cerdpip package is 110°C/W, junction to ambient.
- These specifications apply for $V_S = \pm 15\text{V}$ and $0^\circ\text{C} < T_A < 70^\circ\text{C}$ unless otherwise specified. With the LM211, however, all temperature specifications are limited to $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ and for the LM111 is limited to $-55^\circ\text{C} < T_A < 125^\circ\text{C}$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.
- The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
- The response time specified (see definitions) is for a 100mV input step with 5mV overdrive.

VOLTAGE COMPARATOR

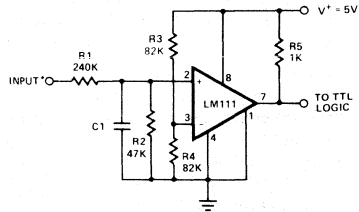
LM111/211/311

TYPICAL APPLICATIONS

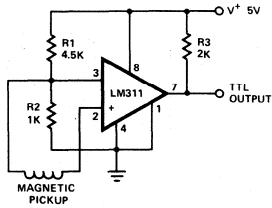
**ZERO CROSSING DETECTOR
DRIVING MOS LOGIC**



**TTL INTERFACE WITH HIGH
LEVEL LOGIC**



**DETECTOR FOR MAGNETIC
TRANSDUCER**



*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.



DUAL VOLTAGE COMPARATOR

LM119/219/319

DESCRIPTION

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the μ A710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25mA.

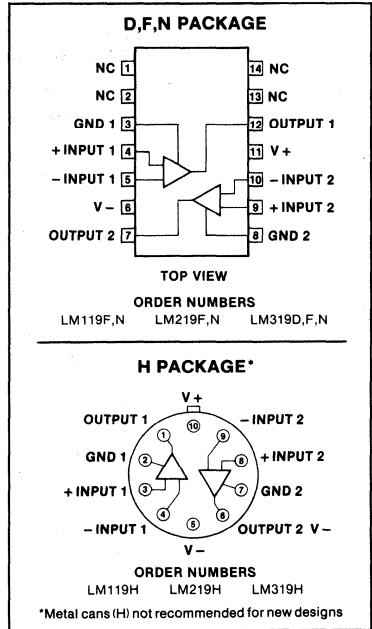
Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to $\pm 15V$. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the μ A711.

The LM119 is specified from $-55^{\circ}C$ to $+125^{\circ}C$, the LM219 is specified from $-25^{\circ}C$ to $+85^{\circ}C$, and the LM319 is specified from $0^{\circ}C$ to $+70^{\circ}C$.

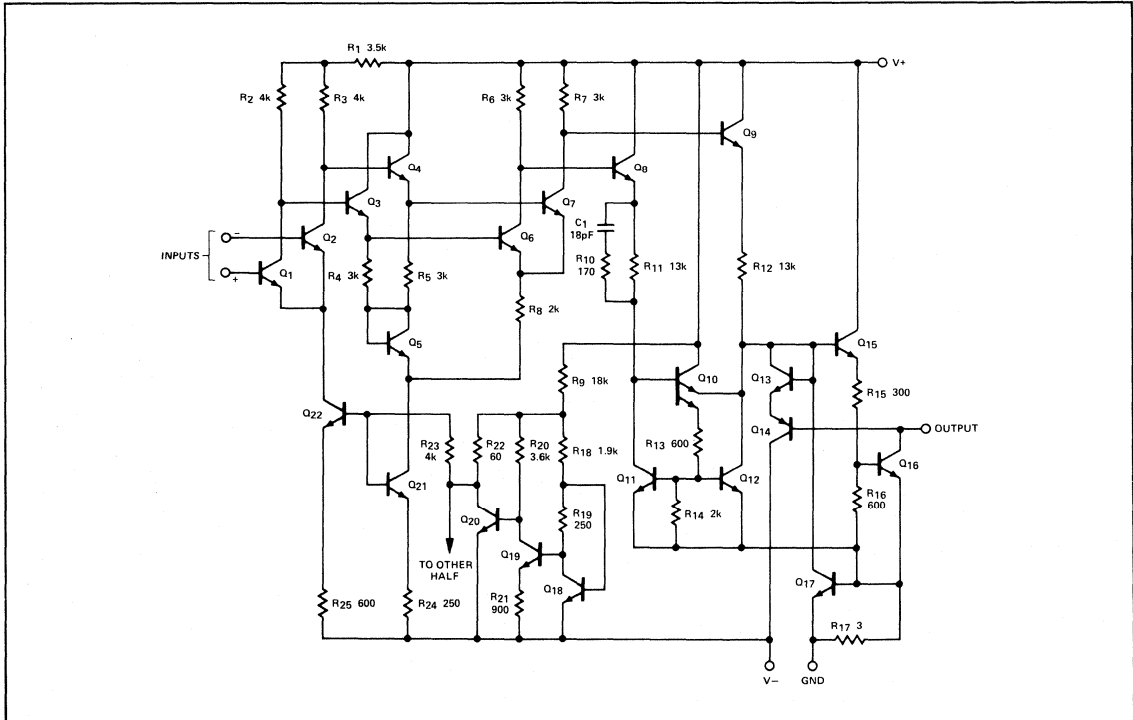
FEATURES

- Two independent comparators
- Operates from a single 5V supply
- Typically 80ns response time at $\pm 15V$
- Minimum fan-out of 3 (each side)
- Maximum input current of $1\mu A$ over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate
- MIL-STD-883 A, B, C available

PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC



DUAL VOLTAGE COMPARATOR

LM119/219/319

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Total supply voltage	36	V
Output to negative supply voltage	36	V
Ground to negative supply voltage	25	V
Ground to positive supply voltage	18	V
Differential input voltage	±5	V
Input voltage ¹	±15	V
Power dissipation ²	500	mW
Output short circuit duration	10	s
Operating temperature range		
LM119	-55 to +125	°C
LM219	-25 to +85	°C
LM319	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

NOTES

- For supply voltages less than ±15V, the absolute maximum rating is equal to the supply voltage.
- The absolute maximum junction temperature is 150°C. Device dissipation must be derated as follows:
 N/K package—150°C/watt above 75°C
 F package —110°C/watt above 95°C

DC ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, for $\left. \begin{matrix} \text{LM119, } -55^\circ\text{C} \leq T_A \leq 125^\circ\text{C} \\ \text{LM219, } -25^\circ\text{C} \leq T_A \leq 85^\circ\text{C} \\ \text{LM319, } 0^\circ\text{C} \leq T_A \leq 70^\circ\text{C} \end{matrix} \right\}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LM119/219			LM319			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage ^{1,2}	$R_S \leq 5K\Omega$, $T_A = 25^\circ\text{C}$ Over temp.		0.7	4.0 7		2.0	8.0 10	mV mV
I_{OS} Input offset current ^{1,2}	$T_A = 25^\circ\text{C}$ Over temp.		30	75 100		80	200 300	nA nA
I_B Input bias current ¹	$T_A = 25^\circ\text{C}$ Over temp.		150	500 1000		250	1000 1200	nA nA
A_V Voltage gain	$T_A = 25^\circ\text{C}$	10	40		8	40		V/mV
V_{OL} Saturation voltage	$V_{IN} = 5mV$, $I_{OUT} = 25mA$, $T_A = 25^\circ\text{C}$		0.75	1.5		0.75	1.5	V V
	$V_{IN} = 10mV$, $I_{OUT} = 25mA$, $T_A = 25^\circ\text{C}$ $V^+ \geq 4.5V$, $V^- = 0$							
	$V_{IN} = 6mV$, $I_{OUT} = 3.2mA$ $T_A \geq 0^\circ\text{C}$ $T_A \leq 0^\circ\text{C}$		0.23	0.4 0.6				V V
	$V_{IN} = 10mV$, $I_{OUT} = 3.2mA$					0.3	0.4	V V
I_{OH} Output leakage current	$V^- = 0V$, $V_{IN} = 5mV$ $V_{OUT} = 35V$, $T_A = 25^\circ\text{C}$ Over temp.		0.2 1	2 10				μA μA
	$V^- = 0V$, $V_{IN} = 10mV$ $V_{OUT} = 35V$, $T_A = 25^\circ\text{C}$					0.2	10	μA μA
V_{IN} Input voltage range	$V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0V$	1	±13		1	±13	3	V V
V_{ID} Differential input voltage				±5			±5	V
I^+ Positive supply current	$V^+ = 5V$, $V^- = 0V$, $T_A = 25^\circ\text{C}$		4.3			4.3		mA
I^+ Positive supply current	$V_S = \pm 15V$, $T_A = 25^\circ\text{C}$		8.0	11.5		8.0	12.5	mA
I^- Negative supply current	$V_S = \pm 15V$, $T_A = 25^\circ\text{C}$		3.0	4.5		3.0	5.0	mA

NOTES

- V_{OS} , I_{OS} and I_B specifications apply for a supply voltage range of $V_S = \pm 15V$ down to a single 5V supply.
- The offset voltages and offset currents given are the maximum values required to drive the output to within 1 volt of either supply with a 1mA load. Thus these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.



DUAL VOLTAGE COMPARATOR

LM119/219/319

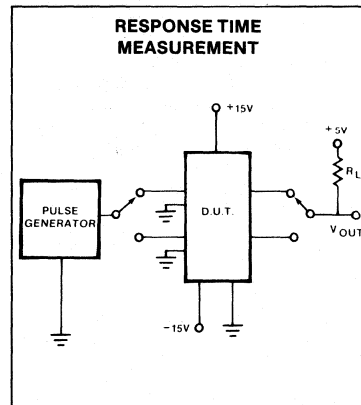
AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Response time*	$V_S = \pm 15V, T_A = 25^\circ C$ $R_L = 500\Omega$ (see test figure)		80		ns

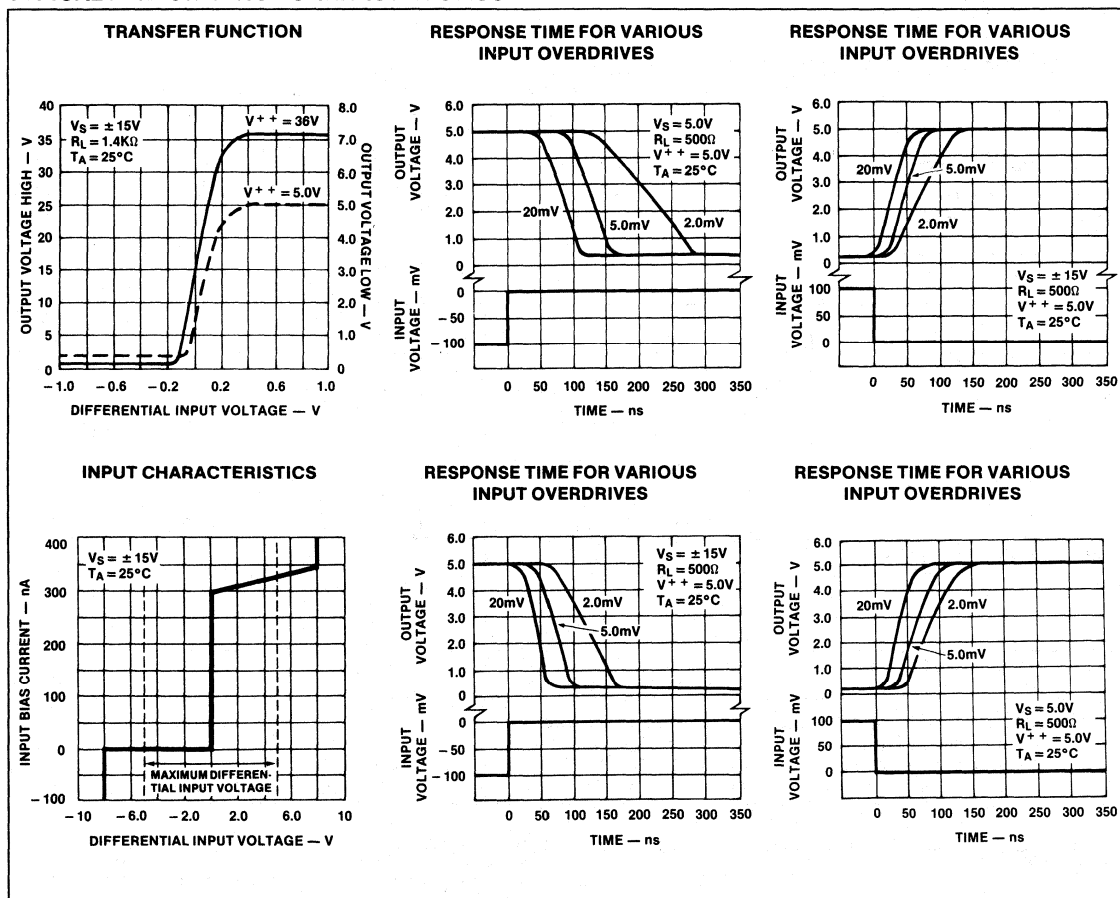
*NOTE

The response time specified is for a 100mV step with 5mV overdrive.

TEST CIRCUIT



TYPICAL PERFORMANCE CHARACTERISTICS

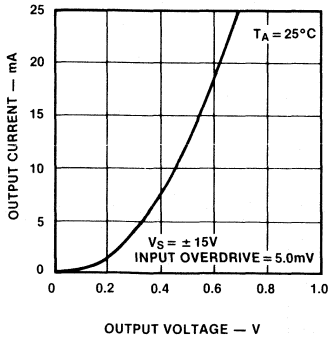


DUAL VOLTAGE COMPARATOR

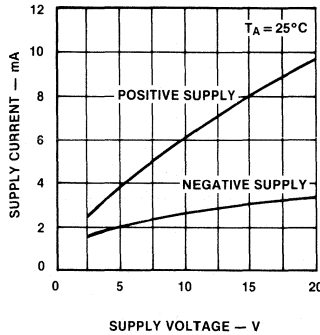
LM119/219/319

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

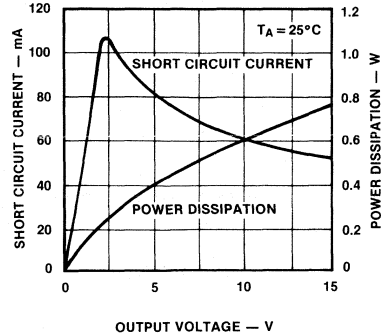
OUTPUT SATURATION VOLTAGE



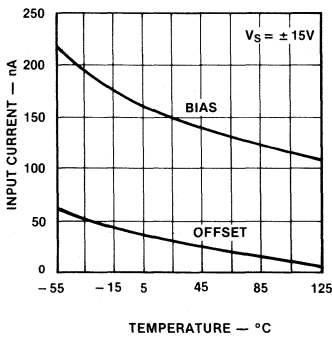
SUPPLY CURRENT



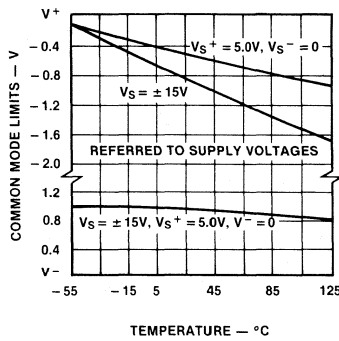
OUTPUT LIMITING CHARACTERISTICS



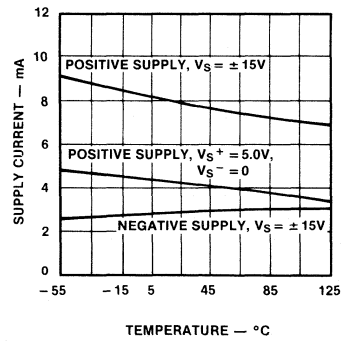
INPUT CURRENTS (LM119/219)



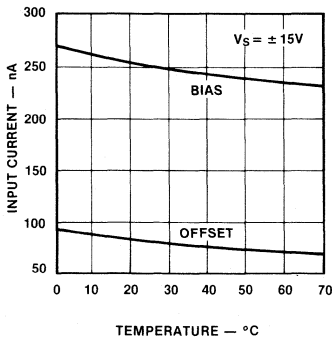
COMMON MODE LIMITS (LM119/219)



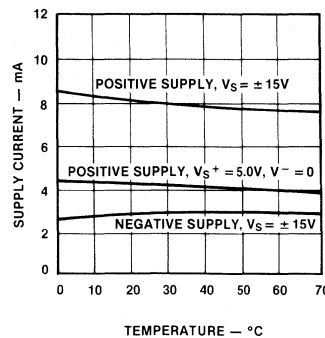
SUPPLY CURRENT (LM119/219)



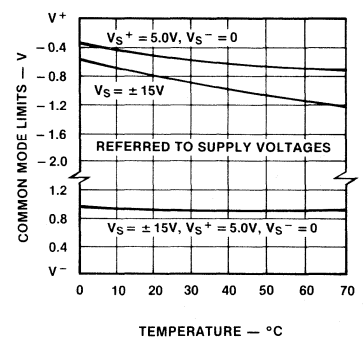
INPUT CURRENTS (LM319)



SUPPLY CURRENTS (LM319)



COMMON MODE LIMITS (LM319)

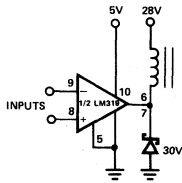


DUAL VOLTAGE COMPARATOR

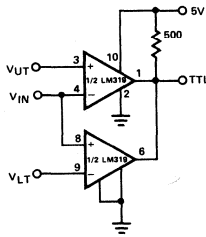
LM119/219/319

TYPICAL APPLICATIONS

RELAY DRIVER

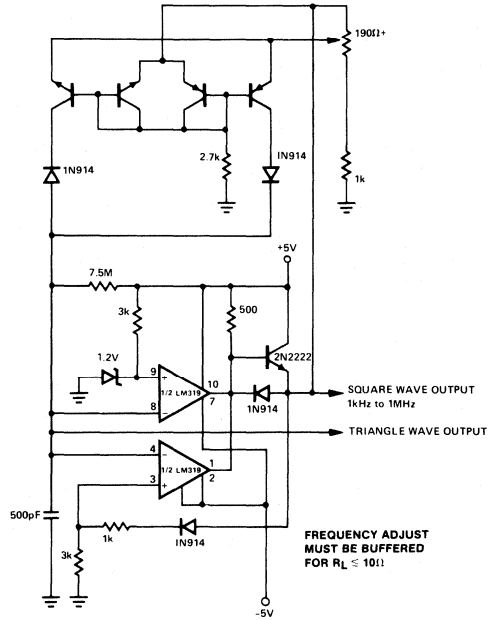


WINDOW DETECTOR



$V_{OUT} = 5V$ for $V_{LT} < V_{IN} < V_{UT}$
 $V_{OUT} = 0$ for $V_{IN} < V_{LT}$ or $V_{IN} > V_{UT}$

WIDE RANGE VARIABLE OSCILLATOR



QUAD VOLTAGE COMPARATOR

LM139/239/339 MC3302/LM2901

DESCRIPTION

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for each comparator which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM139 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

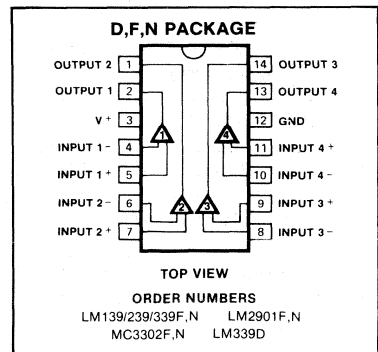
FEATURES

- Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies $\pm 1.0Vdc$ to $\pm 18Vdc$
- Very low supply current drain (0.8mA) independent of supply voltage (1.0mW/comparator at 5.0Vdc)
- Low input biasing current 25nA
- Low input offset current $\pm 5nA$ and offset voltage $\pm 2mV$
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage.
- Low output 250mV at 4mA saturation voltage
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.

APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

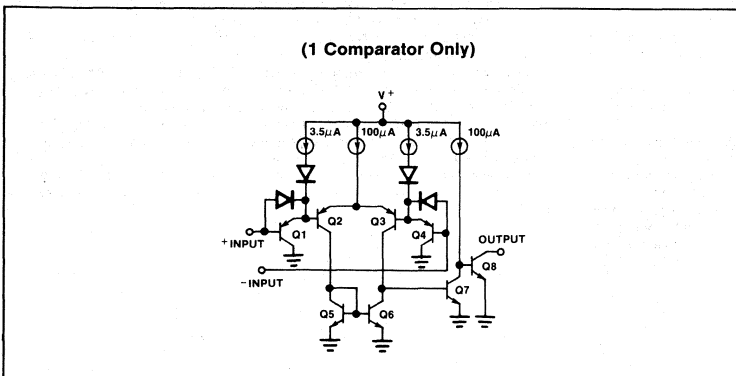
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Vcc supply voltage	36 or ± 18	
Differential input voltage	36	
Input voltage	-0.3 to +36	
Power dissipation ¹		
Molded DIP	570	mW
CERDIP	900	mW
Output short circuit to ground ²	Continuous	
Input current ($V_{IN} < -0.3Vdc$) ³	50	mA
Operating temperature range		
LM139	-55 to +125	°C
LM239	-25 to +85	°C
LM339	0 to +70	°C
LM2901/MC3302	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

EQUIVALENT CIRCUIT



QUAD VOLTAGE COMPARATOR

LM139/239/339 MC3302/LM2901

DC ELECTRICAL CHARACTERISTICS $V_+ = 5V_{dc}$, LM139: $-55^\circ C \leq T_A \leq 125^\circ C$ unless otherwise specified
 LM239: $-25^\circ C \leq T_A \leq 85^\circ C$ unless otherwise specified
 LM339: $0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	LM139			LM239/339			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage ⁵	$T_A = 25^\circ C$ Over temp.		± 2.0	± 5.0 9.0		± 2.0	± 5.0 9.0	mV
V_{CM} Input common mode voltage range ⁶	$T_A = 25^\circ C$ Over temp.	0 0		$V_+ - 1.5$ $V_+ - 2.0$	0 0		$V_+ - 1.5$ $V_+ - 2.0$	V
V_{IDR} Differential input voltage ⁴	Keep all $V_{INs} \geq 0V_{dc}$ (or V-if used)			V_+			V_+	V
I_B Input bias current ⁷	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25^\circ C$ Over temp.		25	100 300		25	250 400	nA
I_{OS} Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25^\circ C$ Over temp.		± 3.0	± 25 ± 100		± 5.0	± 50 ± 150	nA nA
I_{OL} Output sink current	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $V_0 \leq 1.5V_{dc}$, $T_A = 25^\circ C$	6.0	16		6.0	16		mA
I_{OH} Output leakage current	$V_{IN(+)} \geq 1V_{dc}$, $V_{IN(-)} = 0$ $V_0 = 5V_{dc}$, $T_A = 25^\circ C$ $V_0 = 30V_{dc}$, over temp.		0.1	1.0		0.1	1.0	nA μA
I_{CC} Supply current	$R_L = \infty$ on all comparators, $T_A = 25^\circ C$		0.8	2.0		0.8	2.0	mA
A_V Voltage gain	$R_L \geq 15k\Omega$, $V_+ = 15V_{dc}$ $T_A = 25^\circ C$	50	200		50	200		V/mV
V_{OL} Saturation voltage	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25^\circ C$ Over temp.		250	400 700		250	400 700	mV
T_{LSR} Large signal response time	$V_{IN} = TTL$ logic swing, $V_{REF} = 1.4V_{dc}$, $V_{RL} = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		300			300		ns
T_R Response time ⁸	$V_{RL} = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		1.3			1.3		μs

NOTES

- For operating at high temperatures, the LM339/339A, LM2901 and MC3302 must be derated based on a $125^\circ C$ maximum junction temperature and a thermal resistance of $175^\circ C/W$ which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM139/139A/239/239A must be derated on a $150^\circ C$ maximum junction temperature. The low power dissipation and the "On-Off" characteristics of the outputs keep the chip dissipation very small ($P_D \leq 100mW$), provided the output transistors are allowed to saturate.
- Short circuits from the output to V_+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V_+ .
- This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V_+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{dc}$.
- Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{dc}$ (or $0.3V_{dc}$ below the magnitude of the negative power supply, if used).
- At output switch point, $V_0 = 1.4V_{dc}$, $R_S = 0\Omega$ with V_+ from $5V_{dc}$ to $30V_{dc}$; and over the full input common-mode range ($0V_{dc}$ to $V_+ - 1.5V_{dc}$).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than $0.3V$. The upper end of the common-mode voltage range is $V_+ - 1.5V$, but either or both inputs can go to $30V_{dc}$ without damage.
- The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- The response time specified is for a $100mV$ input step with a $5mV$ overdrive. For larger overdrive signals, 300ns can be obtained, see typical performance characteristics section.

QUAD VOLTAGE COMPARATOR

LM139/239/339 MC3302/LM2901

DC ELECTRICAL CHARACTERISTICS

V+ = 15Vdc, MC3302

LM2901/MC3302: -40°C ≤ T_A ≤ 85°C unless otherwise specified

PARAMETER	TEST CONDITIONS	LM2901			MC3302			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{OS} Input offset voltage ⁵	T _A = 25°C Over temp.		±2.0 ±9	±7.0 ±15		±3.0	±20 ±40	mV
V _{CM} Input common mode voltage range ⁶	T _A = 25°C Over temp.	0 0		V+ - 1.5 V+ - 2.0			V+ - 1.5 V+ - 2.0	V
V _{IDR} Differential input voltage ⁴	Keep all V _{INs} ≥ 0Vdc (or V-if need)			V+			V+	V
I _B Input bias current ⁷	I _{IN(+)} or I _{IN(-)} with output in linear range T _A = 25°C Over temp.		25 200	250 500		25	500 1000	nA
I _{OS} Input offset current	I _{IN(+)} - I _{IN(-)} T _A = 25°C Over temp.		±5 ±50	±50 ±200		±5		nA nA
I _{OL} Output sink current	V _{IN(-)} ≥ 1Vdc, V _{IN(+)} = 0, V _O ≤ 1.5Vdc, T _A = 25°C V _O = 800mV, Over temp.	6.0	16		2.0			mA
I _{OH} Output leakage current	V _{IN(+)} ≥ 1Vdc, V _{IN(-)} = 0 V _O = 5Vdc, T _A = 25°C V _O = 30V Over temp. V _O = 28V T _A = 25°C		0.1	1.0		0.1	1.0	nA μA
I _{CC} Supply current	R _L = ∞ on comparators, V+ = 5Vdc, T _A = 25°C V+ = 30V, T _A = 25°C V+ = 5 to 28 Vdc, T _A = 25°C		0.8 1.0	2.0 2.5		0.8	2.0	mA
A _V Voltage gain	R _L ≥ 15kΩ, V+ = 15Vdc T _A = 25°C	25	100		2	100		V/mV
V _{OL} Saturation voltage	V _{IN(-)} ≥ 1Vdc, V _{IN(+)} = 0, I _{SINK} ≤ 4mA T _A = 25°C Over temp. I _{SINK} = 2mA, V+ = 5V to 28V, T _A = 25°C		400	400 700		150	400	mV
T _{LSR} Large signal response time	V _{IN} = TTL logic swing, V _{REF} = 1.4Vdc, V _{RL} = 5Vdc, R _L = 5.1kΩ, T _A = 25°C		300			300		ns
T _R Response time ⁸	V _{RL} = 5Vdc, R _L = 5.1kΩ, T _A = 25°C		1.3			1.3		μs

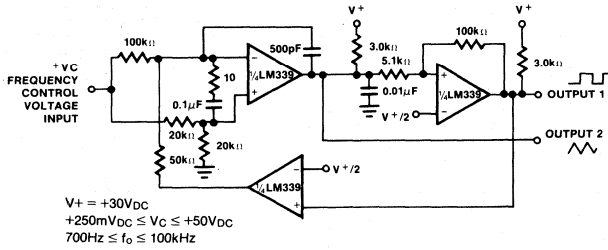
Notes 1-8, refer to preceding page.

QUAD VOLTAGE COMPARATOR

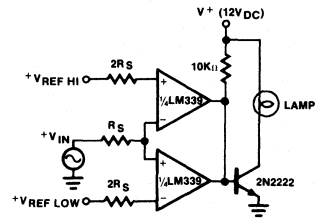
LM139/239/339 MC3302/LM2901

TYPICAL APPLICATIONS

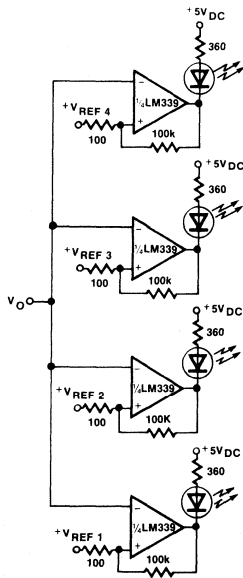
TWO-DECADE HIGH-FREQUENCY VCO



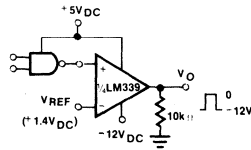
LIMIT COMPARATOR



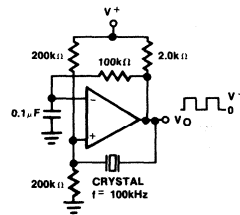
VISIBLE VOLTAGE INDICATOR



TTL TO MOS LOGIC CONVERTER



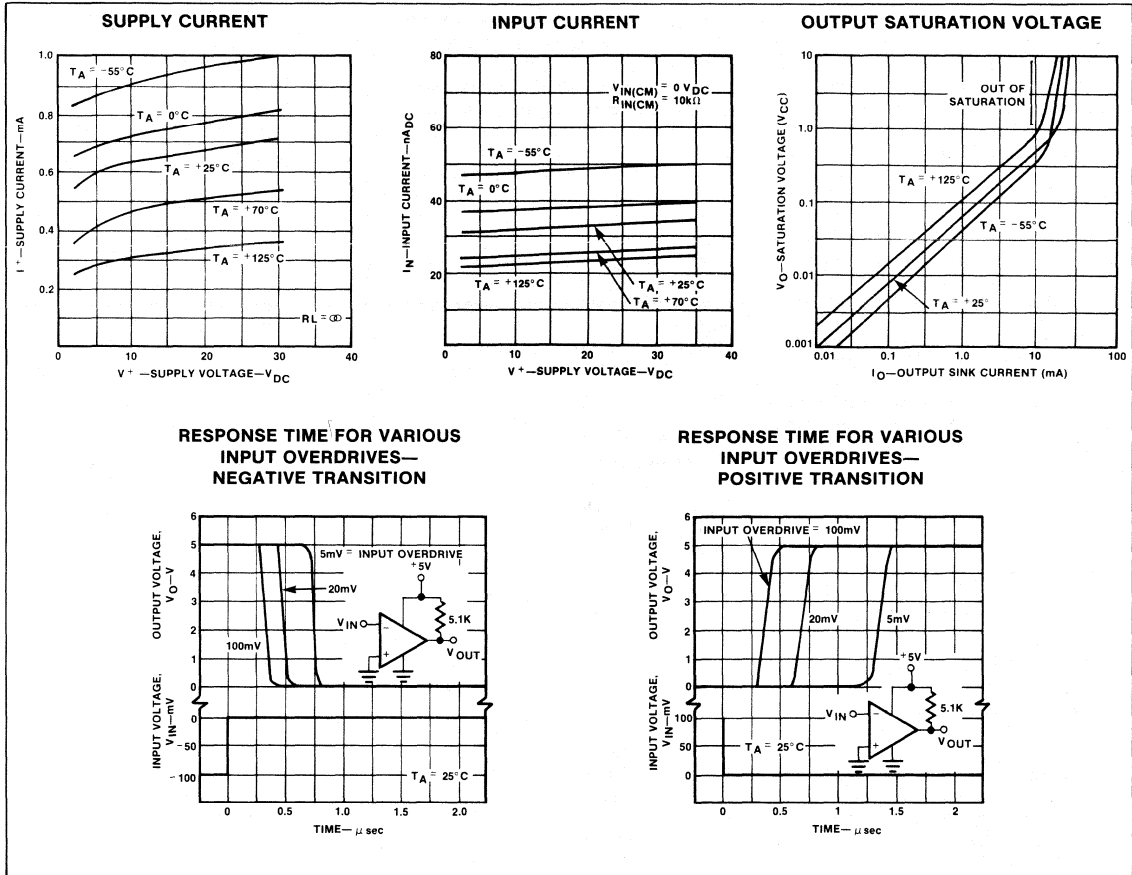
CRYSTAL CONTROLLED OSCILLATOR



QUAD VOLTAGE COMPARATOR

LM139/239/339 MC3302/LM2901

TYPICAL PERFORMANCE CHARACTERISTICS



LOW POWER DUAL VOLTAGE COMPARATOR LM193/A/293/A/393/A/2903

DESCRIPTION

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common mode voltage range includes ground, even though operated from a single power supply voltage.

The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

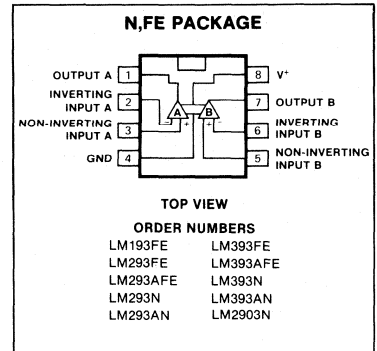
FEATURES

- **Wide single supply voltage range 2.0Vdc to 36Vdc or dual supplies $\pm 1.0\text{Vdc}$ to $\pm 18\text{Vdc}$**
- **Very low supply current drain (0.8mA) independent of supply voltage (2.0mW/comparator at 5.0Vdc)**
- **Low input biasing current 25nA**
- **Low input offset current $\pm 5\text{nA}$ and offset voltage $\pm 2\text{mV}$**
- **Input common-mode voltage range includes ground**
- **Differential input voltage range equal to the power supply voltage.**
- **Low output 250mV at 4mA saturation voltage**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems.**

APPLICATIONS

- A/D converters
- Wide range VCO
- MOS clock generator
- High voltage logic gate
- Multivibrators

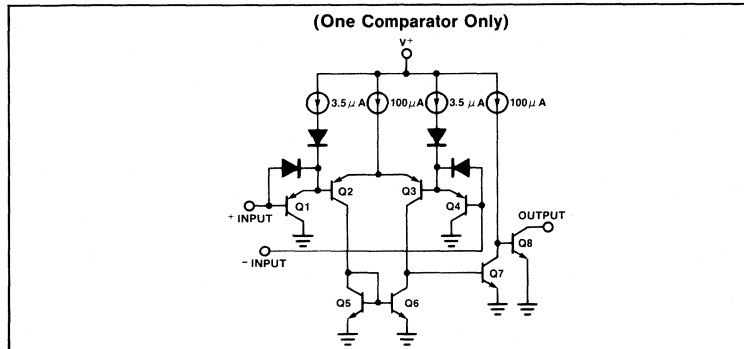
PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} supply voltage	36 or ± 18	Vdc
Differential input voltage	36	Vdc
Input voltage	-0.3 to +36	Vdc
Power dissipation ¹		
Molded DIP	570	mW
Metal can	900	mW
Output short circuit to ground ²	Continuous	
Input current (V _{IN} < -0.3Vdc) ³	50	mA
Operating temperature range		
LM193/193A	-55 to +125	°C
LM293/293A	-25 to +85	°C
LM393/393A	0 to +70	°C
LM2903	-40 to +85	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering 10 sec.)	300	°C

EQUIVALENT CIRCUIT



LOW POWER DUAL VOLTAGE COMPARATOR LM193/A/293/A/393/A/2903

DC ELECTRICAL CHARACTERISTICS $V_+ = 5V_{dc}$, LM193/193A: $-55^\circ C \leq T_A \leq +125^\circ C$ unless otherwise specified.
 LM293/293A: $-25^\circ C \leq T_A \leq +85^\circ C$ unless otherwise specified.
 LM393/393A: $0^\circ C \leq T_A \leq +70^\circ C$ unless otherwise specified.
 LM2903: $-40^\circ C \leq T_A \leq +85^\circ C$ unless otherwise specified.⁷

PARAMETER	TEST CONDITIONS	LM193A			LM293A/393A			LM2903			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage ⁵	$T_A = 25^\circ C$ Over temp.		± 1.0	± 2.0 ± 4.0		± 1.0	± 2.0 ± 4.0		± 2.0 ± 9	± 7.0 ± 15	mV
V_{CM} Input common mode voltage range ^{6,10}	$T_A = 25^\circ C$ Over temp.	0 0		$V+ - 1.5$ $V+ - 2.0$	0 0		$V+ - 1.5$ $V+ - 2.0$	0 0		$V+ - 1.5$ $V+ - 2.0$	V
V_{IDR} Differential input voltage ⁴	Keep all V_{IN} 's $\geq 0V_{dc}$ (or V-if need)			V+			V+			V+	V
I_B Input bias current ⁸	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25^\circ C$ Over temp.		25	100 300		25	250 400		25 200	250 500	nA
I_{OS} Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25^\circ C$ Over temp.		± 3.0	± 25 ± 100		± 5.0	± 50 ± 150		± 5 ± 50	± 50 ± 200	nA nA
I_{OL} Output sink current	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $V_0 \leq 1.5V_{dc}$, $T_A = 25^\circ C$	6.0	16		6.0	16		6.0	16		mA
I_{OH} Output leakage current	$V_{IN(+)} \geq 1V_{dc}$, $V_{IN(-)} = 0$ $V_0 = 30V_{dc}$ Over temp. $V_0 = 5V_{dc}$, $T_A = 25^\circ C$		0.1	1.0		0.1	1.0		0.1	1.0	μA na
I_{CC} Supply current	$R_L = \infty$ on both comparators. $T_A = 25^\circ C$ $V_+ = 30V$, over temp.		0.8 1	1 2.5		0.8 1	1 2.5		0.8 1	1 2.5	mA
A_V Voltage gain	$R_L \geq 15k\Omega$, $V_+ = 15V_{dc}$, $T_A = 25^\circ C$	50	200		50	200		25	100		V/mV
V_{OL} Saturation voltage	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25^\circ C$ Over temp.		250	400 700		250	400 700		400	400 700	mV
T_{LSR} Large signal response time	$V_{IN} = TTL$ logic swing, $V_{REF} = 1.4V_{dc}$, $V_{RL} = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		300			300			300		ns
T_R Response time ⁹	$V_{RL} = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		1.3			1.3			1.3		μs

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LOW POWER DUAL VOLTAGE COMPARATOR LM193/A/293/A/393/A/2903

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_+ = 5V_{dc}$, LM193/193A: $-55^\circ C \leq T_A \leq +125^\circ C$ unless otherwise specified.
 LM293/293A: $-25^\circ C \leq T_A \leq +85^\circ C$ unless otherwise specified.
 LM393/393A: $0^\circ C \leq T_A \leq +70^\circ C$ unless otherwise specified.
 LM2903: $-40^\circ C \leq T_A \leq +85^\circ C$ unless otherwise specified.⁷

PARAMETER	TEST CONDITIONS	LM193			LM293/393			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Input offset voltage ⁵	$T_A = 25^\circ C$ Over temp.		± 2.0	± 5.0 ± 9.0		± 2.0	± 5.0 ± 9.0	mV
V_{CM} Input common mode voltage range ^{6,10}	$T_A = 25^\circ C$ Over temp.	0 0		$V_{\pm 1.5}$ $V_{\pm 2.0}$	0 0		$V_{\pm 1.5}$ $V_{\pm 2.0}$	V
V_{IDR} Differential input voltage ⁴	Keep all V_{IN} 's $\geq 0V_{dc}$ (or V_- if need)			V_+			V_+	V
I_B Input bias current ⁸	$I_{IN(+)}$ or $I_{IN(-)}$ with output in linear range $T_A = 25^\circ C$ Over temp.		25	100 300		25	250 400	nA
I_{OS} Input offset current	$I_{IN(+)} - I_{IN(-)}$ $T_A = 25^\circ C$ Over temp.		± 3.0	± 25 ± 100		± 5.0	± 50 ± 150	nA nA
I_{OL} Output sink current	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $V_O \leq 1.5V_{dc}$, $T_A = 25^\circ C$	6.0	16		6.0	16		mA
I_{OH} Output leakage current	$V_{IN(+)} \geq 1V_{dc}$, $V_{IN(-)} = 0$ $V_O = 5V_{dc}$, $T_A = 25^\circ C$ $V_O = 30V_{dc}$, over temp.		0.1	1.0		0.1	1.0	nA μA
I_{CC} Supply current	$R_L = \infty$ on both comparators $T_A = 25^\circ C$ $V_+ = 30V$, over temp.		0.8	1 2.5		0.8	1 2.5	mA
A_V Voltage gain	$R_L \geq 15k\Omega$, $V_+ = 15V_{dc}$	50	200		50	200		V/mV
V_{OL} Saturation voltage	$V_{IN(-)} \geq 1V_{dc}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4mA$ $T_A = 25^\circ C$ Over temp.		250	400 700		250	400 700	mV
T_{LSR} Large signal response time	$V_{IN} = TTL$ logic swing, $V_{REF} = 1.4V_{dc}$, $R_L = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		300			300		ns
T_R Response time ⁹	$V_R = 5V_{dc}$, $R_L = 5.1k\Omega$, $T_A = 25^\circ C$		1.3			1.3		μs

NOTES

- For operating at high temperatures, the LM393/393A and LM2903 must be derated based on a $125^\circ C$ maximum junction temperature and a thermal resistance of $175^\circ C/W$ which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/193A/293/293A must be derated based on a $150^\circ C$ maximum junction temperature. The low bias dissipation and the "On-Off" characteristics of the outputs keeps the chip dissipation very small ($P_D \leq 100mW$), provided the output transistors are allowed to saturate.
- Short circuits from the output to V_+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20mA independent of the magnitude of V_+ .
- This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V_+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V_{dc}$.
- Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V_{dc}$ (V_{dc} below the magnitude of the negative power supply, if used).
- At output switch point, $V_O \approx 1.4V_{dc}$, $R_S = 0\Omega$ with V_+ from $5V_{dc}$ to $30V_{dc}$; and over the full input common-mode range ($0V_{dc}$ to $V_+ - 1.5V_{dc}$).
- The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than $0.3V$. The upper end of the common-mode voltage range is $V_+ - 1.5V$, but either or both inputs can go to $30V_{dc}$ without damage.
- With the LM293/293A, all temperature specifications are limited to $-25^\circ C \leq T_A \leq +85^\circ C$ and the LM393/393A, all temperature specifications are limited to $0^\circ C \leq T_A \leq +70^\circ C$. The LM2903 is limited to $-40^\circ C \leq T_A \leq +85^\circ C$.
- The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- The response time specified is for a $100mV$ input step with a $5mV$ overdrive.
- For input signals that exceed V_{CC} , only the overdriven comparator is affected. With a $5V$ supply, V_{IN} should be limited to $25V$ max., and a limiting resistor should be used on all inputs that might exceed the positive supply.

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP

NE/SE521

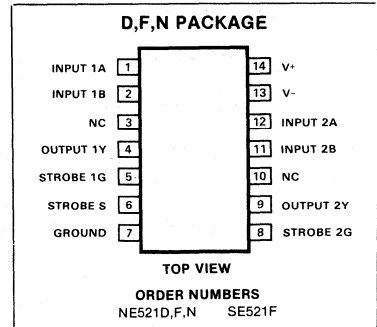
FEATURES

- 12ns maximum guaranteed propagation delay
- 20 μ A maximum input bias current
- TTL compatible strobes and outputs
- Large common mode input voltage range
- Operates from standard supply voltages
- Military qualifications pending

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver

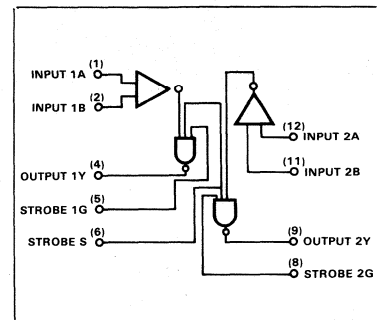
PIN CONFIGURATION



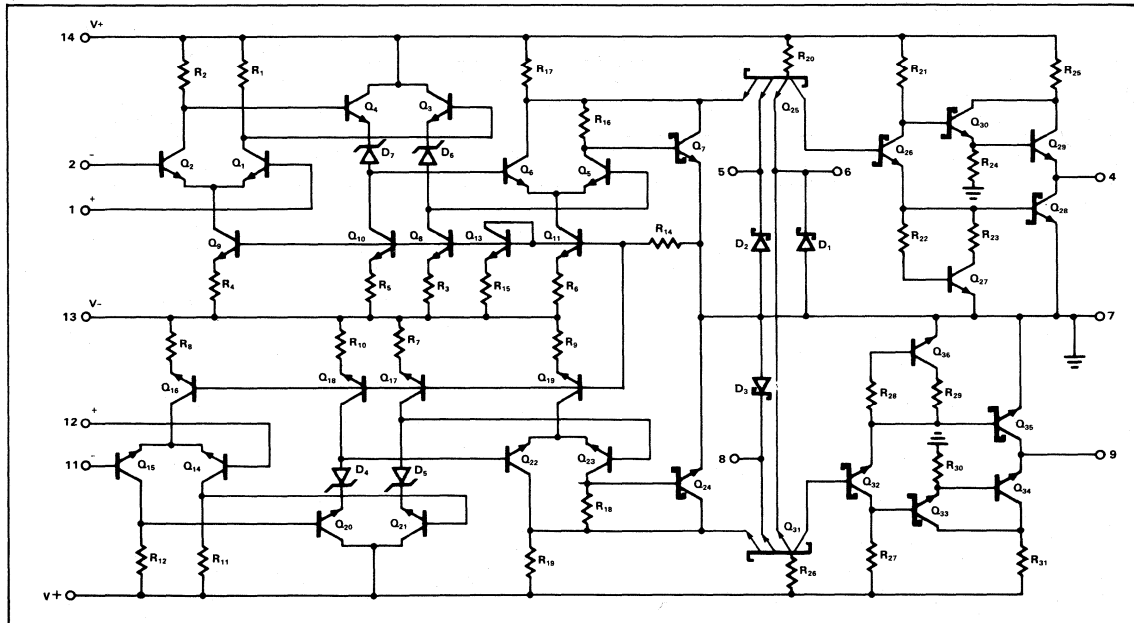
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		V
V+ Positive	+7	
V- Negative	-7	
V _{IDR} Differential input voltage	± 6	V
V _{IN} Input voltage		V
Common mode	± 5	
Strobe/gate	+5.25	
P _D Power dissipation	600	mW
T _A Operating temperature range		$^{\circ}$ C
NE521	0 to 70	
SE521	-55 to +125	
T _{stg} Storage temperature range	-65 to +150	$^{\circ}$ C
Lead temperature	+300	$^{\circ}$ C
(solder, 60 sec)		

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP

NE/SE521

DC ELECTRICAL CHARACTERISTICS $V_+ = +5V$, $V_- = -5V$, $T_A = -55$ to $+125^\circ C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE LIMITS			UNITS	
		Min	Typ	Max		
V_{OS}	Input offset voltage At 25°C Over temperature range		6	7.5 15	mV	
I_{BIAS}	Input bias current At 25°C Over temperature range		7.5	20 40	μA	
I_{OS}	Input offset current At 25°C Over temperature range		1.0	5 12	μA	
V_{CM}	Common mode voltage range	± 3			V	
V_{IL}	Low level input voltage At 25°C Over temperature			0.8 0.7	V	
V_{IH}	High level input voltage	2.0			V	
I_{IH}	Input current High	$V_+ = +5.5V$, $V_- = -5.5V$ $V_{IH} = 2.7V$ 1G or 2G strobe Common strobe S		50 100	μA μA	
I_{IL}	Low	$V_{IL} = 0.5V$ 1G or 2G strobe Common strobe S		-2.0 -4.0	mA mA	
V_{OH} V_{OL}	Output voltage High Low	$V_{I(S)} = 2.0V$ $V_+ = +4.5V$, $V_- = -4.5V$, $I_{LOAD} = -1mA$ $V_+ = +4.5V$, $V_- = -4.5V$, $I_{LOAD} = 10mA$ $T_A = 25^\circ C$, $I_{LOAD} = 20mA$	2.5	3.4	0.5 0.5	V
V_+ V_-	Supply voltage Positive Negative		4.5 -4.5	5.0 -5.0	5.5 -5.5	V
I_{CC+} I_{CC-}	Supply current Positive Negative	$V_+ = 5.5V$, $V_- = -5.5V$, $T_A = 25^\circ C$		27 -15	35 -28	mA
I_{SC}	Short circuit output current		-35		-115	mA

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP

NE/SE521

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_+ = +5V$, $V_- = -5V$, $T_A = 0$ to $70^\circ C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	NE LIMITS			UNITS	
		Min	Typ	Max		
V_{OS}	Input offset voltage At $25^\circ C$ Over temperature range	$V_+ = +4.75V$, $V_- = -4.75V$		6	7.5 10	mV
I_{BIAS}	Input bias current At $25^\circ C$ Over temperature range	$V_+ = +5.25V$, $V_- = -5.25V$		7.5	20 40	μA
I_{OS}	Input offset current At $25^\circ C$ Over temperature range	$V_+ = +5.25V$, $V_- = -5.25V$		1.0	5 12	μA
V_{CM}	Common mode voltage range	$V_+ = +4.75V$, $V_- = -4.75V$	± 3			V
I_{IH}	Input current High	$V_+ = +5.25V$, $V_- = -5.25V$ $V_{IH} = 2.7V$ 1G or 2G strobe Common strobe S			50 100	μA μA
I_{IL}	Low	$V_{IL} = 0.5V$ 1G or 2G strobe Common strobe S			-2.0 -4.0	mA mA
V_{OH} V_{OL}	Output voltage High Low	$V_{I(S)} = 2.0V$ $V_+ = +4.75V$, $V_- = -4.75V$, $I_{LOAD} = -1mA$ $V_+ = +5.25V$, $V_- = -5.25V$, $I_{LOAD} = 20mA$	2.7	3.4	0.5	V
V_+ V_-	Supply voltage Positive Negative		4.75 -4.75	5.0 -5.0	5.25 -5.25	V
I_{CC+} I_{CC-}	Supply current Positive Negative	$V_+ = 5.25V$, $V_- = -5.25V$, $T_A = 25^\circ C$		27 -15	35 -28	mA
I_{SC}	Short circuit output current		-40		-100	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C$, $R_L = 280 \Omega$, $C_L = 15pF$, $V_+ = +5V$, $V_- = -5V$

PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
			Min	Typ	Max	
Large Signal Switching Speed						
Propagation delay						ns
$t_{PLH(D)}$	Low to high ¹	Amp		8	12	
$t_{PHL(D)}$	High to low ¹	Amp		6	9	
$t_{PLH(S)}$	Low to high ²	Strobe		4.5	10	
$t_{PHL(S)}$	High to low ²	Strobe		3.0	6	
Maximum operating frequency			40	55		MHz

NOTES

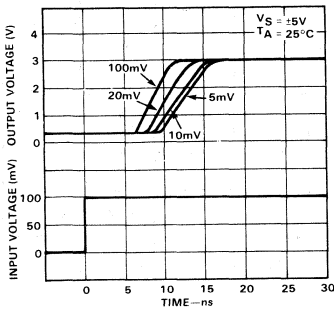
- Response time measured from 0V point of $\pm 100mV$ p-p 10MHz square wave to the 1.5V point of the output
- Response time measured from 1.5V point of input to 1.5V point of the output

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP

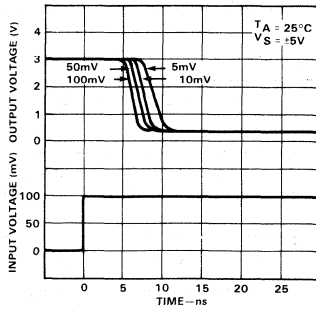
NE/SE521

TYPICAL PERFORMANCE CHARACTERISTICS

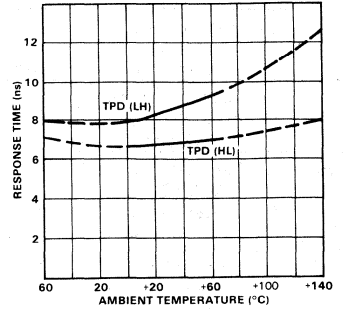
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



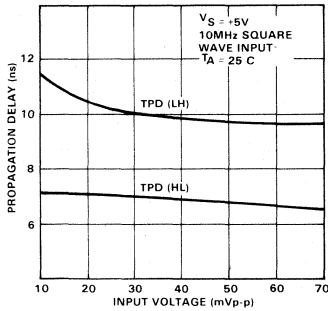
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



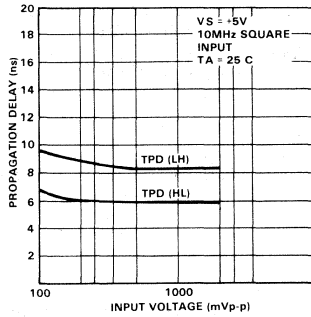
RESPONSE TIME vs TEMPERATURE



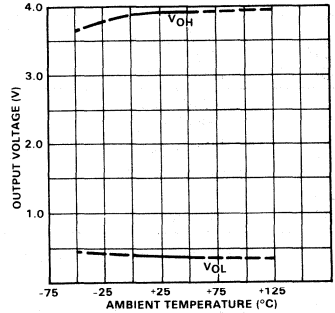
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGE



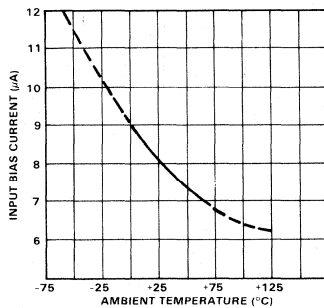
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



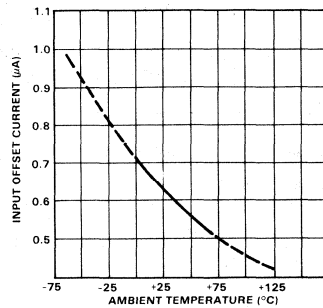
OUTPUT VOLTAGE vs AMBIENT TEMPERATURE



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP

NE/SE522

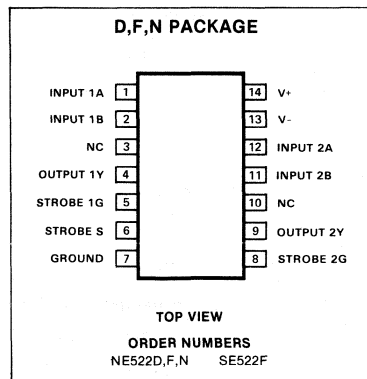
FEATURES

- 15ns maximum guaranteed propagation delay
- 20 μ A maximum input bias current
- TTL compatible strobes and outputs
- Open collector output for wire-OR'd applications
- Large common mode input voltage range
- Operates from standard supply voltages

APPLICATIONS

- MOS memory sense amp
- A-to-D conversion
- High speed line receiver

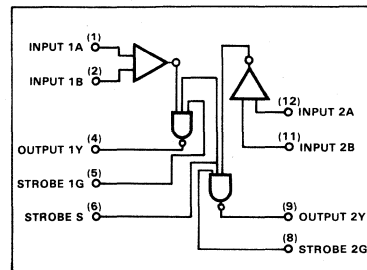
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

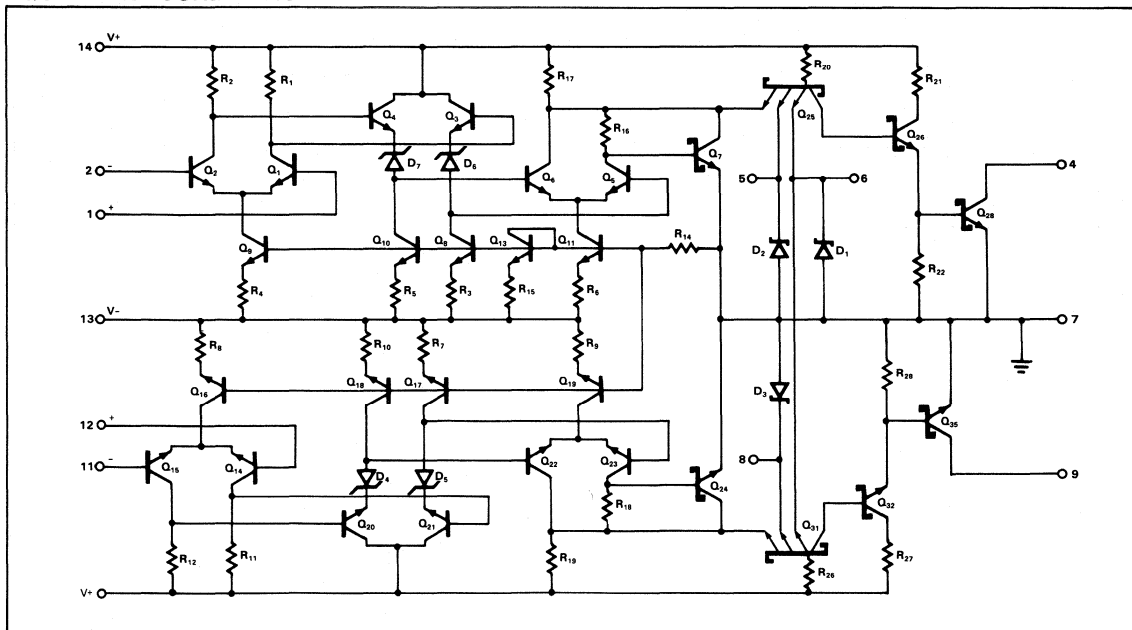
PARAMETER	RATING	UNIT	
V+	Supply voltage Positive	+7	V
V-	Negative	-7	V
VIDR	Differential input voltage	± 6	V
VIN	Input voltage Common mode	± 5	V
	Strobe/gate	± 5.25	V
PD	Power dissipation	600	mW
TA	Operating temperature range NE	0 to 70	$^{\circ}$ C
	SE	-55 to +125	$^{\circ}$ C
Tstg	Storage temperature range Lead temperature (solder, 60 sec)	-65 to +150 +300	$^{\circ}$ C

BLOCK DIAGRAM



8

EQUIVALENT SCHEMATIC



HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP

NE/SE522

DC ELECTRICAL CHARACTERISTICS $\pm 5V \pm 10\%$, $T_A = -55$ to 125°C unless otherwise specified

PARAMETER	TEST CONDITIONS	SE LIMITS			UNIT
		Min	Typ	Max	
V_{OS} Input offset voltage At 25°C Over temperature range	$V_+ = +4.5V$, $V_- = -4.5V$		6	7.5 15.	mV
I_{BIAS} Input bias current At 25°C Over temperature range	$V_+ = +5.5V$, $V_- = -5.5V$		7.5	20. 40.	μA
I_{OS} Input offset current At 25°C Over temperature range	$V_+ = +5.5V$, $V_- = -5.5V$		1.0	5. 12.	μA
V_{CM} Common mode voltage range	$V_+ = +4.5V$, $V_- = -4.5V$	± 3			V
V_{IL} Low level input Voltage at 25°C over temperature				.08 .07	V
V_{IH} High level temperature		2.0			V
I_{IH} Input current High	$V_+ = +5.5V$, $V_- = -5.5V$ $V_{IH} = 2.7V$ 1G or 2G strobe Common strobe S			50 100	μA μA
I_{IL} Input current Low	$V_{IL} = 0.5V$ 1G 2G strobe Common strobe S			-2 -4	mA mA
V_{OL} Output voltage Low	$V_+ = +4.5V$, $V_- = -4.5V$ $I_{OL} = 20\text{mA}$, $T_A = 25^\circ\text{C}$ $I_{OL} = 10\text{mA}$.5 .5	V
I_{OH} Output current High	$V_{CC+} = +4.5$, $V_{CC-} = -4.5V$, $V_{OH} = 5.5V$			250	μA
V_+ Supply voltage Positive V_- Negative		4.5 -4.5	5.0 -5.0	5.5 -5.5	V
I_{CC+} Supply current Positive I_{CC-} Negative	$V_+ = 5.5V$, $V_- = -5.5V$		27 -15	35 -28	mA

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP

NE/SE522

DC ELECTRICAL CHARACTERISTICS (Cont'd) $\pm 5V \pm 5\%$, $T_A = 0$ to $70^\circ C$ unless otherwise specified

PARAMETER	TEST CONDITIONS	NE LIMITS			UNIT
		Min	Typ	Max	
V_{OS} Input offset voltage At $25^\circ C$ Over temperature range	$V_+ = +4.75V$, $V_- = -4.75V$		6	7.5 10	mV
I_{BIAS} Input bias current At $25^\circ C$ Over temperature range	$V_+ = +5.25V$, $V_- = -5.25V$		7.5	20 40	μA
I_{OS} Input offset current At $25^\circ C$ Over temperature range	$V_+ = +5.25V$, $V_- = -5.25V$		1.0	5 12	μA
V_{CM} Common mode voltage range	$V_+ = +4.75V$, $V_- = -4.75V$	± 3			V
I_{IH} Input current High	$V_+ = +5.25V$, $V_- = -5.25V$ $V_{IH} = 2.7V$ 1G or 2G strobe Common strobe S			50 100	μA μA
I_{IL} Low	$V_{IL} = 0.5V$ 1G 2G strobe Common strobe S			-2.0 -4.0	mA mA
V_{OL} Output voltage Low	$V_+ = +5.25V$, $V_- = -5.25V$, $V_I(S) = 2.0V$ $I_{LOAD} = 20mA$			0.5	V
I_{OH} Output current High	$V_{CC+} = +4.75$, $V_{CC-} = -4.75V$, $V_{OH} = 5.25V$			250	μA
V_+ Supply voltage Positive V_- Negative		4.75 -4.75	5.0 -5.0	5.25 -5.25	V
I_{CC+} Supply current Positive I_{CC-} Negative	$V_+ = 5.25V$, $V_- = -5.25V$, $T_A = 25^\circ C$		27 -15	50 -28	mA

8

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C$, $R_L = 280\Omega$, $C_L = 15pF$

PARAMETER	FROM INPUT	TO OUTPUT	LIMITS			UNIT
			Min	Typ	Max	
Input resistance				4		$k\Omega$
Input capacitance				3		pF
Large Signal Switching Speed Propagation delay						ns
$t_{PLH}(D)$ Low to high ¹	Amp	Output		10	15	
$t_{PHL}(D)$ High to low ¹	Amp	Output		8	12	
$t_{PLH}(S)$ Low to high ²	Strobe	Output		6	13	
$t_{PHL}(S)$ High to low ²	Strobe	Output		5	9	
Maximum operating frequency			25	35		MHz

NOTES

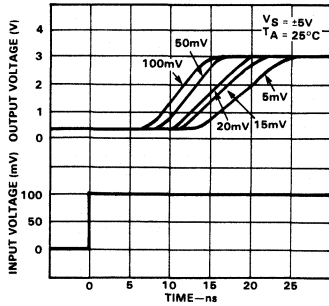
- Response time measured from 0V point of $\pm 100mV$ p-p 10MHz square wave to the 1.5V point of the output
- Response time measured from 1.5V point of input to 1.5V point of the output

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP

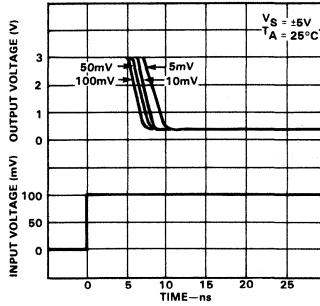
NE/SE522

TYPICAL PERFORMANCE CHARACTERISTICS

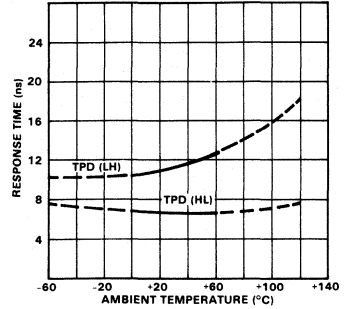
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



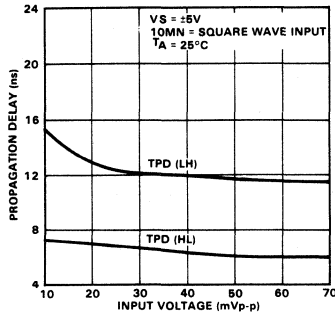
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



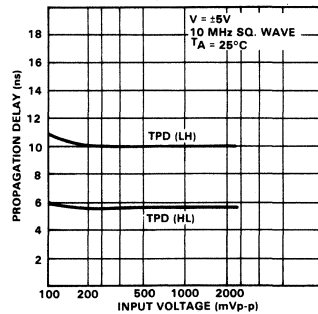
RESPONSE TIME vs TEMPERATURE



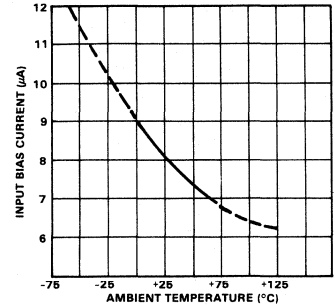
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



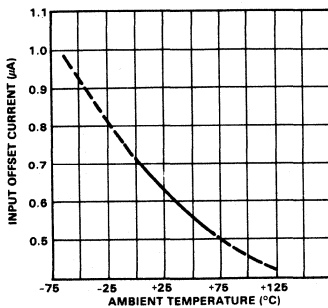
PROPAGATION DELAY FOR VARIOUS INPUT VOLTAGES



INPUT BIAS CURRENT vs AMBIENT TEMPERATURE



INPUT OFFSET CURRENT vs AMBIENT TEMPERATURE



VOLTAGE COMPARATOR

NE/SE527

DESCRIPTION

The SE/NE527 is a high speed analog voltage comparator which, in the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T2L gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

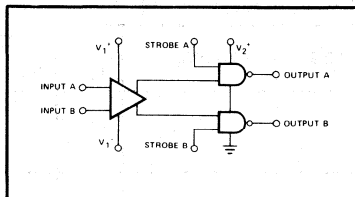
FEATURES

- 15ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common mode and differential voltage range
- MII std 883A,B,C available

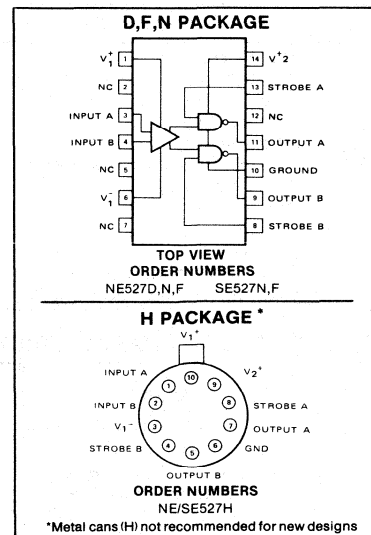
APPLICATIONS

- A/D conversion
- ECL to TTL interface
- TTL to ECL interface
- Memory sensing
- Optical data coupling

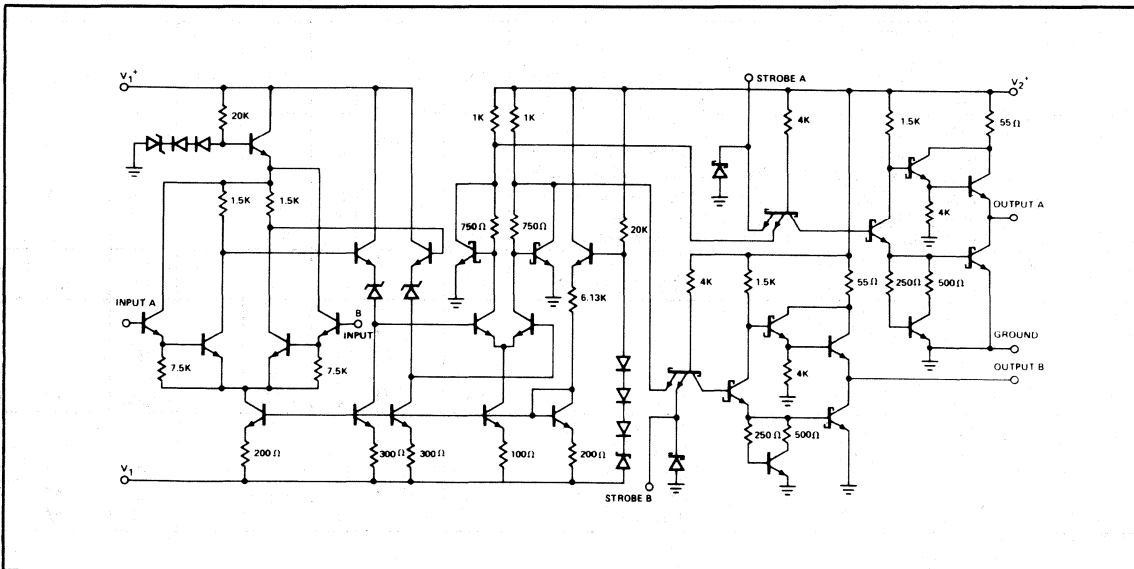
BLOCK DIAGRAM



PIN CONFIGURATIONS



EQUIVALENT SCHEMATIC



VOLTAGE COMPARATOR

NE/SE527

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+7	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE527	0 to +70	°C
SE527	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

DC ELECTRICAL CHARACTERISTICS $V_{1+} = 10V, V_{1-} = -10V, V_{2+} = +5.0V$

PARAMETER	TEST CONDITIONS	SE527			NE527			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS								
Input offset voltage @ 25°C				4			6	mV
Over temperature range				6			10	mV
Input bias current @ 25°C				2			2	μA
Over temperature range				4			4	μA
Input offset current @ 25°C	$V_{IN} = 0V$			0.5			0.75	μA
Over temperature range				1			1	μA
GATE CHARACTERISTICS								
Output voltage								
"1" State	$V_{2+} = 4.75V, I_{SOURCE} = -1mA$ $V_{2+} = 4.75V, I_{SINK} = 10mA$	2.5	3.3		2.7	3.3		V
"0" State				0.5			0.5	V
Strobe inputs								
"0" Input current ¹	$V_{2+} = 5.25V, V_{STROBE} = 0.5V$			-2			-2	mA
"1" Input current @ 25°C ¹	$V_{2+} = 5.25V, V_{STROBE} = 2.7V$			50			100	μA
Over temperature range	$V_{2+} = 5.25V, V_{STROBE} = 2.7V$			200			200	μA
"0" Input voltage	$V_{2+} = 4.75V$			0.8			0.8	V
"1" Input voltage	$V_{2+} = 4.75V$	2.0			2.0			V
Short circuit								
Output current	$V_{2+} = 5.25V, V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS								
Supply voltage								
V1+		5		10	5		10	V
V1-		-6		-10	-6		-10	V
V2+		4.5	5	5.5	4.75	5	5.25	V
Supply current	$V_{1+} = 10V, V_{1-} = -10V$ $V_{2+} = 5.25V$							
I1+	Over temp.			5			5	mA
I1-	Over temp.			10			10	mA
I2+	Over temp.			20			20	mA

NOTES

1. Strobe input current test conditions

INPUT A (VIN)	INPUT B	STROBE A	STROBE B
> V Offset	GND	Measure	IIH
< V Offset	GND	Measure	IIL

2. Parameters are guaranteed over the temperature range unless otherwise specified.

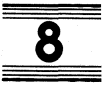
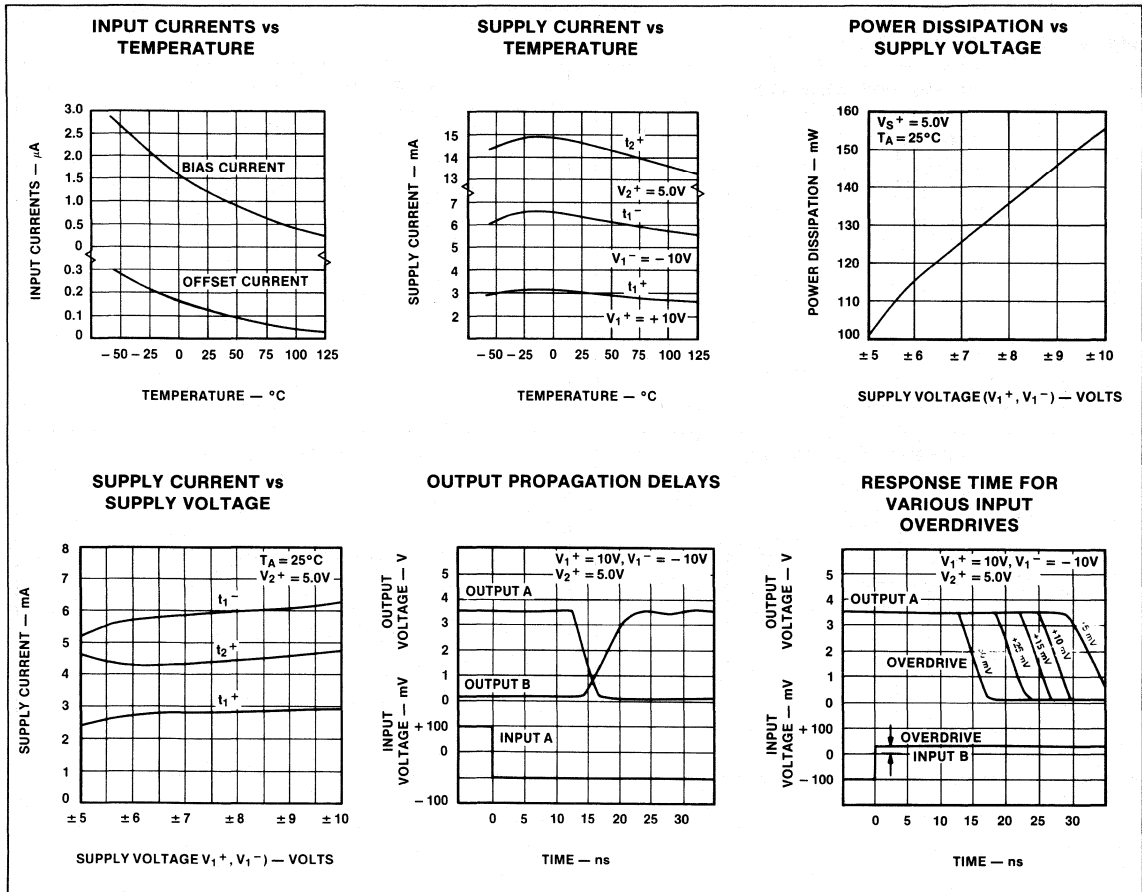
VOLTAGE COMPARATOR

NE/SE527

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response propagation delay time t_{PLH} t_{PHL}	$V_{IN} = \pm 100\text{mV}$ step		16	26	ns
			14	24	ns
Delay between output A and B			2	5	ns
Strobe delay time t_{on} Turn-on time t_{off} Turn-off time			6		ns
			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS



VOLTAGE COMPARATOR

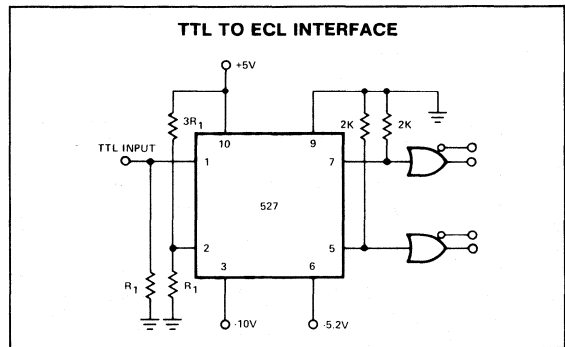
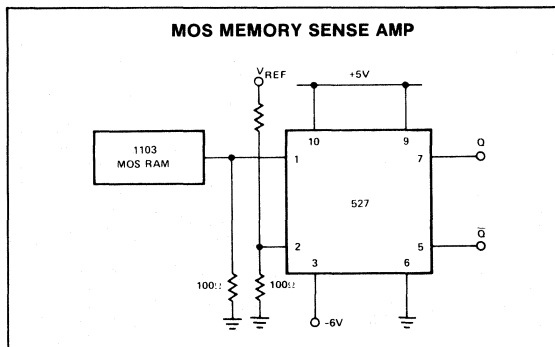
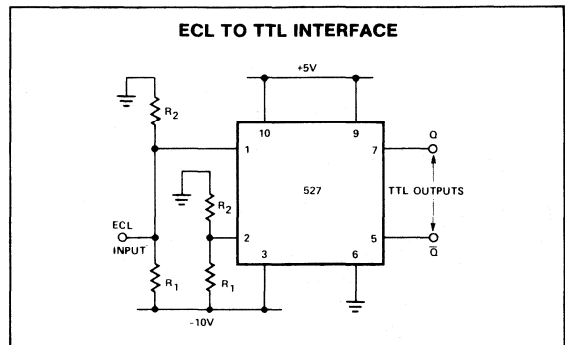
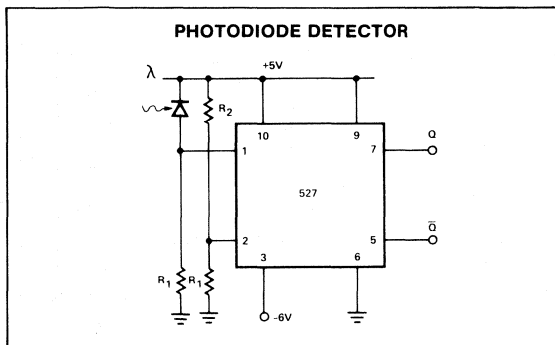
NE/SE527

APPLICATIONS

One of the main features of the device is that supply voltages (V_{1+} , V_{1-}) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V_{1-}) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V_{1+} and V_{1-}) up to a maximum of ± 6 volts as supply voltages are increased.

It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS



VOLTAGE COMPARATOR

NE/SE529

DESCRIPTION

The SE/NE529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip.

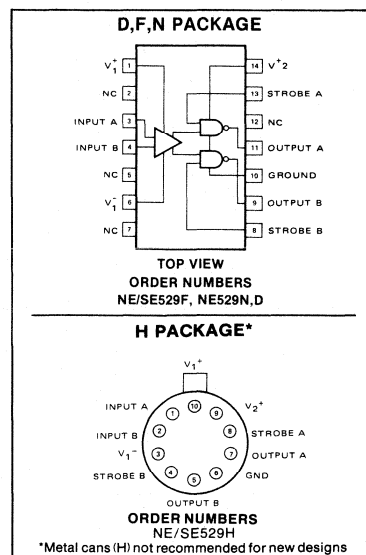
FEATURES

- 10ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common mode and differential voltage range

APPLICATIONS

- A/D conversion
- ECL to TTL interface
- TTL to ECL interface
- Memory sensing
- Optical data coupling
- Mil std 883A,B,C available

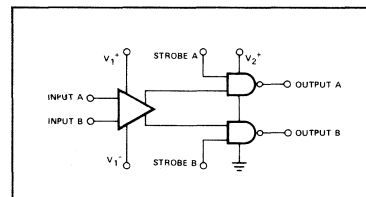
PIN CONFIGURATION



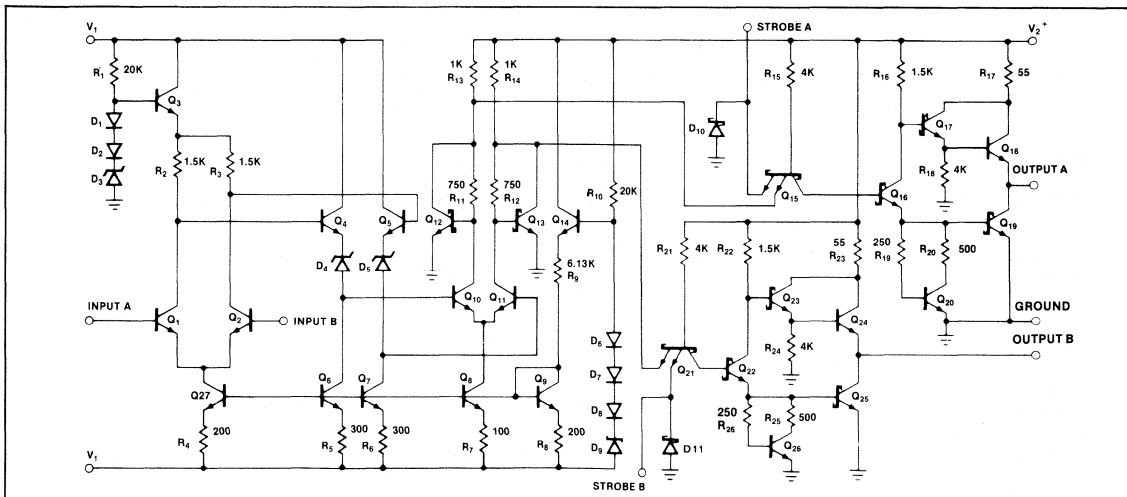
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+7	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE529	0 to +70	°C
SE529	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



VOLTAGE COMPARATOR

NE/SE529

DC ELECTRICAL CHARACTERISTICS $V_{1+} = +10V, V_{2+} = +5.0V, V_{1-} = -10V$

PARAMETER	TEST CONDITIONS	SE529			NE529			UNIT
		Min	Typ	Max	Min	Typ	Max	
INPUT CHARACTERISTICS Input offset voltage @25°C Over temperature range				4 6			6 10	mV mV
	Input bias current @25°C Over temperature range	$V_{IN} = 0V$		5 12 36		5	20 50	μA μA
Input offset current @25°C Over temperature range	$V_{IN} = 0V$		2	3 9		2	5 15	μA μA
GATE CHARACTERISTICS Output voltage "1" state "0" state	$V_{2+} = 4.75V, I_{source} = -1mA$ $V_{2+} = 4.75V, I_{sink} = 10mA$	2.5	3.3		2.7	3.3		V V
				0.5			0.5	
Strobe inputs "0" Input current ¹ "1" Input current @ 25°C ¹ Over temperature range "0" input voltage "1" input voltage	$V_{2+} = 5.25V, V_{strobe} = 0.5V$ $V_{2+} = 5.25V, V_{strobe} = 2.7V$ $V_{2+} = 5.25V, V_{strobe} = 2.7V$ $V_{2+} = 4.75V$ $V_{2+} = 4.75V$			-2 50			-2 100	mA μA
				200			200	μA
		2.0			0.8		0.8	V
			2.0					V
Short circuit Output current	$V_{2+} = 5.25V, V_{OUT} = 0V$	-18		-70	-18		-70	mA
POWER SUPPLY REQUIREMENTS Supply voltage V_{1+} V_{1-} V_{2+}		5 -6 4.5	5	10 -10 5.5	5 -6 4.75	5	10 -10 5.25	V V V
Supply current I_{1+} I_{1-} I_{2+}	$V_{1+} = 10V, V_{1-} = -10V$ $V_{2+} = 5.25V$ Over temp. Over temp. Over temp.							mA mA mA

NOTES

1. Strobe input current test conditions

INPUT A (V_{IN})	INPUT B		STROBE A	STROBE B
> V Offset	GND	Measure	IIL	IIH
< V Offset	GND	Measure	IIH	IIL

2. Parameters are guaranteed over the temperature range unless otherwise specified.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C$

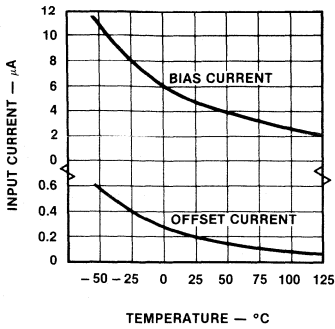
PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Transient response Propagation delay time t_{PLH} t_{PHL}	$V_{IN} = \pm 100mV$ step		12 10	22 20	ns ns
Delay between output A and B			2	5	ns
Strobe delay time t_{ON} turn-on time t_{OFF} turn-off time				6 6	

VOLTAGE COMPARATOR

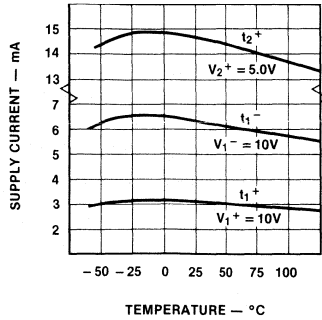
NE/SE529

TYPICAL PERFORMANCE CHARACTERISTICS

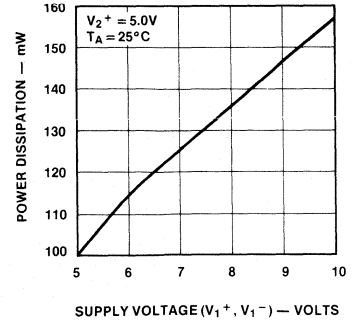
INPUT CURRENTS vs TEMPERATURE



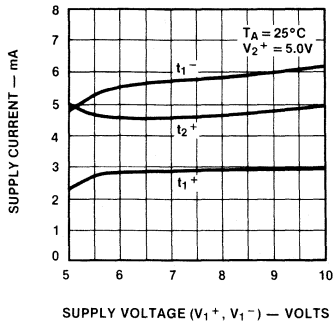
SUPPLY CURRENT vs TEMPERATURE



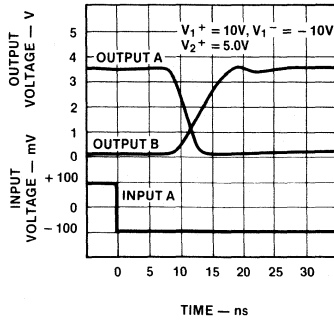
POWER DISSIPATION vs SUPPLY VOLTAGE



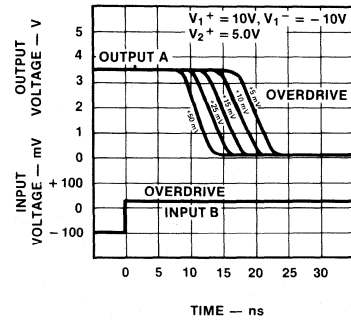
SUPPLY CURRENT vs SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



VOLTAGE COMPARATOR

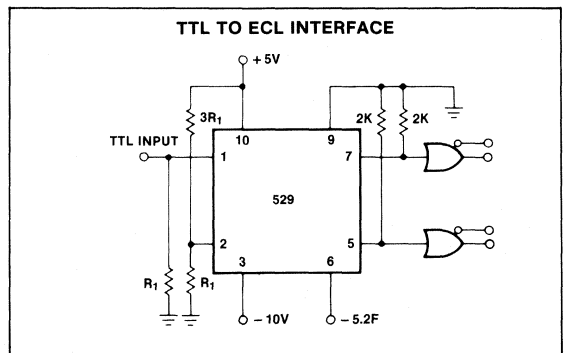
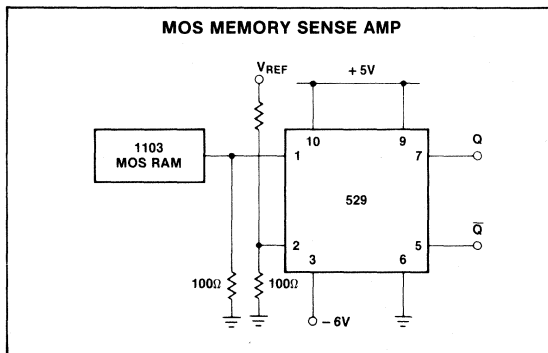
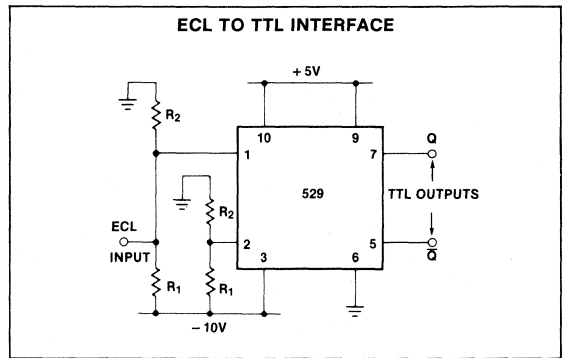
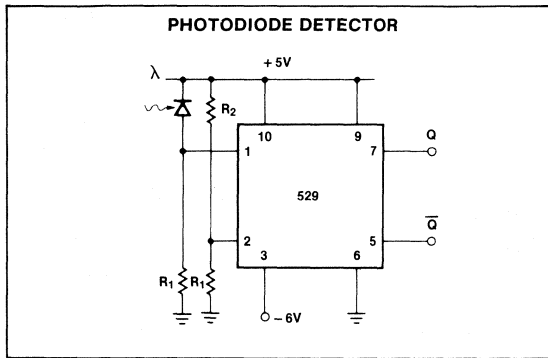
NE/SE529

APPLICATIONS

One of the main features of the device is that supply voltages (V_{1+} , V_{1-}) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V_{1-}) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V_{1+} and V_{1-}) up to a maximum of ± 6 volts as supply voltages are increased.

It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS



Section 9 Interface Products

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Section 9 — Interface Products

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NE5090	Addressable Relay Driver	9-22

DUAL LINE RECEIVER

DS7820/DS8820

DESCRIPTION

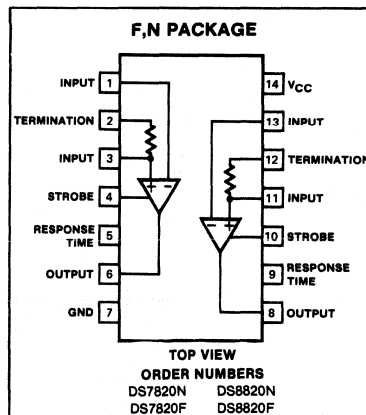
The DS7820, specified from -55°C to 125°C, and the DS8820, specified from 0°C to 70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

FEATURES

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Independent channel strobing
- High input resistance
- Fanout of two with DTL or TTL
- Output can be wire OR'ed
- DS7820 MII std 883A,B,C available

PIN CONFIGURATION



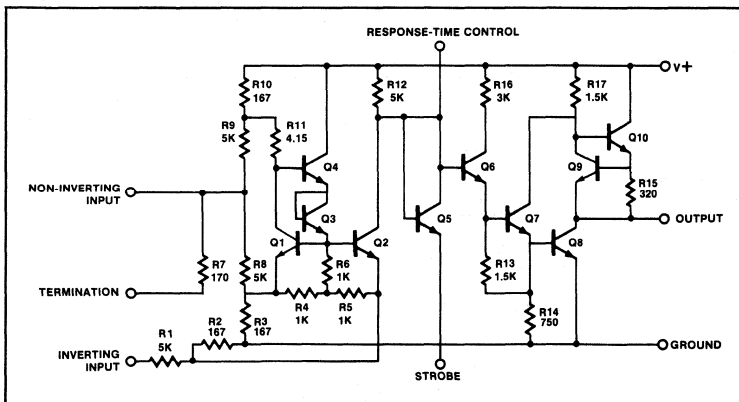
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	8.0	V
Input voltage	±20	V
Differential input voltage	±20	V
Strobe voltage	8.0	V
Output sink current	25	mA
Power dissipation	600	mW
Operating temperature range		
DS7820	-55 to +125	°C
DS8820	0 to 70	°C
Lead temperature (soldering, 10sec)	300	°C

NOTE

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

CIRCUIT SCHEMATIC



DUAL LINE RECEIVER

DS7820/DS8820

DC ELECTRICAL CHARACTERISTICS

Specifications apply for $4.5V \leq V_{CC} \leq 5.5$,
 $-15V \leq V_{CM} \leq 15V$ and $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ for the DS7820
 or $0^{\circ}C \leq T_A \leq +70^{\circ}C$ for the DS8820 unless otherwise specified.
 Typical values given are for $V_{CC} = 5.0V$, $T_A = 25^{\circ}C$ and $V_{CM} = 0V$
 unless stated differently.^{1,2,3}

PARAMETER	TEST CONDITIONS	DS7820			DS8820			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{TH} Input threshold	$V_{IN} = 0V$	-0.5	0	0.5	-0.5	0	0.5	V
V_{TH} Input threshold	$-15V \leq V_{IN} \leq 15V$	-1.0	0	1.0	-1.0	0	1.0	V
V_{OH} High output level	$I_{OUT} \leq -0.2mA$	2.5		5.5	2.5		5.5	V
V_{OL} Low output level	$I_{SINK} \leq 3.5mA$	0		0.4	0		0.4	V
R_{IN-} Inverting input resistance		3.6	5.0		3.6	5.0		k Ω
R_{IN+} Noninverting input resistance		1.8	2.5		1.8	2.5		k Ω
R_T Line termination resistance		120	170	250	120	170	250	Ω
I_{ST} Strobe current	$V_{Strobe} = 0.4V$		1.0	1.4		1.0	1.4	mA
I_{ST} Strobe current	$V_{Strobe} = 5.5V$			-5			-5	μA
I_{CC} Supply current ³	$V_{IN} = 15V$		3.2	6.0		3.2	6.0	mA
I_{CC} Supply current ³	$V_{IN} = 0V$		5.8	10.2		5.8	10.2	mA
I_{CC} Supply current ³	$V_{IN} = -15V$		8.3	15.0		8.3	15.0	mA
I_{IN+} Noninverting input current	$V_{IN} = 15V$		3.0	7.0		5.0	7.0	mA
I_{IN+} Noninverting input current	$V_{IN} = 0V$	-1.6	-1.0		-1.6	-1.0		mA
I_{IN+} Noninverting input current	$V_{IN} = -15V$	-9.8	-7.0		-9.8	-7.0		mA
I_{IN-} Inverting input current	$V_{IN} = 15V$		3.0	4.2		3.0	4.2	mA
I_{IN-} Inverting input current	$V_{IN} = 0V$		0	-0.5		0	-0.5	mA
I_{IN-} Inverting input current	$V_{IN} = -15V$	-4.2	-3.0		-4.2	-3.0		mA

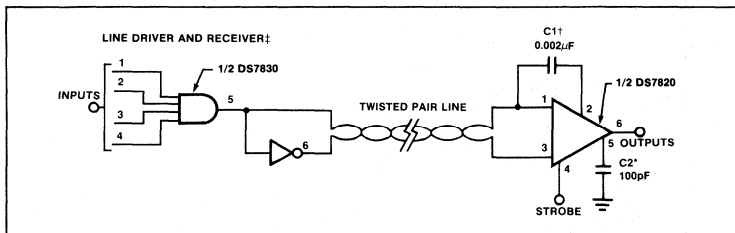
NOTES

- All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
- Only one output at a time should be shorted.
- The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	DS7820			DS8820			UNIT
		Min	Typ	Max	Min	Typ	Max	
T_R Response time	$C_{delay} = 0$		40			40		ns
T_R Response time	$C_{delay} = 100pF$		150			150		ns

DS7820-DS8820 TYPICAL APPLICATION



†Exact value depends on line length

‡ V_{CC} is 4.5V to 5.5V for both the DS7820 and DS7830

*Optional to control response time

DUAL LINE RECEIVER

DS7820A/DS8820A

DESCRIPTION

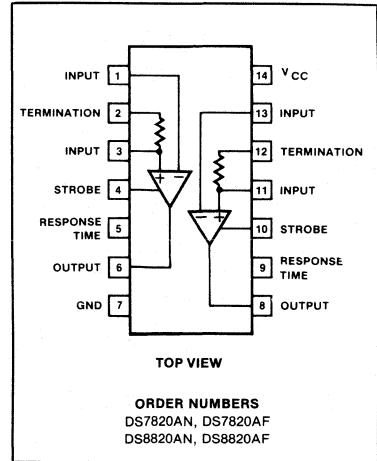
The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (-55°C to 125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

FEATURES

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with either DTL or TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

PIN CONFIGURATION



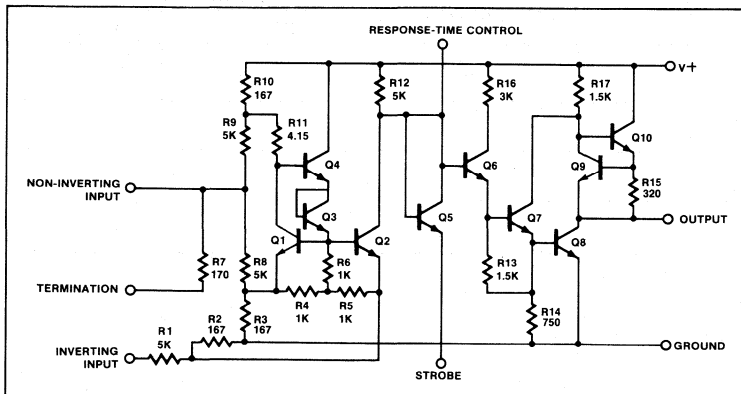
ABSOLUTE MAXIMUM RATINGS*

PARAMETER	RATING	UNIT
Supply voltage	8.0	V
Input voltage	±20	V
Differential input voltage	±20	V
Strobe voltage	8.0	V
Output sink current	50	mA
Power dissipation	600	mW
Operating temperature range		
DS7820A	-55 to +125	°C
DS8820A	0 to +70	°C
Lead temperature (soldering, 60sec)	300	°C

*NOTE

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

EQUIVALENT SCHEMATIC



DUAL LINE RECEIVER

DS7820A/DS8820A

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.1,2,3,4

PARAMETER	TEST CONDITIONS	DS7820A/DS8820A			UNIT	
		Min	Typ	Max		
V_{TH} Differential threshold voltage	$I_{OUT} = -400\mu\text{A}$		0.06	0.5	V	
	$V_{OUT} \geq 2.5\text{V}$		0.06	1.0	V	
	$I_{OUT} = +16\text{mA}$		-0.08	-0.5	V	
	$V_{OUT} \leq 0.4\text{V}$		-0.08	-1.0	V	
R_{I^-} Inverting input resistance	$-15\text{V} \leq V_{CM} \leq +15\text{V}$	3.6	5		k Ω	
R_{I^+} Non-inverting input resistance	$-15\text{V} \leq V_{CM} \leq +15\text{V}$	1.8	2.5		k Ω	
R_T Line termination resistance		120	170	250	Ω	
I_{I^-} Inverting input current	$V_{CM} = 15\text{V}$		3.0	4.2	mA	
	$V_{CM} = 0\text{V}$		0	-0.5	mA	
	$V_{CM} = -15\text{V}$		-3.0	-4.2	mA	
I_{I^+} Non-inverting input current	$V_{CM} = 15\text{V}$		5.0	7.0	mA	
	$V_{CM} = 0\text{V}$		-1.0	-1.6	mA	
	$V_{CM} = -15\text{V}$		-7.0	-9.8	mA	
I_{CC} Power supply current	$V_{DIFF} = -1\text{V}$, $I_{OUT} = \text{Logical "0"}$ $V_{DIFF} = -0.5\text{V}$,	$V_{CM} = 15\text{V}$ $V_{CM} = -15\text{V}$ $V_{CM} = 0\text{V}$	3.9 9.2 6.5	6.0 14.0 10.2	mA mA mA	
	V_{OH} Logical "1" output voltage	$I_{OUT} = -400\mu\text{A}$, $V_{DIFF} = 1\text{V}$	2.5	4.0	5.5	V
	V_{OL} Logical "0" output voltage	$I_{OUT} = +16\text{mA}$, $V_{DIFF} = -1\text{V}$	0	0.22	0.4	V
V_{SH} Logical "1" strobe input voltage	$I_{OUT} = +16\text{mA}$, $V_{OUT} \leq 0.4\text{V}$, $V_{DIFF} = -3\text{V}$	2.1			V	
	$I_{OUT} = -400\mu\text{A}$, $V_{OUT} \geq 2.5\text{V}$, $V_{DIFF} = -3\text{V}$			0.9	V	
I_{SH} Logical "1" strobe input current	$V_{STROBE} = 5.5\text{V}$, $V_{DIFF} = 3\text{V}$		0.01	5.0	μA	
I_{SL} Logical "0" strobe input current	$V_{STROBE} = 0.4\text{V}$, $V_{DIFF} = -3\text{V}$		-1.0	-1.4	mA	
I_{SC} Output short circuit current	$I_{OUT} = 0\text{V}$, $V_{CC} = 5.5\text{V}$, $V_{STROBE} = 0\text{V}$	-2.8	-4.5	-6.7	mA	

NOTES

- These specifications apply for $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$, $-15\text{V} \leq V_{CM} \leq 15\text{V}$ and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for the DS7820A or $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ for the DS8820A unless otherwise specified. Typical values given are for $V_{CC} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$ and $V_{CM} = 0\text{V}$ unless stated differently.
- All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.
- Only one output at a time should be shorted.
- The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$ unless otherwise specified.

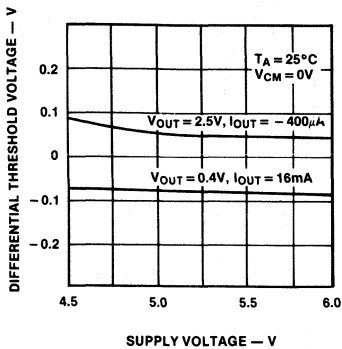
PARAMETER	TEST CONDITIONS	DS7820A/DS8820A			UNIT
		Min	Typ	Max	
t_{PD0} Propagation delay, differential input to "0" output			30	45	ns
t_{PD1} Propagation delay, differential input to "1" output			27	40	ns
t_{PD0} Propagation delay, strobe input to "0" output			16	25	ns
t_{PD1} Propagation delay, strobe input to "1" output			18	30	ns

DUAL LINE RECEIVER

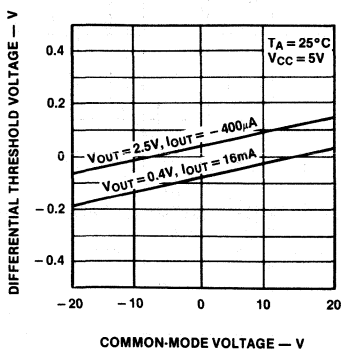
DS7820A/DS8820A

TYPICAL PERFORMANCE CHARACTERISTICS

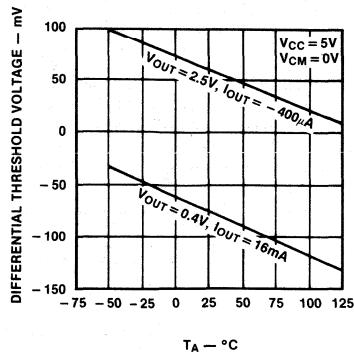
SUPPLY VOLTAGE SENSITIVITY



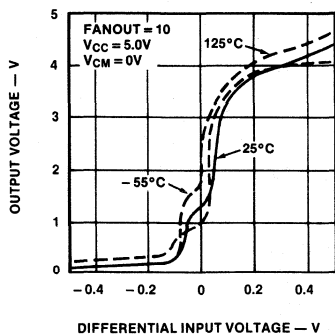
COMMON-MODE VOLTAGE SENSITIVITY



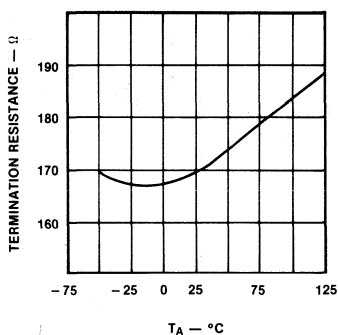
TEMPERATURE SENSITIVITY



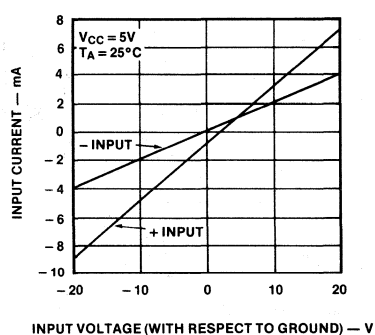
TRANSFER FUNCTION



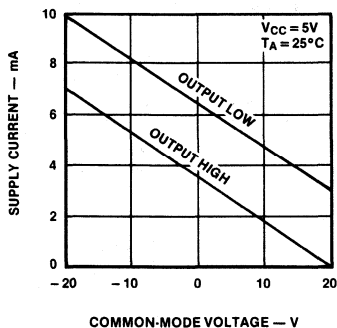
TERMINATION RESISTANCE



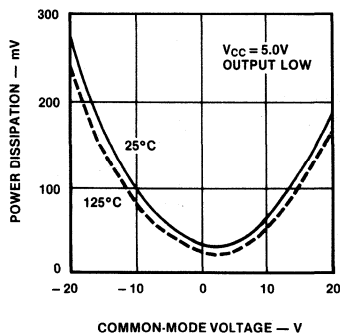
INPUT CHARACTERISTICS



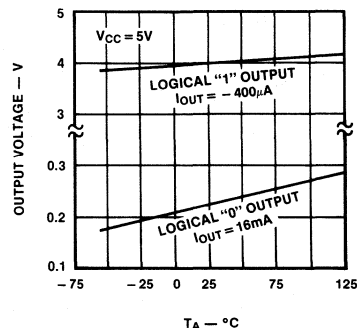
POWER SUPPLY CURRENT



INTERNAL POWER DISSIPATION



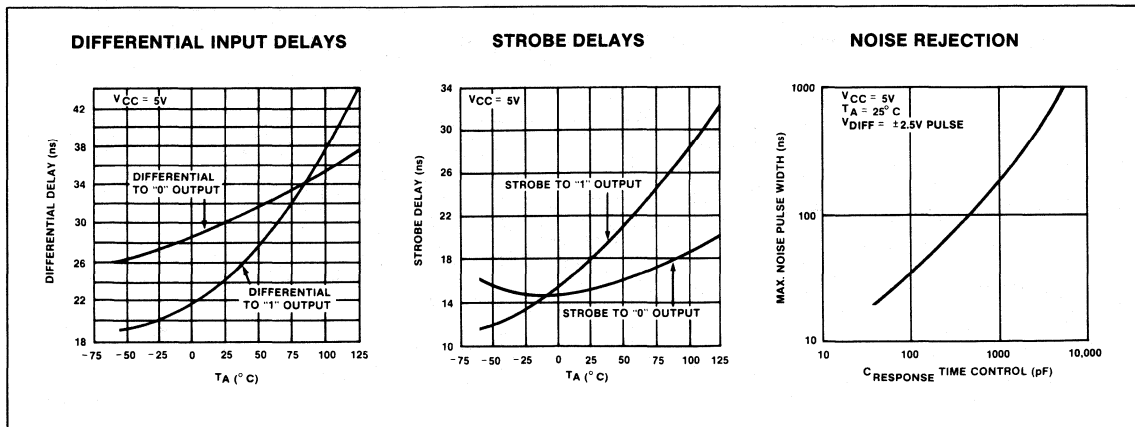
OUTPUT VOLTAGE LEVELS



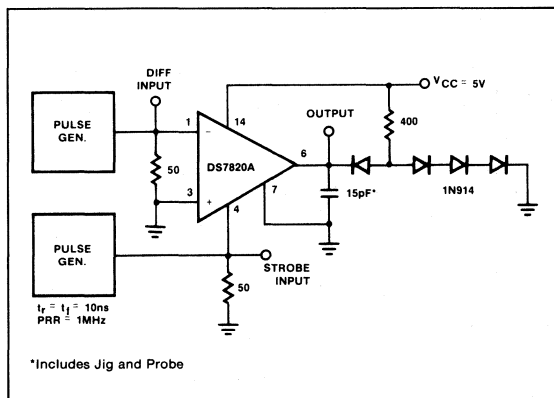
DUAL LINE RECEIVER

DS7820A/DS8820A

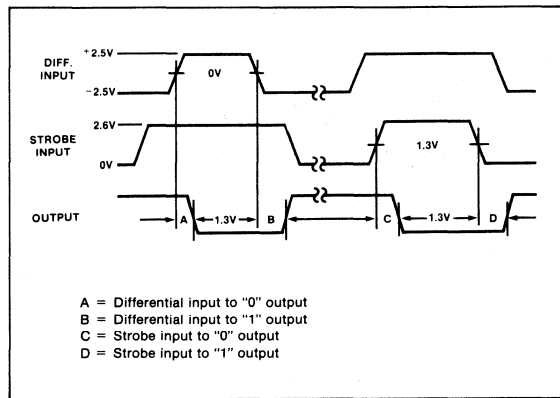
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



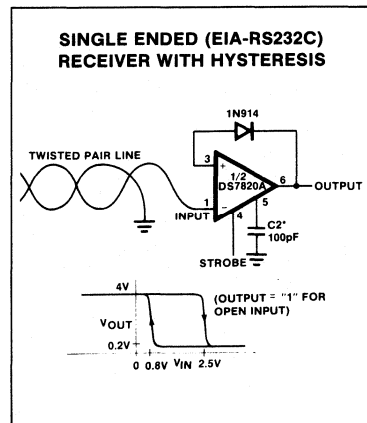
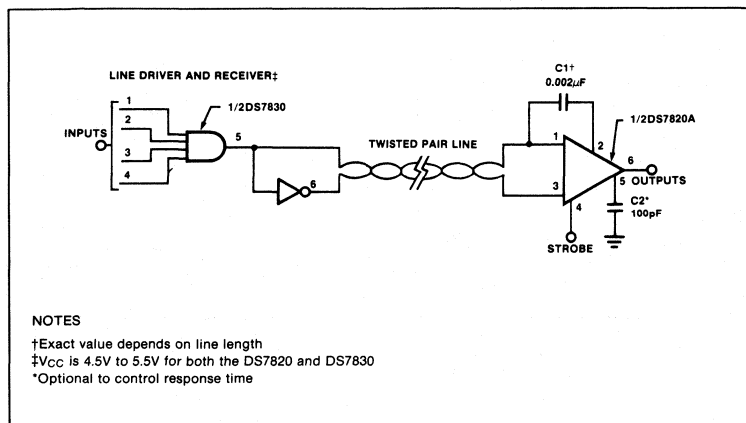
AC TEST CIRCUIT



VOLTAGE WAVEFORM



TYPICAL APPLICATIONS



DUAL DIFFERENTIAL LINE DRIVER

DS7830/DS8830

DESCRIPTION

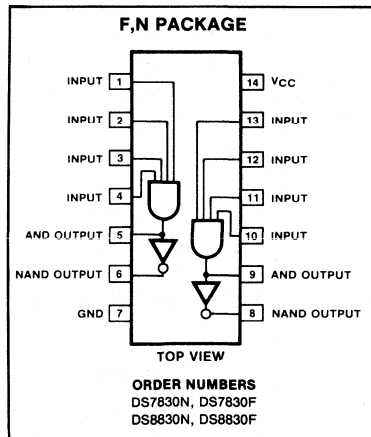
The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

FEATURES

- Single 5 volt power supply
- High speed
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- Short circuit protection
- DS7830 Mil std 883A,B,C available

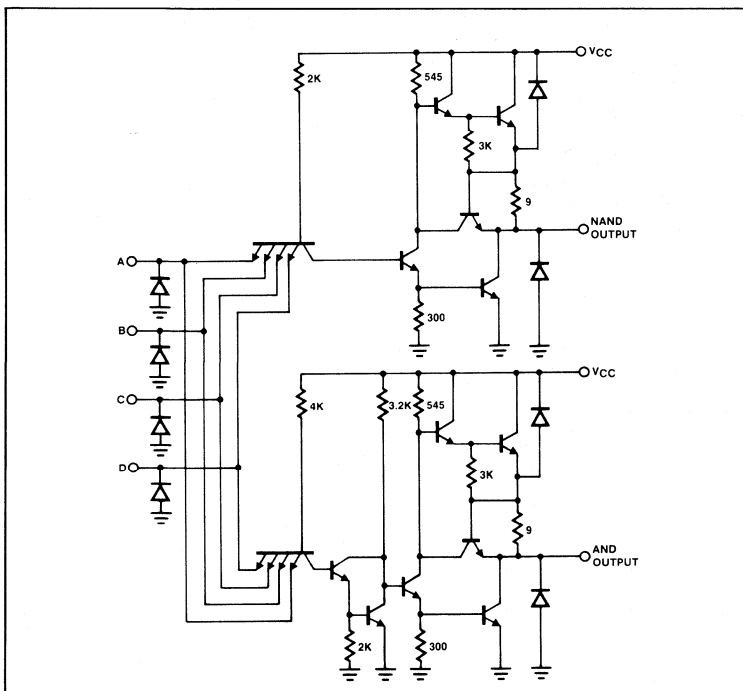
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC}	7.0	V
Input voltage	5.5	V
Operating temperature range		
DS7830	-55 to +125	°C
DS8830	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

EQUIVALENT SCHEMATIC



DUAL DIFFERENTIAL LINE DRIVER

DS7830/DS8830

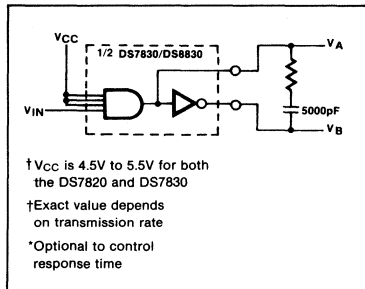
ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ $V_{CC} = 5\text{V}$ unless otherwise specified.^{1,2}

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Logical "1" input voltage		2.0			V
Logical "0" input voltage				0.8	V
Logical "1" output voltage	$V_{IN} = 0.8\text{V}$ $I_{OUT} = -0.8\text{mA}$	2.4			V
Logical "1" output voltage	$V_{IN} = 0.8\text{V}$ $I_{OUT} = -40\text{mA}$	1.8	2.9		V
Logical "0" output voltage	$V_{IN} = 2.0\text{V}$ $I_{OUT} = +32\text{mA}$		0.2	0.4	V
Logical "0" output voltage	$V_{IN} = 2.0\text{V}$ $I_{OUT} = +40\text{mA}$		0.22	0.5	V
Logical "1" input current	$V_{IN} = +2.4\text{V}$			120	μA
Logical "1" input current	$V_{IN} = 5.5\text{V}$			2	mA
Logical "0" input current	$V_{IN} = 0.4\text{V}$			4.8	mA
Output short circuit current ²	$V_{CC} = 5.0\text{V}$	-40	-100	-120	mA
Supply current	$V_{CC} = 5.0\text{V}$ $V_{IN} = 5.0\text{V}$ (Each driver)		11	18	mA
Propagation delay AND gate t_{pd1}	$T_A = 25^\circ\text{C}$		8	12	ns
Propagation delay AND gate t_{pd0}	$V_{CC} = 5.0\text{V}$		11	18	ns
Propagation delay NAND gate t_{pd1}	$CL = 15\text{pF}$		8	12	ns
Propagation delay NAND gate t_{pd0}	See Figure 1		5	8	ns
Differential delay t_1	Load, 100 Ω and 5000pF		12	16	ns
Differential delay t_2	See Figure 2		12	16	ns

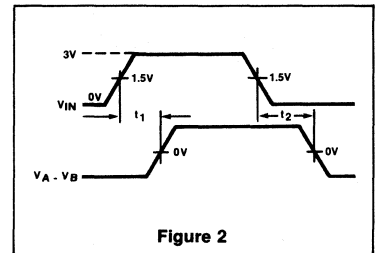
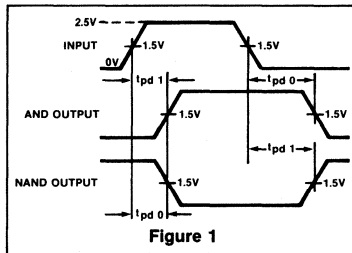
NOTES

- Specifications apply for DS7830 $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 10\%$, DS8830 $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$ unless otherwise specified.
- Applies for $T_A = +125^\circ\text{C}$, only one output at a time to be shorted.

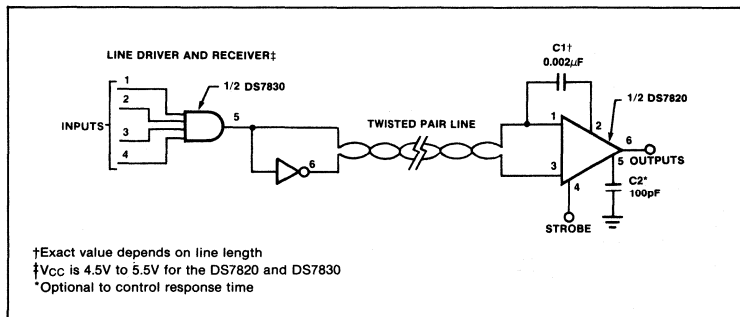
AC TEST CIRCUIT



SWITCHING TIME WAVEFORMS



TYPICAL APPLICATION



QUAD LINE DRIVER

MC1488

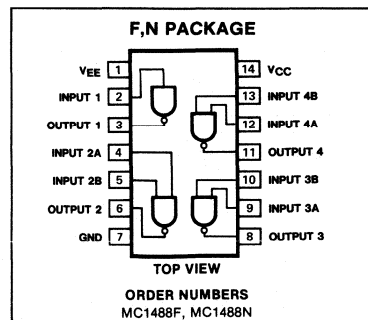
DESCRIPTION

The MC1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V.24.

FEATURES

- Current limited output: $\pm 10\text{mA Typ}$
- Power-off source impedance: $300\Omega \text{ Min}$
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

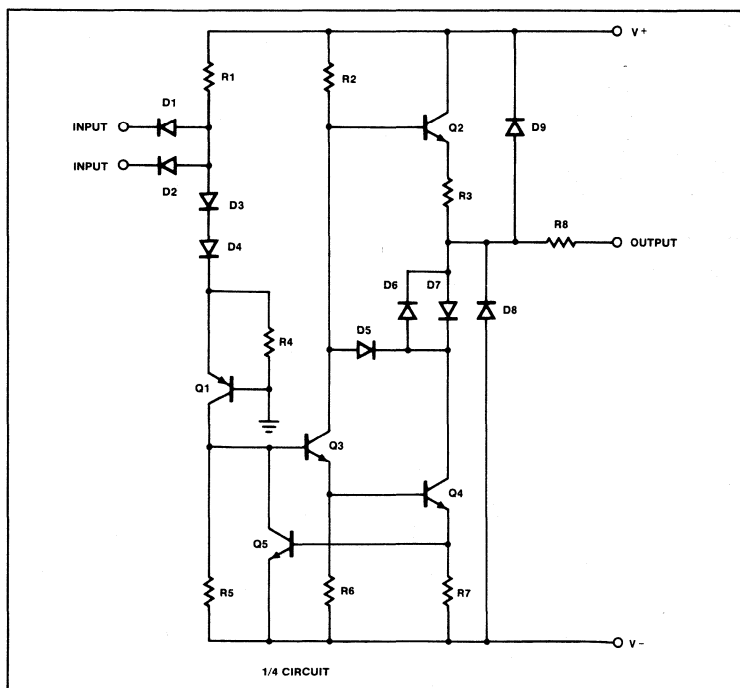
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage $V+$	+15	V
$V-$	-15	V
Input voltage (V_{IN})	$-15 \leq V_{IN} \leq 7.0$	V
Output voltage	± 15	V
Power dissipation:		
F package	1000	mW
N package	800	mW
Operating temperature range	0 to +75	$^{\circ}\text{C}$
Storage temperature range	-65 to +150	$^{\circ}\text{C}$
Lead temperature (soldering, 10sec)	300	$^{\circ}\text{C}$

CIRCUIT SCHEMATIC



QUAD LINE DRIVER

MC1488

DC ELECTRICAL CHARACTERISTICS $V_+ = +9.0V \pm 1\%$, $V_- = -9.0V \pm 1\%$, $T_A = 0^\circ C$ to $+75^\circ C$
 unless otherwise specified.
 All typicals are for $V_+ = 9.0V$, $V_- = -9.0V$, and $T_A = 25^\circ C$.*

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
		Min	Typ	Max		
Logic "0" input current	$V_{IN} = 0V$		-1.0	-1.6	mA	
Logic "1" input current	$V_{IN} = +5.0V$.005	10.0	μA	
High level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 0.8V$	$V_+ = 9.0V$ $V_- = -9.0V$	6.0	7.0	V	
		$V_+ = 13.2V$ $V_- = -13.2V$	9.0	10.5	V	
Low level output voltage	$R_L = 3.0k\Omega$ $V_{IN} = 1.9V$	$V_+ = 9.0V$ $V_- = -9.0V$	-6.0	-6.8	V	
		$V_+ = 13.2V$ $V_- = -13.2V$	-9.0	-10.5	V	
High level output Short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 0.8V$		-5.0	-10.0	-12.0	mA
Low level output Short-circuit current	$V_{OUT} = 0V$ $V_{IN} = 1.9V$		6.0	10.0	12.0	mA
Output resistance	$V_+ = V_- = 0V$ $V_{OUT} = \pm 2V$		300			Ω
Positive supply current (output open)	$V_{IN} = 1.9V$	$V_+ = 9.0V, V_- = -9.0V$ $V_+ = 12V, V_- = -12V$ $V_+ = 15V, V_- = -15V$		15.0 19.0 25.0	20.0 25.0 34.0	mA mA mA
	$V_{IN} = 0.8V$	$V_+ = 9.0V, V_- = -9.0V$ $V_+ = 12V, V_- = -12V$ $V_+ = 15V, V_- = -15V$		4.5 5.5 8.0	6.0 7.0 12.0	mA mA mA
Negative supply current (output open)	$V_{IN} = 1.9V$	$V_+ = 9.0V, V_- = -9.0V$ $V_+ = 12V, V_- = -12V$ $V_+ = 15V, V_- = -15V$		-13.0 -18.0 -25.0	-17.0 -23.0 -34.0	mA mA mA
	$V_{IN} = 0.8V$	$V_+ = 9.0V, V_- = -9.0V$ $V_+ = 12V, V_- = -12V$ $V_+ = 15V, V_- = -15V$		-1 -1 -0.1	-15 -15 -2.5	μA μA mA
Power dissipation	$V_+ = 9.0V, V_- = -9.0V$ $V_+ = 12V, V_- = -12V$		252 444	333 576	mW mW	
Propagation delay to "1" (t_{pd1})	$R_L = 3.0k\Omega, C_L = 15pF, T_A = 25^\circ C$		275	560	ns	
Propagation delay to "0" (t_{pd0})	$R_L = 3.0k\Omega, C_L = 15pF, T_A = 25^\circ C$		70	175	ns	
Rise time (t_r)	$R_L = 3.0k\Omega, C_L = 15pF, T_A = 25^\circ C$		75	100	ns	
Fall time (t_f)	$R_L = 3.0k\Omega, C_L = 15pF, T_A = 25^\circ C$		40	75	ns	

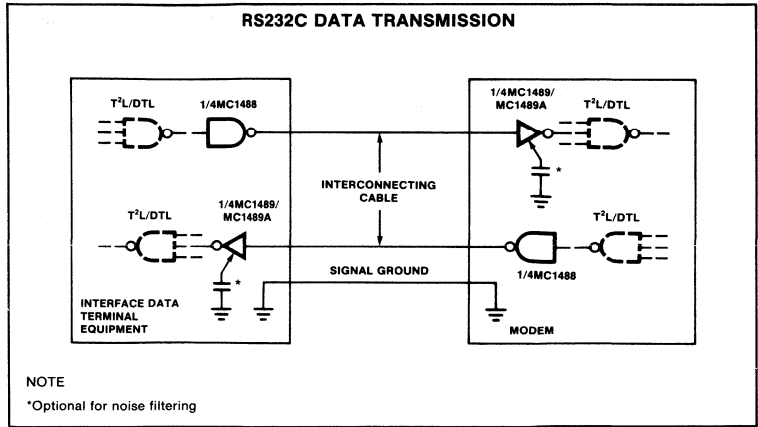
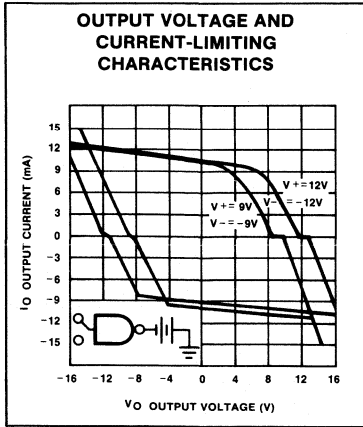
NOTE

*Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.

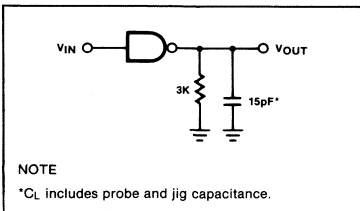
QUAD LINE DRIVER

MC1488

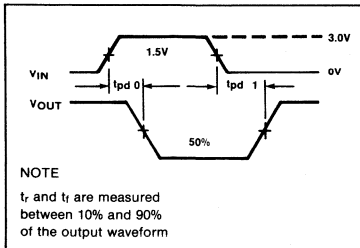
TYPICAL PERFORMANCE CHARACTERISTICS



AC LOAD CIRCUIT



SWITCHING WAVEFORMS



APPLICATIONS

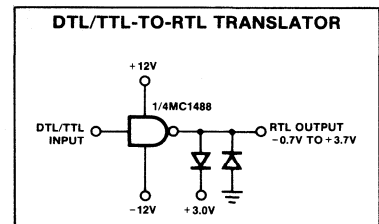
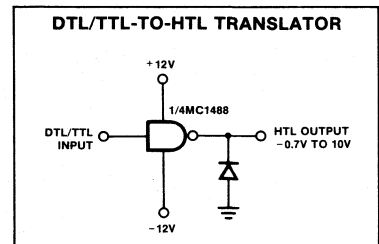
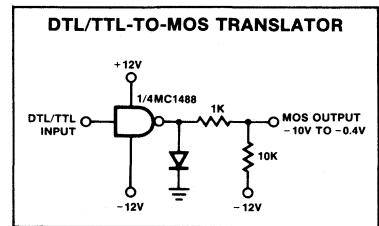
By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC} (\Delta T / \Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and ΔV/ΔT is the slew rate.

RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

TYPICAL APPLICATIONS



QUAD LINE RECEIVERS

MC1489/MC1489A

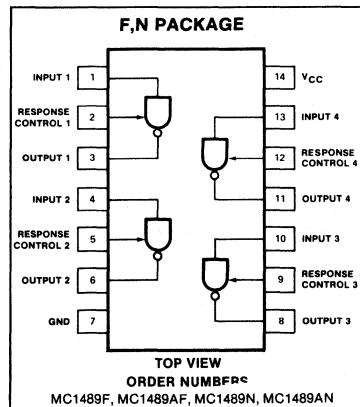
DESCRIPTION

The MC1489/MC1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS-232C.

FEATURES

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand $\pm 30V$

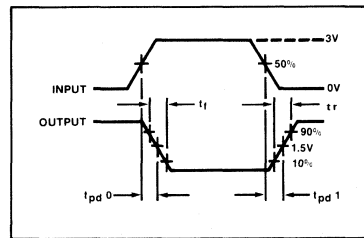
PIN CONFIGURATION



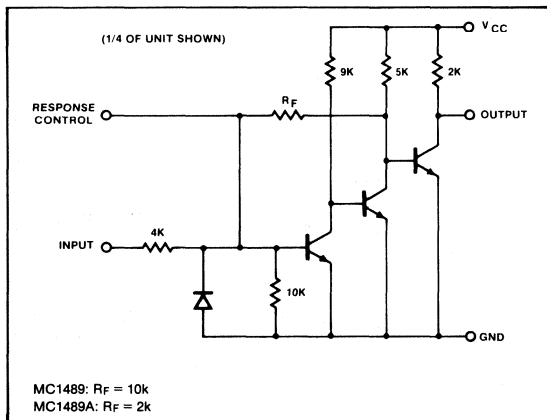
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Power supply voltage	10	V
Input voltage range	± 30	V
Output load current	20	mA
Power dissipation:		
F package	1	W
N package	800	mW
Operating temperature range	0 to +75	$^{\circ}C$
Storage temperature range	-65 to +150	$^{\circ}C$

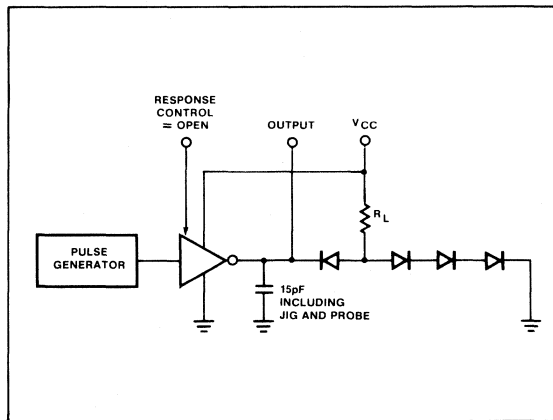
VOLTAGE WAVEFORMS



EQUIVALENT SCHEMATIC



AC TEST CIRCUIT



QUAD LINE RECEIVERS

MC1489/MC1489A

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 1\%$, $0^\circ C \leq T_A \leq +75^\circ C$ unless otherwise specified.^{1,2}

PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input high threshold voltage	$T_A = 25^\circ C$, $V_{OUT} \leq 0.45V$, $I_{OUT} = 10mA$	1.0		1.5	1.75		2.25	V
Input low threshold voltage	$T_A = 25^\circ C$, $V_{OUT} \leq 2.5V$, $I_{OUT} = -0.5mA$	0.75		1.25	0.75		1.25	V
	$V_{IN} = +25V$ $V_{IN} = -25V$	+3.6 -3.6	+5.6 -5.6	+8.3 -8.3	+3.6 -3.6	+5.6 -5.6	+8.3 -8.3	mA
Input current	$V_{IN} = +3V$ $V_{IN} = -3V$	+0.43 -0.43	+0.53 -0.53		+0.43 -0.43	+0.53 -0.53		mA
Output high voltage	$V_{IN} = 0.75V$, $I_{OUT} = -0.5mA$ Input = Open, $I_{OUT} = -0.5mA$	2.6	3.8	5.0	2.6	3.8	5.0	V
Output low voltage	$V_{IN} = 3.0V$, $I_{OUT} = 10mA$	2.6	3.8 0.33	5.0 0.45	2.6	3.8 0.33	5.0 0.45	V
Output short circuit current	$V_{IN} = 0.75V$		3.0			3.0		mA
Supply current	$V_{IN} = 5.0V$		20	26		20	26	mA
Power dissipation	$V_{IN} = 5.0V$		100	130		100	130	mW

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

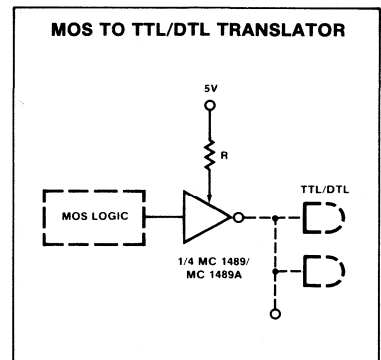
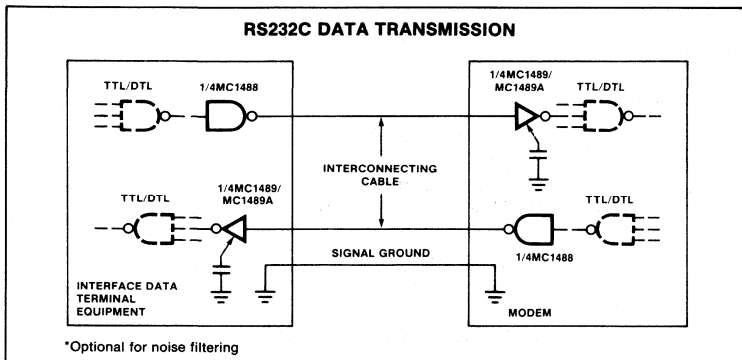
AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 1\%$, $T_A = 25^\circ C$ unless otherwise specified.^{1,2}

PARAMETER	TEST CONDITIONS	MC1489			MC1489A			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input to output "high" Propagation delay (t_{pd1})	$R_L = 3.9k\Omega$ (AC test circuit)		25	85		25	85	ns
Input to output "low" Propagation delay (t_{pd0})	$R_L = 390\Omega$ (AC test circuit)		20	50		20	50	ns
Output rise time	$R_L = 3.9k\Omega$ (AC test circuit)		110	175		110	175	ns
Output fall time	$R_L = 390\Omega$ (AC test circuit)		9	20		9	20	ns

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for response control pin = open.

TYPICAL APPLICATIONS



ADDRESSABLE PERIPHERAL DRIVERS

NE590/NE591

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has 8 Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a \overline{CE} input line which also serves the function of further address decoding. A common clear input, CLR, turns all outputs off when a logic low is applied.

The NE590 has 8 open collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin molded or cerdip package.

The NE591 has 8 open emitter Darlington outputs which source current to an external load from a common collector line, V_S . This V_S line need not necessarily be the same as the 5 volt V_{CC} supply. The device is packaged in an 18-pin molded or cerdip package.

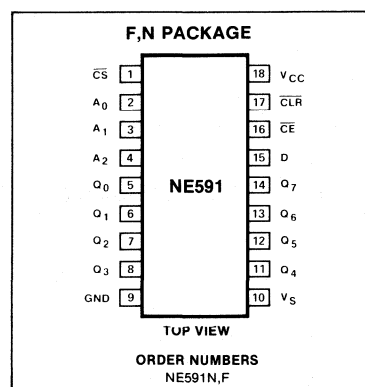
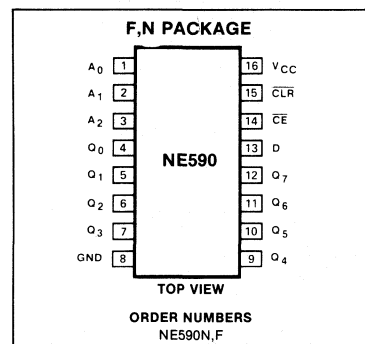
FEATURES

- 8 high current outputs
- Low-loading bus compatible inputs
- Power-on clear ensures safe operation
- NE590 will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- NE590 is pin compatible with 9334

APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver

PIN CONFIGURATION



PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1-3	2-4	A ₀ -A ₂	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	5-8, 11-14	Q ₀ -Q ₇	The 8 device outputs. The NE590 has open collector Darlington outputs. The NE591 has open emitter follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	16	\overline{CE}	Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output. The chip enable. When this input is low, the output latches will accept data. When \overline{CE} goes high, all outputs will retain their existing state, regardless of address or data input conditions.
15	17	\overline{CLR}	The clear input. When \overline{CLR} goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, \overline{CLR} low will override any other condition.
—	1	\overline{CS}	The chip select input provides for an additional level of address decoding.
—	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

ADDRESSABLE PERIPHERAL DRIVERS

NE590/NE591

TRUTH TABLE (NE590)

INPUTS							OUTPUTS							MODE	
CLR	CE	D	A ₀	A ₁	A ₂		Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	
L	H	X	X	X	X		H	H	H	H	H	H	H	H	Clear
L	L	L	L	L	L		H	H	H	H	H	H	H	H	Demultiplex
L	L	H	L	L	L		L	H	H	H	H	H	H		
L	L	L	H	L	L		H	H	H	H	H	H	H		
L	L	H	H	L	L		H	L	H	H	H	H	H		
L	L	L	H	H	H		H	H	H	H	H	H	H		
L	L	H	H	H	H		H	H	H	H	H	H	L		
L	L	H	H	H	H		H	H	H	H	H	H	L		
H	H	X	X	X	X		Q _{N-1} →							Memory	
H	L	L	L	L	L		H	Q _{N-1} →							Addressable Latch
H	L	H	L	L	L		L	Q _{N-1} →							
H	L	L	H	L	L		Q _{N-1}	H	Q _{N-1} →						
H	L	L	H	L	L		Q _{N-1}	L	Q _{N-1} →						
H	L	L	H	H	H		Q _{N-1} → H								
H	L	H	H	H	H		Q _{N-1} → L								
H	L	H	H	H	H		Q _{N-1} → L								

X = Don't care condition
 Q_{N-1} = Previous output state
 L = Low voltage level/"ON" output state
 H = High voltage level/"OFF" output state

(NE591)

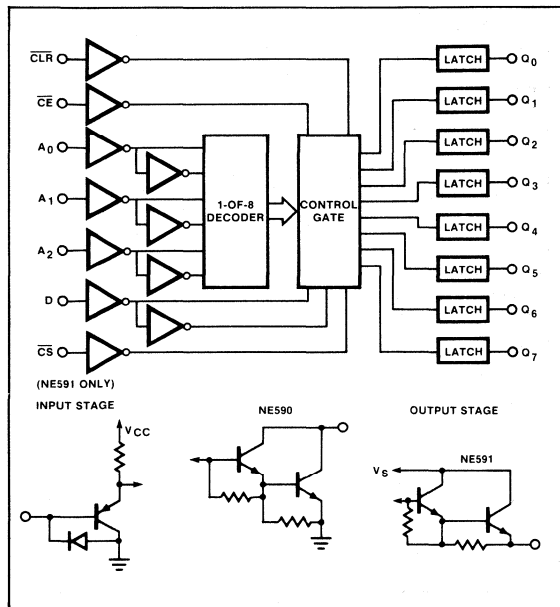
INPUTS								OUTPUTS							MODE	
CLR	CE	CS	D	A ₀	A ₁	A ₂		Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	
L	X	X	X	X	X	X		L	L	L	L	L	L	L	L	Clear
H	H	H	X	X	X	X		Q _{N-1} →							Memory	
H	H	L	X	X	X	X		Q _{N-1} →								
H	L	H	X	X	X	X		Q _{N-1} →								
H	L	L	L	L	L	L		L	Q _{N-1} →							Addressable Latch
H	L	L	H	L	L	L		H	Q _{N-1} →							
H	L	L	L	H	L	L		Q _{N-1}	L	Q _{N-1} →						
H	L	L	H	H	L	L		Q _{N-1}	H	Q _{N-1} →						
H	L	L	L	H	H	H		Q _{N-1} → L								
H	L	L	H	H	H	H		Q _{N-1} → H								
H	L	L	H	H	H	H		Q _{N-1} → H								

X = Don't care
 Q_{N-1} = Previous output state
 L = Low voltage level/"OFF" output state
 H = High voltage level/"ON" output state



ADDRESSABLE PERIPHERAL DRIVERS

NE590/NE591



ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise specified.

PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	-0.5 to +7 V
V _{IN}	Input voltage	-0.5 to +15 V
V _{OUT}	Output voltage	V
	NE590	0 to +7
	NE591	0 to V _{CC}
V _S	Source bus voltage	V
	NE591 only	-0.5 to +7
V _S -V _{CC}	Source/supply differential voltage	V
	NE591 only	-5 to +2
I _{OUT}	Output current	mA
	Each output	300
	All outputs	1000
P _D	Power dissipation ¹	1 W
	Temperature range	°C
T _A	Ambient	0 to +70
T _J	Junction	150
T _{STG}	Storage	-65 to +150
T _{SOld}	Lead soldering temperature (10sec max)	300 °C

DC ELECTRICAL CHARACTERISTICS V_{CC} = 4.75 to 5.25V, 0°C ≤ T_A ≤ 70°C unless otherwise specified.^{2,3}

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V _{IH} V _{IL}	Input voltage High Low	2.0		0.8	V
V _{OL} V _{OH}	Output voltage Low (NE590 only) High (NE591 only)		1.0	1.3 1.5	V
I _{IH} I _{IL}	Input current High Low CE input All other inputs		0.1	10	μA
I _{CC}	Supply current ⁴ All outputs low NE590 NE591 All outputs high NE590 NE591		33 15	50 50	mA
			15 30	50 50	

NOTES

- Derate power dissipation as indicated above threshold ambient temperature:
NE590N at 95°C/W above 55°C
NE590F at 100°C/W above 50°C
NE591N at 90°C/W above 60°C
NE591F at 93°C/W above 57°C
- All typical values are at V_{CC} = 5V and T_A = 25°C.
- For the NE591, V_S = V_{CC} in all tests.
- Supply current for the NE591 is measured with no output load.

ADDRESSABLE PERIPHERAL DRIVERS

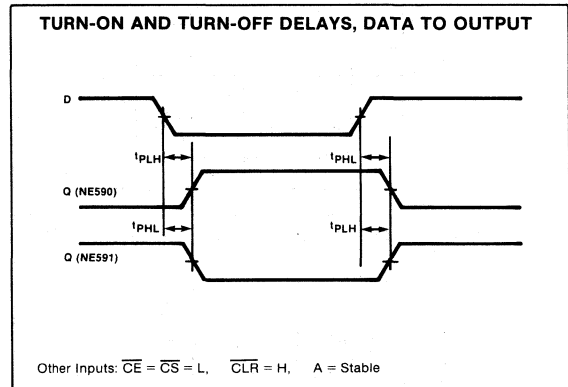
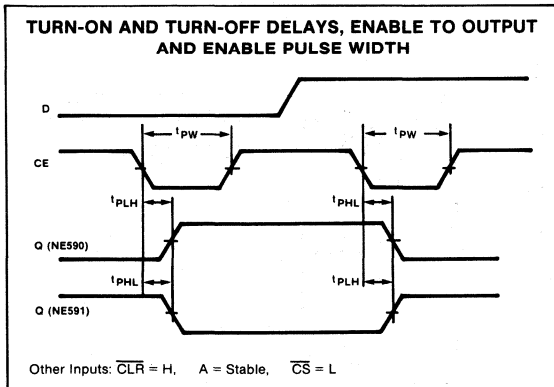
NE590/NE591

SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TO	FROM	NE590			NE591			UNIT
			Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL} Propagation delay time Low to high ⁵ High to low ⁵	Output	\overline{CE}		100 130			70 80		ns
t_{PLH} t_{PHL} Low to high ⁶ High to low ⁶	Output	Data		80 100			60 70		
t_{PLH} t_{PHL} Low to high ⁷ High to low ⁷	Output	Address		125 115			70 70		
t_{PLH} t_{PHL} Low to high ⁸ High to low ⁸	Output	\overline{CLR}		80			60		
t_{PLH} t_{PHL} Low to high ⁵ High to low ⁵	Output	\overline{CS}					70 80		
SWITCHING SET-UP REQUIREMENTS									
$t_s(H)$ ⁹	Chip enable	High data		120			50		ns
$t_s(L)$ ⁹	Chip enable	Low data		120			70		ns
$t_s(A)$ ¹⁰	Chip enable	Address		-60			-10		ns
$t_h(H)$ ⁹	Chip enable	High data		-60			-60		ns
$t_h(L)$ ⁹	Chip enable	Low data		-60			-20		ns
$t_s(CS)$ ⁹	Chip enable	Low chip select					70		ns
$t_{pw}(E)$	Chip enable pulse width ⁵			150			80		ns

NOTES

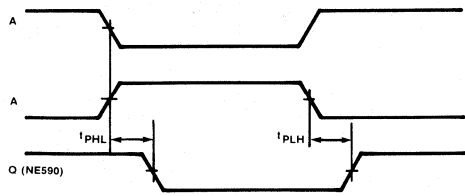
5. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
6. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
7. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
8. See Turn-Off Delay, Clear to Output timing diagram.
9. See Setup and Hold Time, Data to Enable timing diagram.
10. See Setup Time, Address to Enable timing diagram.



ADDRESSABLE PERIPHERAL DRIVERS

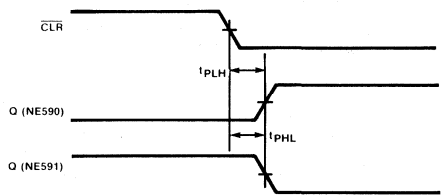
NE590/NE591

TURN-ON AND TURN-OFF DELAYS, ADDRESS TO OUTPUT



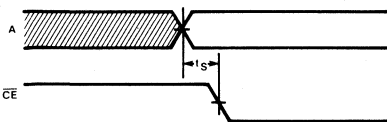
Other Inputs: $\overline{CE} = L$, $\overline{CLR} = L$, $D = H$

TURN-OFF DELAY, CLEAR TO OUTPUT



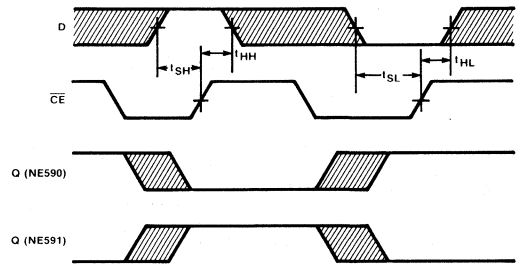
Other Inputs: $\overline{CE} = H$, $\overline{CS} = H$

SETUP TIME, ADDRESS TO ENABLE



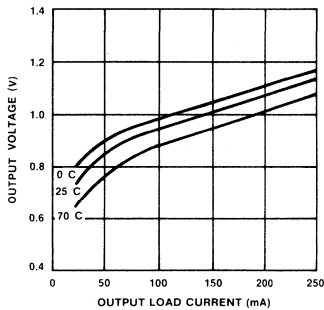
Other Inputs: $\overline{CLR} = H$, $\overline{CS} = L$

SETUP AND HOLD TIME, DATA TO ENABLE

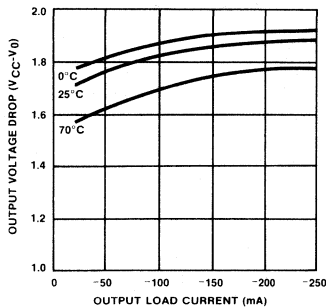


Other Inputs: $\overline{CLR} = H$, $A = \text{Stable}$, $\overline{CS} = L$

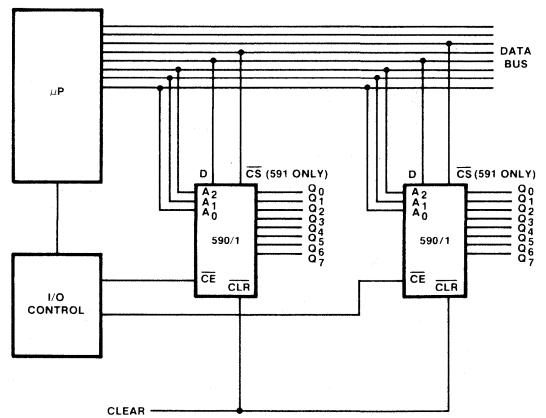
OUTPUT VOLTAGE VS LOAD CURRENT (NE590)



OUTPUT VOLTAGE DROP VS LOAD CURRENT (NE591)



INTERFACING THE 590/591 WITH A MICROPROCESSOR SYSTEM

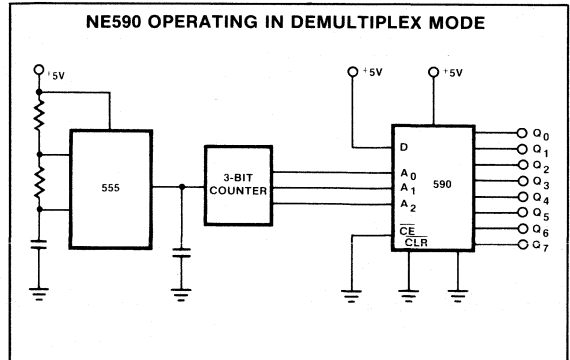
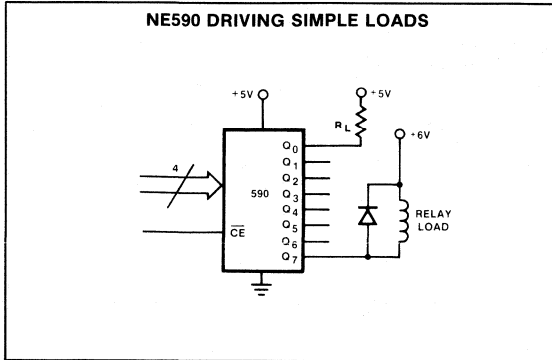


A₀, A₁, A₂, and \overline{CS} may be connected to the address bus if permitted by system design.

ADDRESSABLE PERIPHERAL DRIVERS

NE590/NE591

TYPICAL APPLICATIONS (Cont'd)



ADDRESSABLE RELAY DRIVER

NE/SE5090

Preliminary

DESCRIPTION

The NE/SE5090 addressable relay driver is a high current latched driver, similar in function to the 9934 address decoder. The device has 8 open collector Darlington power outputs, each capable of 150mA load current. The outputs are turned on or off by respectively loading a logic "1" or logic "0" into the device data input. The required output is defined by a 3 bit address. The device must be enabled by a CE input line which also serves the function of further address decoding. A common clear input, CLR, turns all outputs off when a logic "0" is applied. The device is packaged in a 16 pin plastic or CERDIP package.

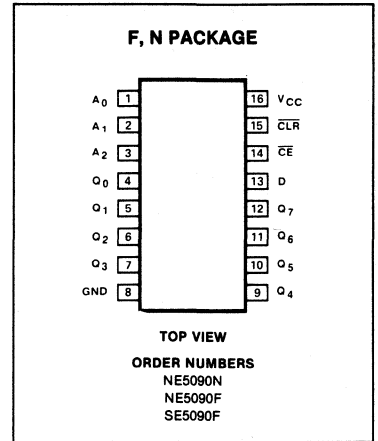
FEATURES

- 8 high current outputs
- Low-loading bus compatible inputs
- Power-on clear ensures safe operation
- Will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- Pin compatible with 9334

APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver

PIN CONFIGURATION



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1-3	A0-A2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	Q0-Q7	The 8 device outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF"
14	CE	The chip enable. When this input is low, the output latches will accept data. When CE goes high, all outputs will retain their existing state, regardless of address or data input conditions.
15	CLR	The clear input. When CLR goes low all output switches are turned "OFF". The high data input will override the clear function on the addressed latch.

TRUTH TABLE - 55 ≤ T_A ≤ + 125 °C, V_{CC} = 4.5V

INPUTS						OUTPUTS								MODE		
CLR	CE	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇			
L	H	X	X	X	X	H	H	H	H	H	H	H	H	Clear		
L	L	L	L	L	L	H	H	H	H	H	H	H	H	Demultiplex		
L	L	L	H	L	L	L	H	H	H	H	H	H	H			
L	L	L	L	H	L	L	H	L	H	H	H	H	H			
L	L	L	H	H	L	L	H	H	H	H	H	H	H			
L	L	L	H	H	H	L	H	H	H	H	H	H	L			
H	H	X	X	X	X	Q _{N-1} →								Memory		
H	L	L	L	L	L	H	Q _{N-1} →								Addressable Latch	
H	L	H	L	L	L	L	Q _{N-1} →									
H	L	L	H	L	L	Q _{N-1}	H	Q _{N-1} →								
H	L	H	H	L	L	Q _{N-1}	L	Q _{N-1} →								
H	L	L	H	H	H	Q _{N-1}	→ H									
H	L	H	H	H	H	Q _{N-1}	→ L									

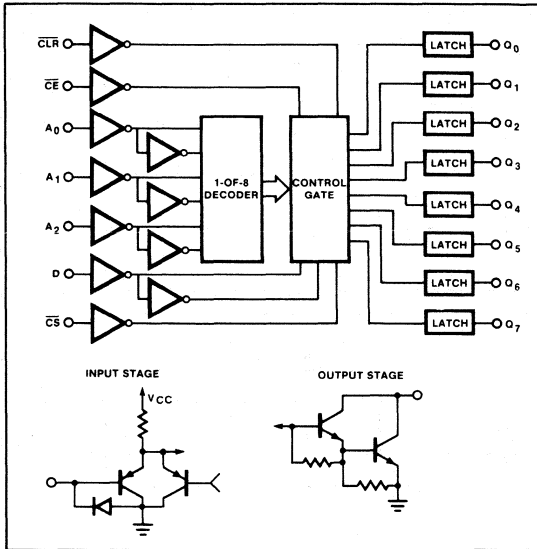
X = Don't care condition
 Q_{N-1} = Previous output state
 L = Low voltage level/"ON" output state
 H = High voltage level/"OFF" output state

ADDRESSABLE RELAY DRIVER

NE/SE5090

Preliminary

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	- 0.5 to + 7 V
V_{IN}	Input voltage	- 0.5 to + 15 V
V_{OUT}	Output voltage	0 to + 30 V
I_{GND}	Ground current	500 mA
I_{OUT}	Output current	200 mA
	Each output	
P_D	Power dissipation ¹	1 W
	Ambient temperature range	
T_A	SE5090	- 55 to + 125 $^\circ\text{C}$
T_A	NE5090	0 to + 70 $^\circ\text{C}$
T_J	Junction	150 $^\circ\text{C}$
T_{STG}	Storage	- 65 to + 150 $^\circ\text{C}$
T_{sold}	Lead soldering temperature (10 sec max)	300 $^\circ\text{C}$

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 4.5\text{V to } 5.5\text{V}$, $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ unless otherwise specified (SE5090)².
 $V_{CC} = 4.75\text{V to } 5.25\text{V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ unless otherwise specified (NE5090)².

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IH} V_{IL}	Input voltage High Low	2.0		0.8	V
V_{OL}	Output voltage Low $I_{OL} = 150\text{mA}$, $T_A = 25^\circ\text{C}$ Over temperature		1.05	1.30 1.50	V
I_{IH} I_{IL}	Input current High Low $V_{IN} = V_{CC}$ $V_{IN} = 0\text{V}$		< 1.0 - 3.0	10	μA
I_{OH}	Leakage current $V_{OUT} = 28\text{V}$,		5	250	μA
I_{CCL} I_{CCH}	Supply current All outputs low All outputs high $V_{CC} = 5.5\text{V}$ SE5090 $= 5.25\text{V}$ NE5090		35 22	60 50	mA

NOTES

- Derate power dissipation as indicated above threshold ambient temperature NE/SE5090 N at 95°C/W above 55°C NE/SE5090 F at 100°C/W above 50°C
- All typical values are at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$



ADDRESSABLE RELAY DRIVER

NE/SE5090

Preliminary

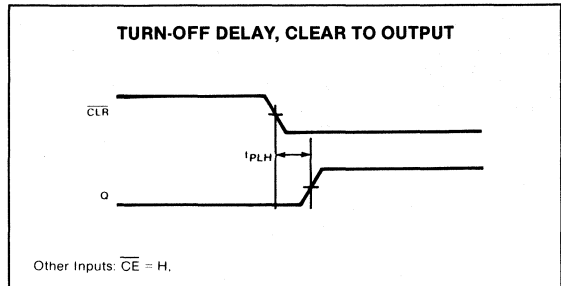
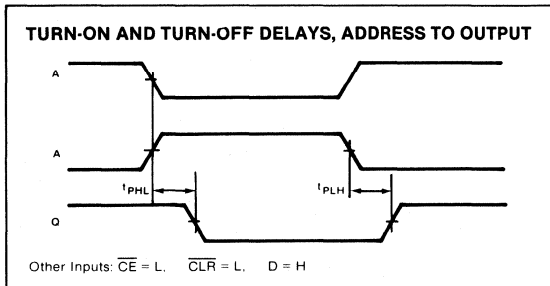
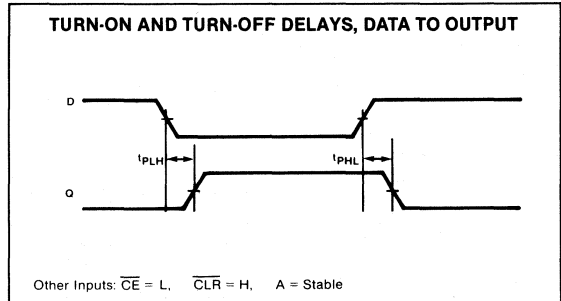
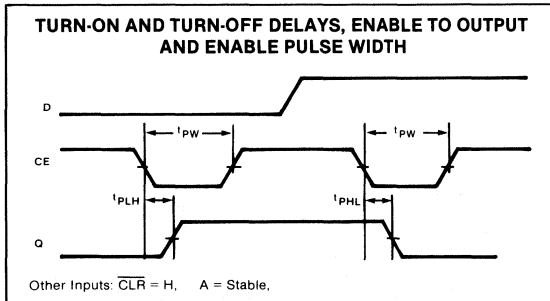
SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C, V_{OUT} = 5V, I_{OUT} = 100mA, V_{IL} = 0.8V, V_{IH} = 2.0V$

PARAMETER		TO	FROM	Min	Typ	Max	UNIT
t_{PLH} t_{PHL}	Propagation delay time Low to high ¹ High to low ¹	Output	\overline{CE}		900 130		ns
t_{PLH} t_{PHL}	Low to high ² High to low ²	Output	Data		920 130		ns
t_{PLH} t_{PHL}	Low to high ³ High to low ³	Output	Address		900 130		ns
t_{PLH} t_{PHL}	Low to high ⁴ High to low ⁴	Output	\overline{CLR}		920		ns
SWITCHING SETUP REQUIREMENTS							
$t_{s(H)}^5$ $t_{s(L)}^5$		Chip enable	High data		40		ns
		Chip enable	Low data		40		ns
$t_{s(A)}^6$		Chip enable	Address		20		ns
$t_{h(H)}^5$ $t_{h(L)}^5$		Chip enable	High data		0		ns
		Chip enable	Low data		0		ns
$t_{pw(E)}^1$	Chip enable pulse width ¹				20		ns

NOTES

1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.
2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.
3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.
4. See Turn-Off Delay, Clear to Output timing diagram.
5. See Setup and Hold Time, Data to Enable timing diagram.
6. See Setup Time, Address to Enable timing diagram.

TIMING DIAGRAMS



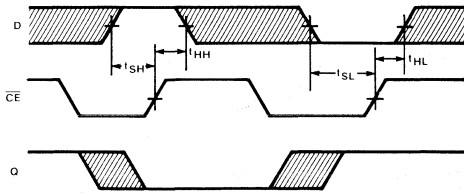
ADDRESSABLE RELAY DRIVER

NE/SE5090

Preliminary

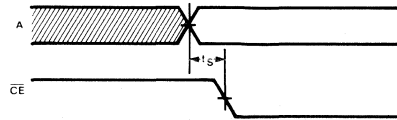
TIMING DIAGRAMS (Cont'd)

SETUP AND HOLD TIME, DATA TO ENABLE



Other Inputs: $\overline{\text{CLR}} = \text{H}$, A = Stable.

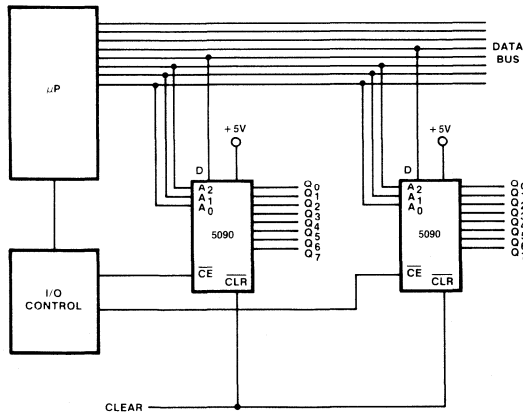
SETUP TIME, ADDRESS TO ENABLE



Other Inputs: $\overline{\text{CLR}} = \text{H}$.

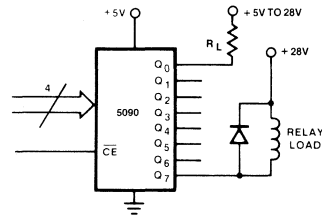
TYPICAL APPLICATIONS

INTERFACING WITH A MICROPROCESSOR SYSTEM

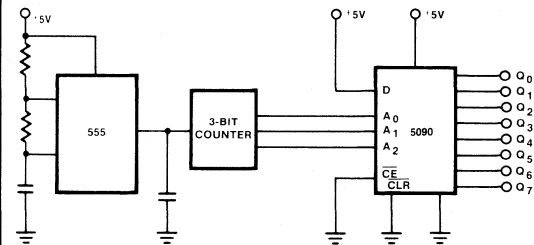


A₀, A₁, A₂ may be connected to the address bus if permitted by system design.

DRIVING SIMPLE LOADS



OPERATING IN DEMULTIPLEX MODE



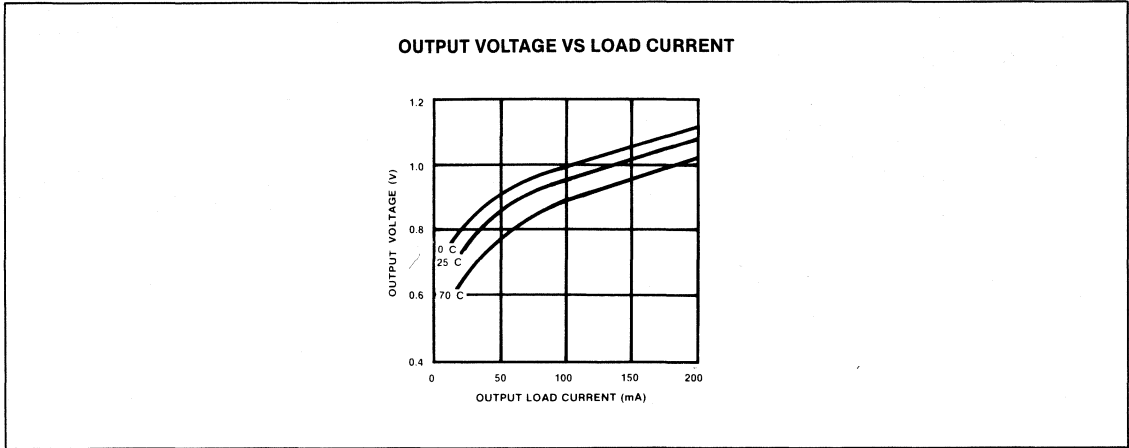
9

ADDRESSABLE RELAY DRIVER

NE/SE5090

Preliminary

TYPICAL PERFORMANCE CHARACTERISTICS



Section 10 Display Drivers

INDEX

Section 10 — Display Drivers

Index	10-1
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NE582-1 Hex Universal Driver	10-5
NE587 LED Decoder/Driver	10-8
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NE/SA594 Vacuum Flourescent Display Driver	10-24

DISPLAY DRIVER—SYMBOLS AND DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

T_{STG}

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

T_{SOLD}

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low

1 is logic level high

X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} (-V_{CC})

Supply Voltage. The range of power supply voltage over which the device will operate safely.

LED

Light Emitting Diode

 \overline{X}

Negate Bar—when it appears over a function indicates that the "true" or valid condition of that function is a logic low level.

i.e. LE - would require a logic high level to cause a latch enable.

\overline{LE} - would require a logic low level to cause a latch enable.

I_{SEG}

Segment Current. The amount of current supplied to each segment in a display. Current ratios are generally compared to segment 'b'.

BCD

Binary Coded Decimal

 \overline{BI} /RBO

Blanking Input or Ripple Blanking Output.

RBI

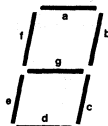
Ripple Blanking Input. The maximum clock frequency: the maximum input frequency at a clock input for the predictable performance. Above this frequency the device may cease to function.

t_{PLH}

Propagation Delay Time. The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL}

Propagation Delay Times. The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.

Segment Identification**t_h**

Hold Time. The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the current logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s

Setup Time. The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_w

Pulse Width. The time between the specified reference points on the leading and trailing edges of a pulse.

t_{rec}

Recovery Time. The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

V_S

Source Voltage. A separate V_{CC} line depending on part type.

I_{OH}

Output Current Source the device can supply while maintaining a specified voltage output level.

Typical Value

The typical value of a particular parameter determined by characterization of the device or sampling. Usually indicates that the particular device is not 100% tested for the parameter because it does not vary or can be determined by design and other tested variables. Occasionally typical values are given rather than min-

10

DISPLAY DRIVER—SYMBOLS AND DEFINITIONS

DISPLAY DRIVER DEFINITIONS (Cont'd)

max values because 100% testing would raise the cost of the product to a prohibitive level. If a typical value must be guaranteed to ensure specific operation, custom testing can often be provided at an additional cost to the user.

I_S

Source Current. Current flowing into the V_S supply terminal of the device with specified operating conditions.

Duty Cycle

Ratio of time on to time off. Generally expressed in percentage.

V_F

Forward voltage drop of a device at a specified current level.

I_B

Input Bias Current Current into an analog circuit input, specified at a particular voltage level.

CLR

Clear. Clear command will preset all internal circuits to a predetermined state.

CE

Chip Enable.

V_{IH}

Input High Voltage. The range of input voltages recognized by the device as a logic high.

V_{IL}

Input Low Voltage. The range of input voltages recognized by the device as a logic low.

V_{OH}

Output High Voltage. The minimum guaranteed High voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.

V_{OL}

Output Low Voltage. The maximum guaranteed low voltage at an output terminal sinking the specified load current I_{OL} .

V_{BR}

Output Breakdown Voltage. Maximum voltage applied to a disabled (off) output to ensure a leakage current less than the specified value.

V_{IN}

The range of voltage on any input which the device can safely handle or a specified input voltage to the device.

V_{OUT}

The range of voltage on any output which the device can safely handle or a specified output voltage to the device.

I_{CC}(-I_{CC})

Supply Current. The current flowing into the $+V_{CC}$ ($-V_{CC}$) supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.

I_{IH}

Input High Current. The Current flowing into or out of an input when a specified High level voltage is applied to that input.

I_{IL}

Input Low Current. The current flowing out of an input when a specified Low level voltage is applied to that input.

I_{OL}

Output Low Current. The current flowing into an output when a which is in the Low State.

I_{OS}

Output Short-Circuit Current. The current flowing out of an output which is in the High state when that output is short circuit to the ground.

I_{CEx}

Output Leakage Current. The current flowing out of or into a disabled (off) output with a specified High output voltage applied.

HEX UNIVERSAL DRIVER

NE582-1

Preliminary

DESCRIPTION

The NE582-1 is a general interface device comprising a high current output transistor and drive circuitry in each of 6 elements. Each output transistor is individually capable of sinking 400mA with a typical saturation voltage of 0.5V. Input loading is such that direct interfacing with P-MOS, N-MOS, C-MOS or TTL is possible.

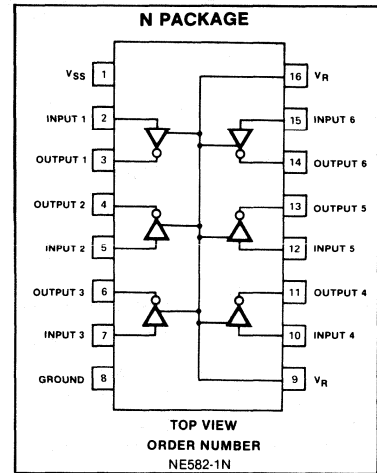
The NE582-1 has applications as a LED display driver, low voltage relay/lamp drivers and many others where high current capability without speed constraints is required.

The NE582-1 is supplied in a 16-pin high dissipation dual-in-line plastic package.

FEATURES

- Low saturation voltage (typically 0.5V) for minimum power dissipation
- High output sink current capability—400mA
- Low input current loading for MOS compatibility
- Low standby power consumption
- Suitable for 3 volt battery operation
- Inputs/outputs are compatible with 75494

PIN CONFIGURATION



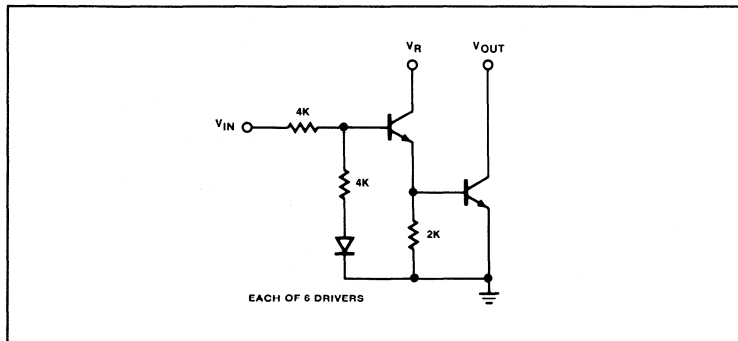
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Input voltage range ¹	-12 to V _{SS}	V
Output voltage ²	15	V
Output to input voltage differential	10	V
Voltage at V _{SS} (pin 1)	10	V
Output current—each output	400	mA
Output current—all outputs	800	mA
Continuous total power dissipation at or below 25°C ³	800	mW
Current in V _R (pin 9 or 16)	25	mA
Operating free-air temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature 1/16 inch from case for 10sec	260	°C

NOTES

1. The inputs are the only pins which may be negative with respect to ground.
2. Voltage values are with respect to ground.
3. Above 25°C, derate power dissipation at 6.25mW/°C.

EQUIVALENT SCHEMATIC



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HEX UNIVERSAL DRIVER

NE582-1

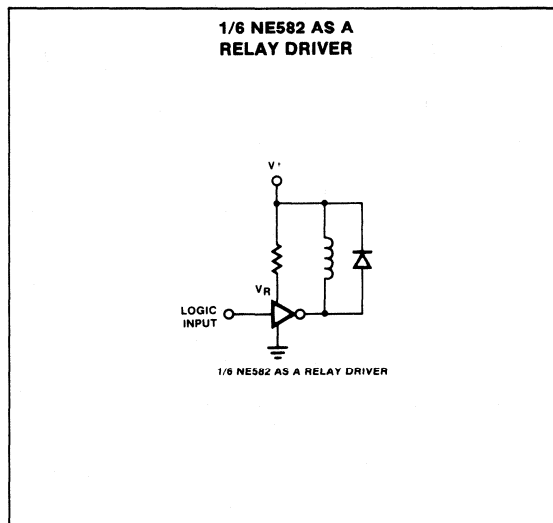
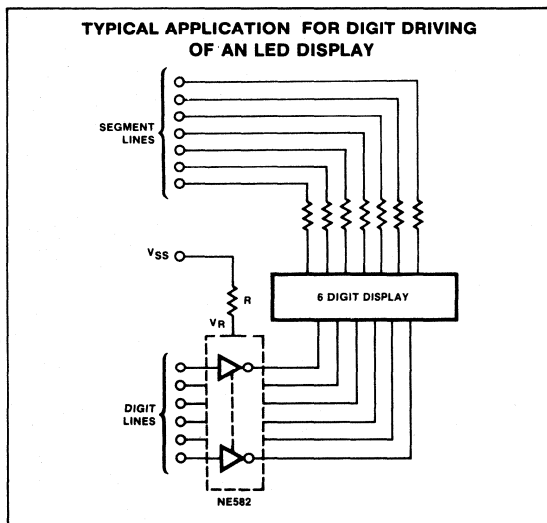
Preliminary

ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to 70°C unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{OL} Low level output voltage	$V_{IN} \ I_R \ I_{OL}$ V mA mA 3.2 6.0 150 $R_{IN} = 1K$ (Series input resistance)		.500	.750	V
I_{OH} High level output current	$V_{OH} = 15V, V_{IN} = 0.1V$			50	μA
I_{IN} Input current at maximum input voltage	$V_{IN} = 10V, I_{OL} = 20mA, I_R = 2mA$		2.2	3.3	mA
V_R I_{SS} Current into pin 1	$V_{IN} = 6.5V, I_R = 6mA, I_{OL} = 80mA$ $V_{SS} = 10V$.9	1.5	V μA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
T_{PLH} Switching characteristics Propagation delay, low to high level input	$R_R = 680\Omega$ $R_L = 39\Omega$ $C_L = 15pF$		600		ns
T_{PHL} Propagation delay, high to low level input	$V_{IH} = 7.5V$ $V_{IL} = 0V$ $t_r = t_f \leq 10ns$ $t_w = 1\mu s$ PRR = 100kHz		50		ns



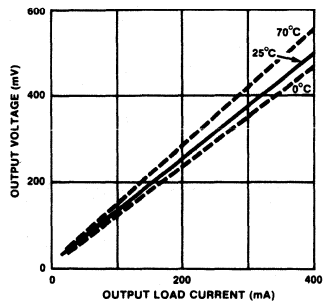
HEX UNIVERSAL DRIVER

NE582-1

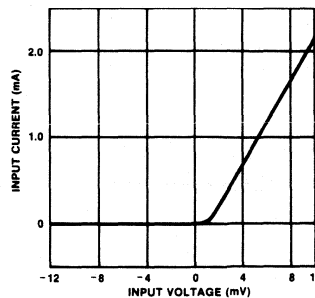
Preliminary

PRELIMINARY SPECIFICATION

OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT LOAD CURRENT,
 $I_R = 25\text{mA}$
 $V_{IN} = 6.5\text{ VOLTS}$



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE,
 $I_R = 25\text{mA}$, $V_{SS} = 10\text{V}$, $T_A = 25^\circ\text{C}$



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LED DECODER/DRIVER

NE587

DESCRIPTION

The NE587 is a latch/decoder/driver for 7-segment common anode LED displays. The NE587 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and \overline{LE} (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

FEATURES

- Latched BCD inputs
- Low loading bus-compatible inputs
- Ripple-blanking on leading and/or trailing edge zeros

APPLICATIONS

- Digital panel meters
- Measuring instruments
- Test equipment
- Digital clocks
- Digital bus monitoring

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7	V
V_{IN}	Input voltage ($D_0 - D_3, \overline{LE}, \overline{RBI}$)	-0.5 to +15	V
V_{OUT}	Output voltage (a-g, RBO)	-0.5 to +7	V
P_D	Power dissipation (25°C) ¹	1000	mW
T_A	Ambient temperature range	0 to 70	$^\circ\text{C}$
T_J	Junction temperature	150	$^\circ\text{C}$
T_{STG}	Storage temperature range	-65 to +150	$^\circ\text{C}$
T_{SOLD}	Soldering temperature (10 sec. max)	300	$^\circ\text{C}$

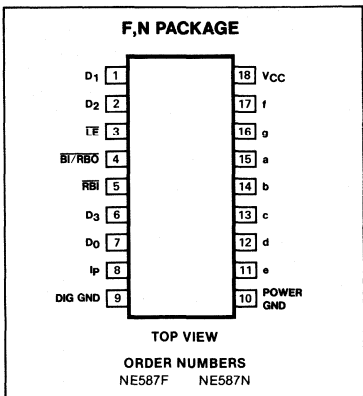
NOTE

Derate power dissipation as indicated

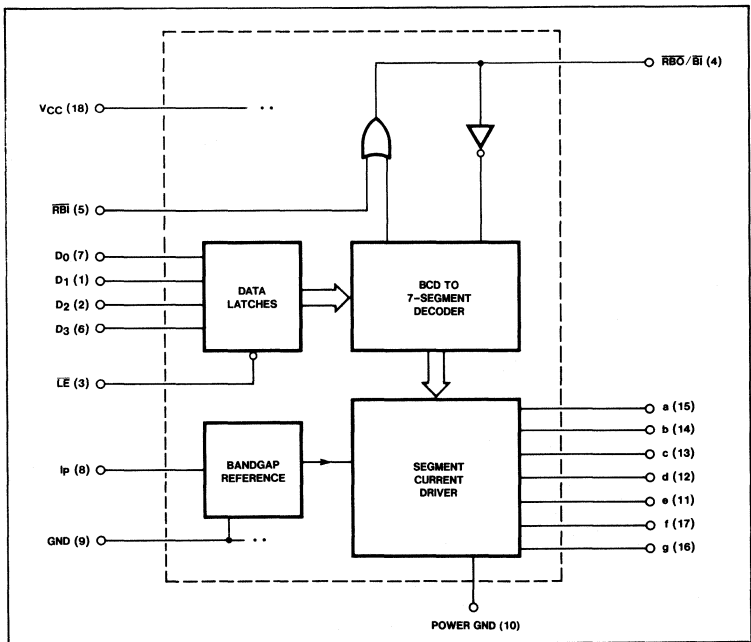
N package - 95°C/watt above 55°C

F package - 100°C/watt above 50°C

PIN CONFIGURATIONS



BLOCK DIAGRAM



LED DECODER/DRIVER

NE587

DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 4.75$ to $5.25V$, $0^{\circ}C < T_A < 70^{\circ}C$.Typical values are at $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $R_P = 1k\Omega (\pm 1\%)$ unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE587			UNIT
		Min	Typ	Max	
V_{CC} Operating supply voltage		4.75	5.00	5.25	V
V_{IH} Input high voltage	All Inputs except \overline{BI} \overline{BI}	2.0 2.0		15 5.5	V
V_{IL} Input low voltage				0.8	V
V_{IC} Input clamp voltage	$I_{IN} = -12mA$, $T_A = 25^{\circ}C$			-1.5	V
I_{IH} Input high current	Inputs $D_0 - D_3$, \overline{LE} , \overline{RBI} $V_{IN} = 2.4V$ $V_{IN} = 15V$ Input \overline{BI} (pin 4) $\overline{RBI} = H$ $V_{IN} = V_{CC} = 5.25V$		1.0 15 10	10 15 100	μA μA
	$V_{IN} = 0.4V$, Inputs $D_0 - D_3$ \overline{LE} , \overline{RBI} Input \overline{BI} $V_{CC} = 5.25V$ $\overline{RBI} = H$, $V_{IN} = 0.4V$			-5 -200 -0.7	μA mA
V_{OL} Output low voltage	Output \overline{RBO} $I_{out} = 3.0mA$.2	.5	V
V_{OH} Output high voltage	Output \overline{RBO} $I_{OUT} = -50\mu A$ $\overline{RBI} = H$	3.5	4.5		V
I_{OUT} Output segment "ON" current	Outputs "a" thru "g" $V_{OUT} = 2.0V$	20	25	30	mA
ΔI_{OUT} Output current ratio (all outputs ON)	With reference to "b" segment $V_{OUT} = 2.0V$	0.90	1.00	1.10	
I_{OFF} Output segment "OFF" current	Outputs "a" thru "g" $V_{OUT} = 5.0V$		20	250	μA
I_{CCO} Supply current	$V_{CC} = 5.25V$ All outputs "ON" $V_{OUT} > 1V$		33	55	mA
I_{CCI} Supply current	$V_{CC} = 5.25V$ All outputs blanked		50	70	mA

NOTE

NE587 PROGRAMMING

The NE587 output current can be programmed, provided a program resistor, R_P , be connected between I_P (pin 8) and Ground (pin 9). The voltage at I_P (pin 8) is constant ($\approx 1.3V$). Thus, a current through R_P is $I_P \approx \frac{1.3V}{R_P}$, as shown in Figure 5. I_P is 20 in the 15 to 50mA output current range.

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LED DECODER/DRIVER

NE587

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$ $T_A = 25^\circ C$. $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

PARAMETER	TEST CONDITIONS	NE587			UNIT
		Min	Typ	Max	
$t_{D_{av}}$ Propagation delay Figure 2	From data to output		135		ns
$t'_{D_{av}}$ Propagation delay Figure 3	From \overline{LE} to output		135		ns
t_W Latch enable pulse width Figure 4		30			ns
t_S Latch enable setup time Figure 4	From data to \overline{LE}	20			ns
t_H Latch enable hold time Figure 4	From \overline{LE} to data	0			ns

NOTE

$t'_{D_{av}} = \frac{1}{2} (t_{HL} + t_{LH})$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY	
	\overline{LE}	\overline{RBI}	D ₃	D ₂	D ₁	D ₀	a	b	c	d	e	f	g	\overline{RBO}		
—	H	*	X	X	X	X	STABLE								**	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK	
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0	
1	L	X	L	L	L	H	H	L	L	H	L	H	L	H	1	
2	L	X	L	L	H	H	L	L	L	L	L	H	L	H	2	
3	L	X	L	L	H	H	L	L	L	L	L	H	L	H	3	
4	L	X	L	H	L	L	H	L	L	H	H	L	L	H	4	
5	L	X	L	H	L	H	L	H	L	L	L	L	L	H	5	
6	L	X	L	H	H	L	L	L	L	L	L	L	L	H	6	
7	L	X	H	H	H	H	L	L	L	H	H	H	H	H	7	
8	L	X	H	L	L	L	L	L	L	L	L	L	L	H	8	
9	L	X	H	L	L	H	L	L	L	L	H	L	L	H	9	
10	L	X	H	L	H	L	H	H	H	H	H	H	L	H	-	
11	L	X	H	L	H	H	L	H	H	L	L	L	L	H	E	
12	L	X	H	H	L	L	H	L	L	H	L	L	L	H	H	
13	L	X	H	H	L	H	H	H	H	L	L	L	H	H	L	
14	L	X	H	H	H	L	L	L	H	H	L	L	L	H	P	
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	blank	
BI	X	X	X	X	X	X	H	H	H	H	H	H	H	L	blank	

NOTES

H = HIGH voltage level, output is "OFF"

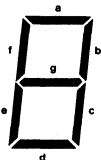
L = LOW voltage level, output is "ON"

X = Don't care

* The \overline{RBI} will blank the display only if a binary zero is stored in the latches.

** \overline{RBO}/BI used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



LED DECODER/DRIVER

NE587

NE587 PROGRAMMING

NE587 output current can be programmed by using a programming resistor, R_p , connected between r_p (pin 8) and Gnd (pin 9). The voltage at r_p (pin 8) is constant ($\approx 1.40V$). A partial schematic of the voltage reference used in the NE587 is shown in figure 1.

Output current to program current ratio, I_O/I_P , is 20 in the 15mA to 50mA range. Note that I_P must be derived from a resistor (R_p), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

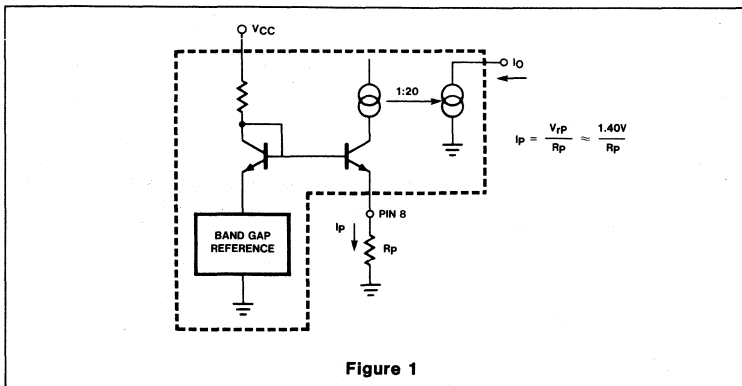


Figure 1

TIMING DIAGRAMS

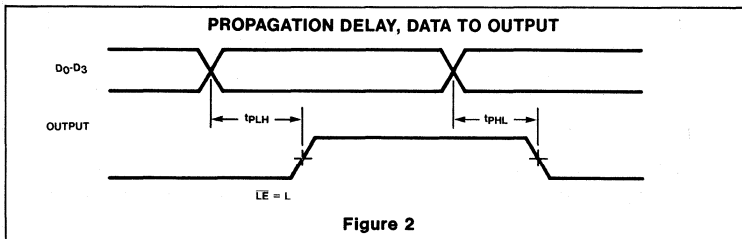


Figure 2

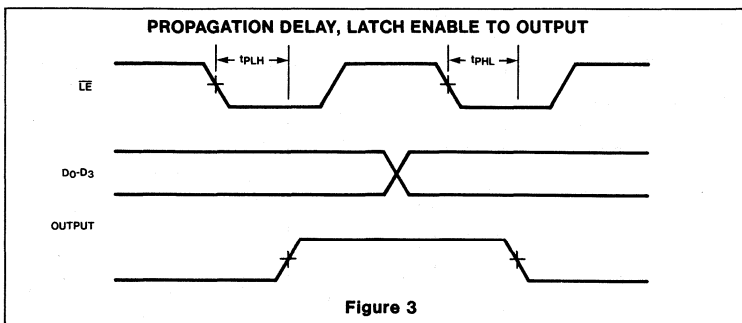


Figure 3

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to figure 6, the two system power supplies are V_{CC} and V_S . In many cases, these will be the same voltage. Necessary parameters are:

- V_{CC} , Supply voltage to driver
- V_S , Supply voltage to display
- I_{CC} , Quiescent supply current of driver
- I_{SEG} , LED segment current
- V_F , LED segment forward voltage at I_{seg}
- K_{DC} , % Duty cycle

V_F , the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

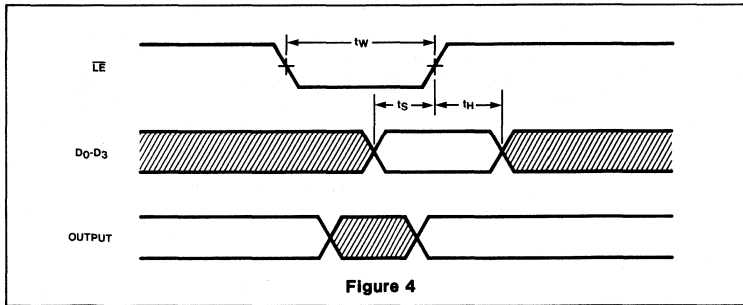
Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

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LED DECODER/DRIVER

NE587

TIMING DIAGRAMS (Cont'd)



These voltages are all for single diode displays. Some early red displays had 2 series LEDs per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

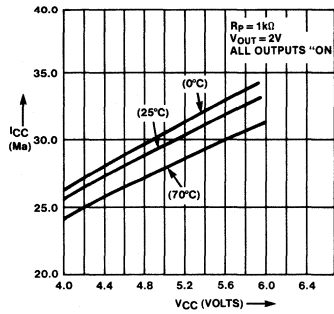
$$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{seg} \times K_{DC} \text{ mW}$$

Assuming $V_S = V_{CC} = 5.25V$
 $V_F = 2.0V$

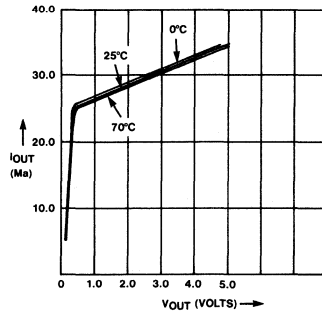
$$P_{d \text{ max}} = 5.25 \times 50 + 3.25 \times 7 \times 30 \text{ mW} = 945 \text{ mW}$$

TYPICAL PERFORMANCE CURVES

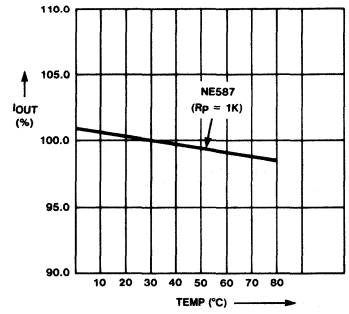
SUPPLY CURRENT VS SUPPLY VOLTAGE
NE587



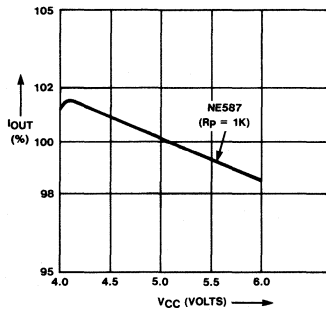
OUTPUT CURRENT VS OUTPUT VOLTAGE
NE587
Rp = 1Kohms



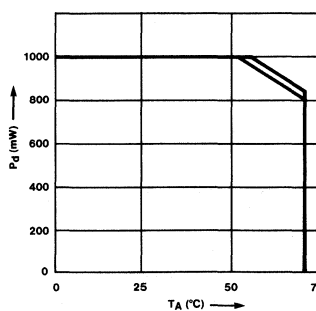
NORMALIZED OUTPUT CURRENT VS TEMPERATURE
VCC = 5.0V



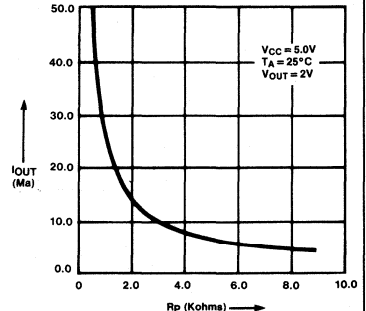
NORMALIZED OUTPUT CURRENT VS SUPPLY VOLTAGE
V_O = 2V
T_A = 25°C



MAXIMUM POWER DISSIPATION VS TEMPERATURE



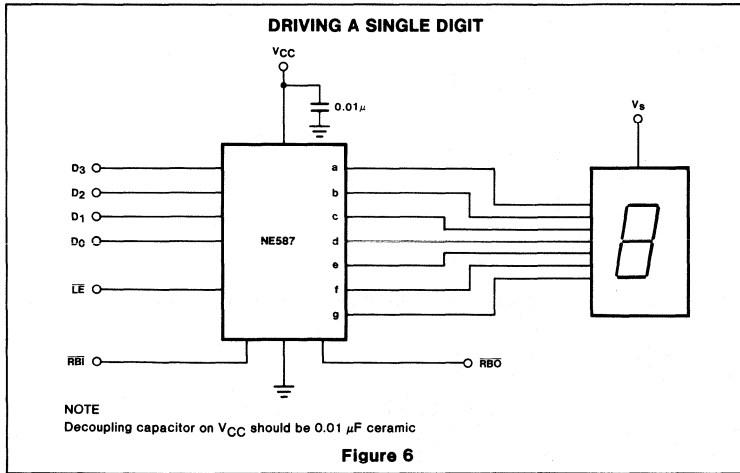
OUTPUT CURRENT VS PROGRAM RESISTOR



LED DECODER/DRIVER

NE587

TYPICAL APPLICATIONS



However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{d\ av} = 5.0 \times 30 + 3.00 \times 5 \times 25\ \text{mW} = 525\ \text{mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph. (See Typical Performance Characteristics).

However, a major portion of this power dissipation ($P_{d\ max}$) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor

from V_{CC} to V_S . The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{seg}} \approx 10\Omega \ (\frac{1}{2}\ \text{W rating})$$

assuming worst case I_{seg} of 30 mA

$$\begin{aligned} \text{Hence now } P_{d\ max} &= V_{CC} \times I_{CC} + (V_S - V_V - R_X \times 7 \times I_{seg}) \times 7 \times I_{seg} \\ &\quad \times K_{DC} \\ &= 5.25 \times 50 + 1.25 \times 7 \times 30 \\ &\quad \text{mW} \\ &= 525\ \text{mW} \end{aligned}$$

$$\text{and } P_{d\ av} = 5.0 \times 30 + 1.25 \times 5 \times 25 = 306\ \text{mW}$$

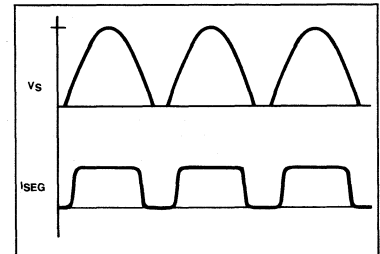
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_D, \quad V_D \approx 0.8\text{V}$$

Where n is the number of diodes used, power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 9. For example a darlington PNP or NPN emitter follower may be preferable. Figure 8 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S , V_F and the output characteristics of the display driver.

With
 $V_S = 4.9\text{V pk.}$
 $V_F = 2.0\text{V}$

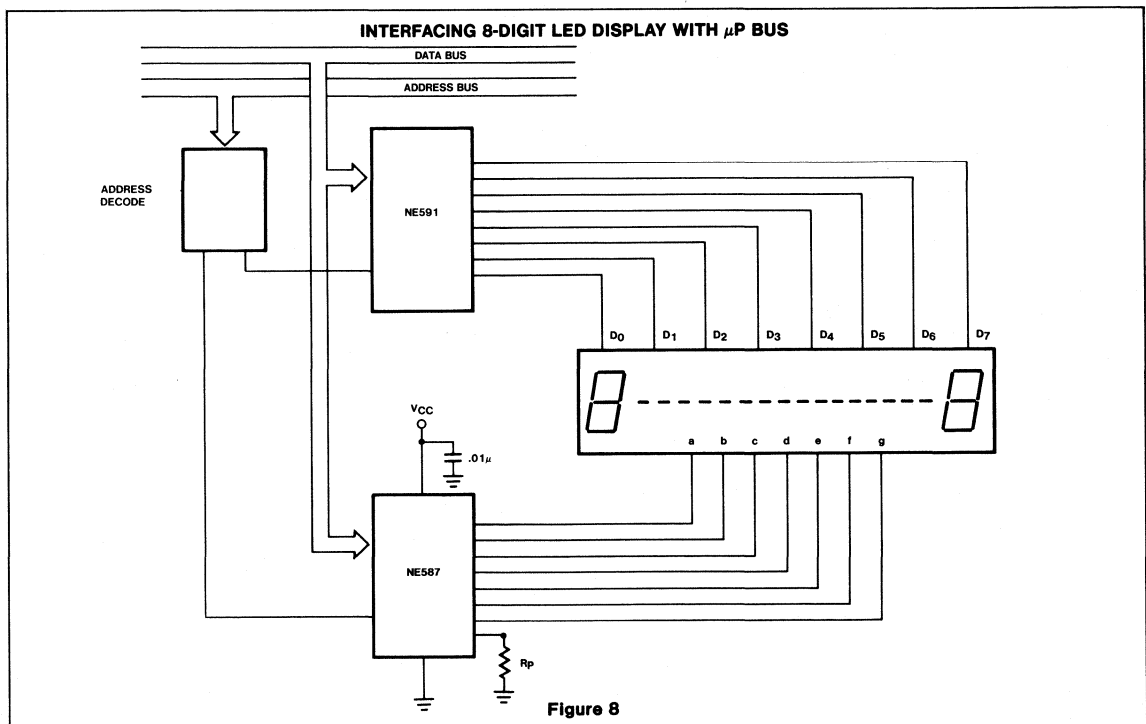
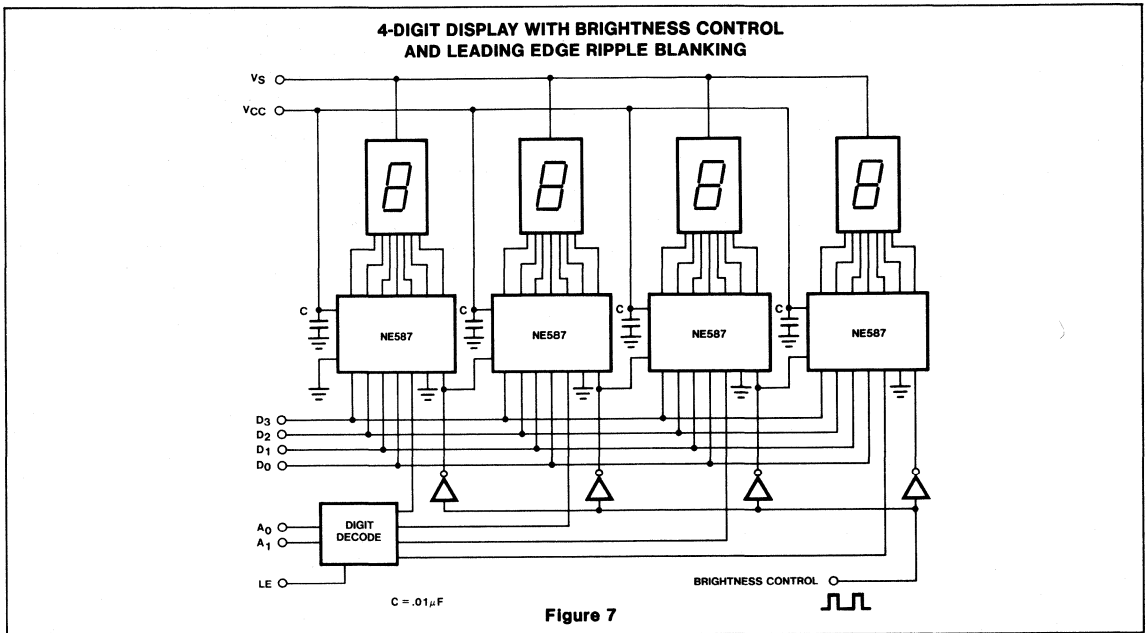
The duty cycle is approximately 60%.

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LED DECODER/DRIVER

NE587

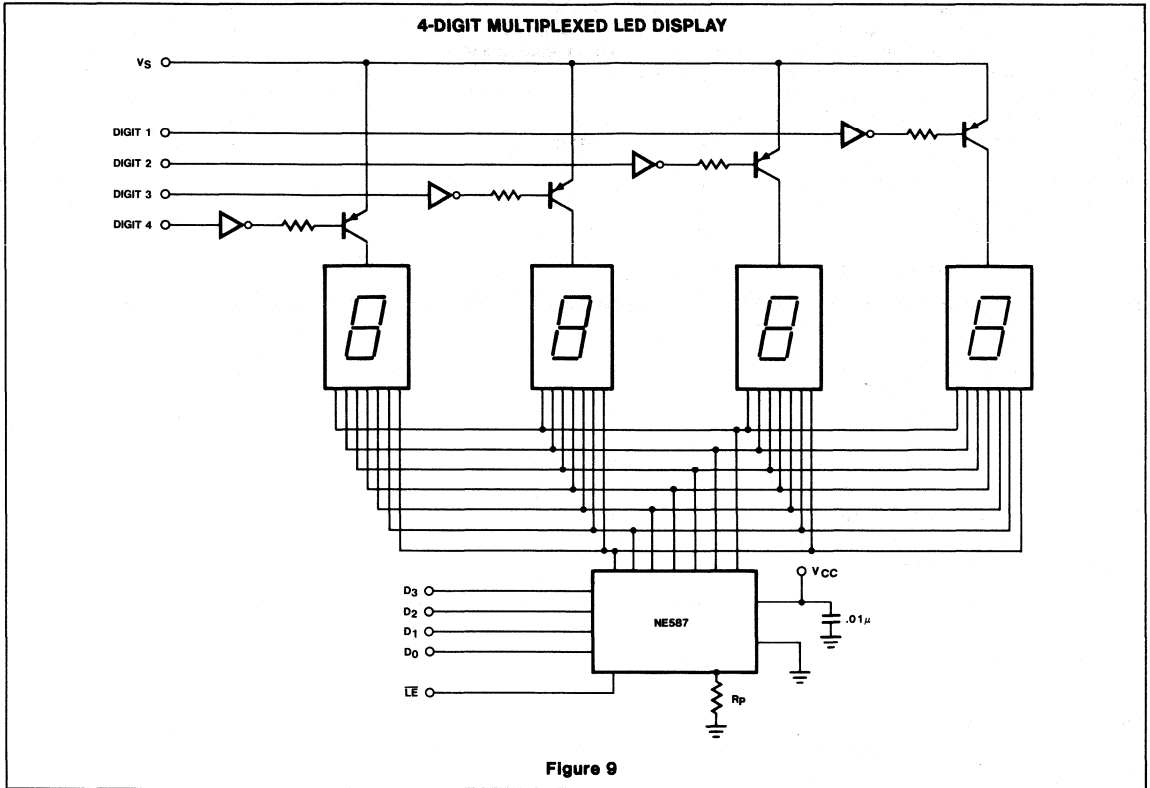
TYPICAL APPLICATIONS (Cont'd)



LED DECODER/DRIVER

NE587

TYPICAL APPLICATIONS (Cont'd)



LED DECODER/DRIVER

NE589

Preliminary

DESCRIPTION

The NE589 is a latch/decoder/driver for 7-segment common cathode LED displays. The NE589 has a programmable current output up to 50mA which is essentially independent of output voltage, power supply voltage, and temperature. The data (BCD) inputs and \overline{LE} (latch enable) input are low-loading so that they are compatible with any data bus system. The 7-segment decoding is implemented with a ROM so that alternative fonts can be made available.

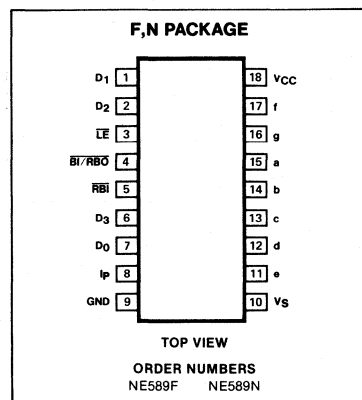
FEATURES

- Latched BCD inputs
- Low loading bus-compatible inputs
- Ripple-blanking on leading and/or trailing edge zeros

APPLICATIONS

- Digital panel meters
- Measuring instruments
- Test equipment
- Digital clocks
- Digital bus monitoring

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified

PARAMETER	RATING	UNIT
V_{CC}, V_S Supply voltage	-0.5 to +7	V
V_{IN} Input voltage ($D_0 - D_3, \overline{LE}, \overline{RBI}$)	-0.5 to +15	V
V_{OUT} Output voltage (a-g, RBO)	-0.5 to +7	V
P_D Power dissipation (25°C) ¹	1000	mW
T_A Ambient temperature range	0 to 70	$^\circ\text{C}$
T_J Junction temperature	150	$^\circ\text{C}$
T_{STG} Storage temperature range	-65 to +150	$^\circ\text{C}$
T_{SOLD} Soldering temperature (10 sec. max)	300	$^\circ\text{C}$

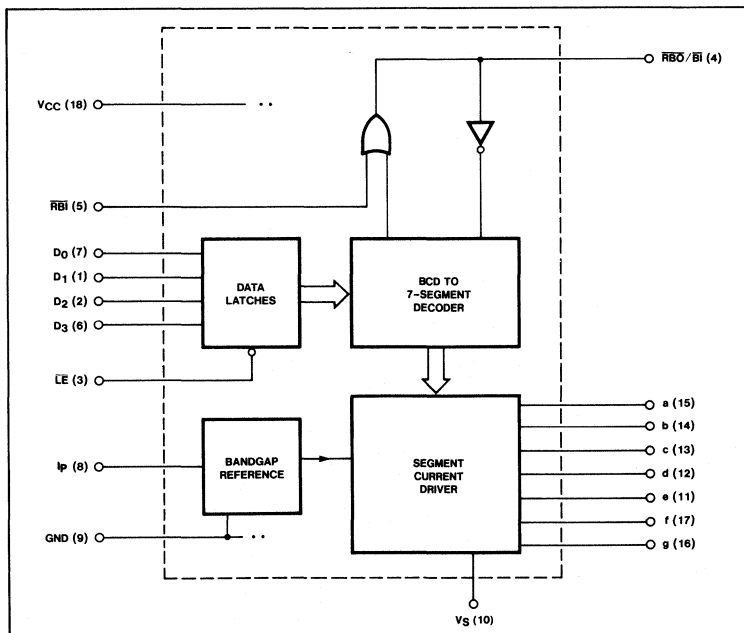
NOTE

Derate power dissipation as indicated

N package - $95^\circ\text{C}/\text{watt}$ above 55°C

F package - $100^\circ\text{C}/\text{watt}$ above 50°C

BLOCK DIAGRAM



LED DECODER/DRIVER

NE589

Preliminary

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 4.75$ to $5.25V$, $0^{\circ}C < T_A < 70^{\circ}C$. Typical values are at $V_{CC} = V_S = 5V$, $T_A = 25^{\circ}C$, $R_P = 7k\Omega$ ($\pm 1\%$) unless otherwise stated.

PARAMETER	TEST CONDITIONS	NE589			UNIT
		Min	Typ	Max	
V_{CC}, V_S Operating supply voltage		4.75	5.00	5.25	V
V_{IH} Input high voltage	All Inputs except \overline{BI} \overline{BI}	2.0		15	V
V_{IL} Input low voltage				0.8	V
V_{IC} Input clamp voltage	$I_{IN} = -12mA$, $T_A = 25^{\circ}C$			-1.5	V
I_{IH} Input high current	Inputs $D_0 - D_3, \overline{LE}, \overline{RBI}$ $V_{IN} = 2.4V$ $V_{IN} = 15V$		0.1		μA μA
I_{IH} Input high current	Input \overline{BI} (pin 4) $\overline{RBI} = H$ $V_{IN} = V_{CC} = 5.25V$		10		μA
I_{IL} Input low current	$V_{IN} = 0.4V$, Inputs $D_0 - D_3$ $\overline{LE}, \overline{RBI}$		-5 -200		μA
I_{IL} Input low current	Input \overline{BI} $V_{CC} = 5.25V$ $\overline{RBI} = H, V_{IN} = 0.4V$		-0.7		mA
V_{OL} Output low voltage	Output \overline{RBO} $I_{OUT} = 3.0mA$				V
V_{OH} Output high voltage	Output \overline{RBO} $I_{OUT} = -50\mu A$ $\overline{RBI} = H$		4.5		V
I_{OUT} Output segment "ON" current	Outputs "a" thru "g" $V_{OUT} = 2.0V$	20	25	30	mA
ΔI_{OUT} Output current ratio (all outputs ON)	With reference to "b" segment $V_{OUT} = 2.0V$	0.90	1.00	1.10	
I_{OFF} Output segment "OFF" current	Outputs "a" thru "g"		20	250	μA
I_{CCO} Supply current	$V_{CC} = 5.25V$ All outputs "ON" $V_{OUT} > 1V$		25		mA
I_{CCI} Supply current	$V_{CC} = 5.25V$ All outputs blanked		30		mA

LED DECODER/DRIVER

NE589

Preliminary

AC ELECTRICAL CHARACTERISTICS $V_{CC} = V_S = 5V$, $T_A = 25^\circ C$, $R_L = 130\Omega$, $C_L = 30pF$ including probe capacity.

PARAMETER	TEST CONDITIONS	NE589			UNIT
		Min	Typ	Max	
$t_{D_{av}}$ Propagation delay Figure 2	From data to output		135		ns
$t_{D_{av}}$ Propagation delay Figure 3	From \overline{LE} to output		135		ns
t_W Latch enable pulse width Figure 4		85			ns
t_S Latch enable setup time Figure 4	From data to \overline{LE}	75			ns
t_H Latch enable hold time Figure 4	From \overline{LE} to data	0			ns

NOTE:

$$t_{D_{AV}} = \max(t_{HL} + t_{LH})$$

TRUTH TABLE

BINARY INPUT	INPUTS						OUTPUTS								DISPLAY
	\overline{LE}	\overline{RBI}	D_3	D_2	D_1	D_0	a	b	c	d	e	f	g	\overline{RBO}	
—	H	*	X	X	X	X	STABLE								STABLE BLANK
0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	
0	L	H	L	L	L	L	H	H	H	H	H	L	L	H	0
1	L	X	L	L	L	H	L	H	H	L	L	L	L	H	1
2	L	X	L	L	H	L	H	H	L	H	H	L	H	H	2
3	L	X	L	L	H	H	H	H	H	H	L	L	H	H	3
4	L	X	L	H	L	L	L	H	H	H	L	L	H	H	4
5	L	X	L	H	L	H	H	L	H	H	L	L	H	H	5
6	L	X	L	H	H	L	H	H	L	H	L	L	H	H	6
7	L	X	L	H	H	H	H	H	H	H	L	L	L	H	7
8	L	X	H	L	L	L	H	H	H	H	H	H	H	H	8
9	L	X	H	L	L	H	H	H	H	H	L	L	H	H	9
10	L	X	H	L	H	L	H	H	H	H	L	L	H	H	a
11	L	X	H	L	H	H	L	L	H	H	H	H	H	H	b
12	L	X	H	H	L	L	H	L	L	H	H	L	L	H	c
13	L	X	H	H	L	H	L	H	H	H	L	L	H	H	d
14	L	X	H	H	H	L	H	L	L	H	H	L	L	H	e
15	L	X	H	H	H	H	H	L	L	L	H	L	L	H	f
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	blank

NOTES

H = HIGH voltage level, output is "ON"

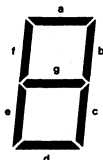
L = LOW voltage level, output is "OFF"

X = Don't care

* The \overline{RBI} will blank the display only if a binary zero is stored in the latches.

** \overline{RBO}/BI used as an input overrides all other input conditions.

SEGMENT IDENTIFICATION



LED DECODER/DRIVER

NE589

Preliminary

NE589 PROGRAMMING

NE589 output current can be programmed by using a programming resistor, R_p , connected between r_p (pin 8) and Gnd (pin 9). The voltage at r_p (pin 8) is constant ($\approx 1.3V$). A partial schematic of the voltage reference used in the NE589 is shown in figure 1.

Output current to program current ratio, I_O/I_p , is 120 in the 10mA to 50mA range. Note that I_p must be derived from a resistor (R_p), and not from a high impedance source such as an I_{OUT} DAC used to control display brightness.

POWER DISSIPATION CONSIDERATIONS

LED displays are power-hungry devices, and inevitably somewhat inefficient in their use of the power supply necessary to drive them. Duty cycle control does afford one way of improving display efficiency, provided that the LEDs are not driven too far into saturation, but the improvement is marginal. Operation at higher peak currents has the added advantage of giving much better matching of light output, both from segment-to-segment and digit-to-digit.

An output current of 10 to 50mA was chosen so that it would be suitable for multiplexed operation of large size LED digits. When designing a display system, particular care must be taken to minimize power dissipation within the IC display driver. Since the output is a constant current source, all the remaining supply voltage, which is not dropped across the LED (and the digit driver, if used), will appear across the output. Thus, the power dissipation will go up sharply if the display power supply voltage rises. Clearly, then, it is good design practice to keep the display supply voltage as low as possible consistent with proper operation of the supply output current sources. Inserting a resistor or diode in series with the display supply is a good way of reducing the power dissipation within the integrated circuit segment driver, although, of course, total system power remains the same.

Power dissipation may be calculated as follows. Referring to figure 5, the two system power supplies are V_{CC} and V_S . In many cases, these will be the same voltage. Necessary parameters are:

- V_{CC} , Supply voltage to driver
- V_S , Supply voltage to display
- I_{CC} , Quiescent supply current of driver
- I_{SEG} , LED segment current
- V_F , LED segment forward voltage at I_{seg}
- KDC , % Duty cycle

V_F , the forward LED drop, depends upon the type of LED material (hence the color) and the forward current. The actual forward voltage drops should be obtained from the LED display manufacturer's literature for the peak segment current selected; however, approximate voltages at nominal rated currents are:

Red	1.6 to 2.0V
Orange	2.0 to 2.5V
Yellow	2.2 to 3.5V
Green	2.5 to 3.5V

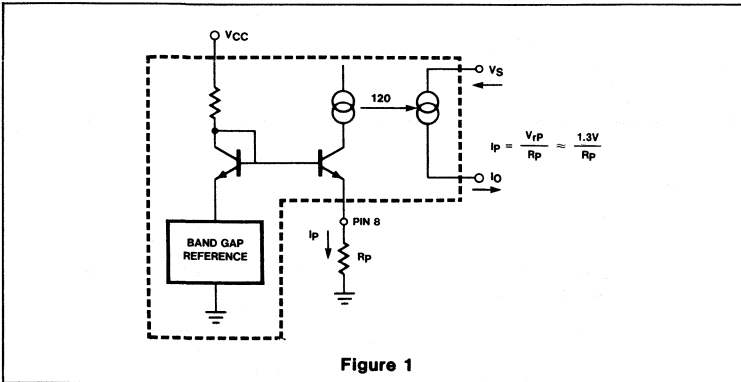


Figure 1

TIMING DIAGRAMS

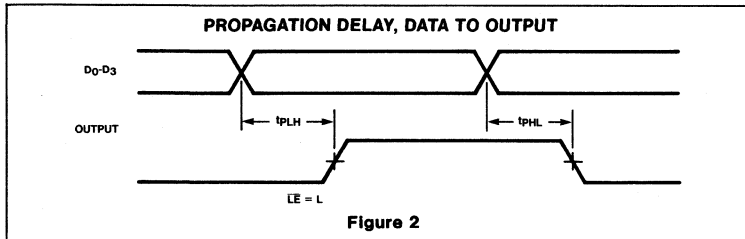


Figure 2

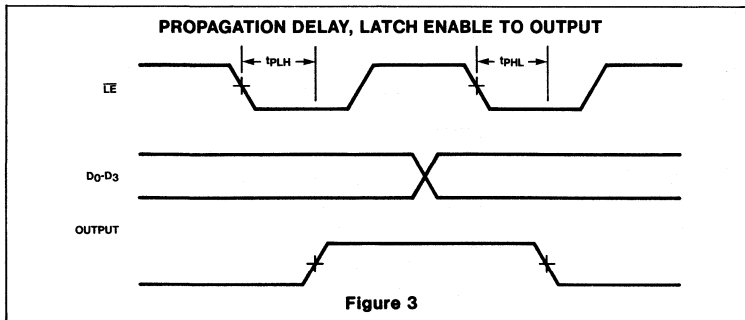


Figure 3

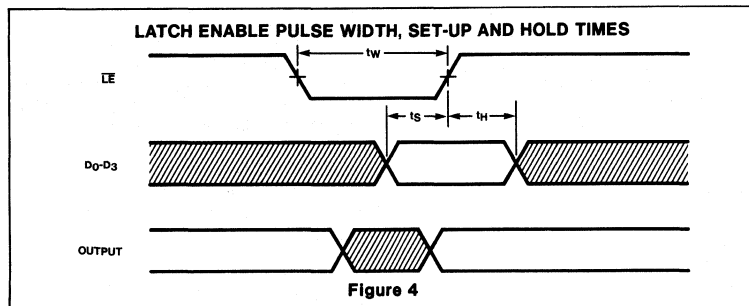
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LED DECODER/DRIVER

NE589

Preliminary

TIMING DIAGRAMS (Cont'd)



These voltages are all for single diode displays. Some early red displays had 2 series LEDs per segment; hence the forward voltage drop was around 3.5V.

Thus a maximum power dissipation calculation when all segments are on, is:

$$P_d = V_{CC} \times I_{CC} + (V_S - V_F) \times 7 \times I_{aeg} \times K_{DC} \text{ mW}$$

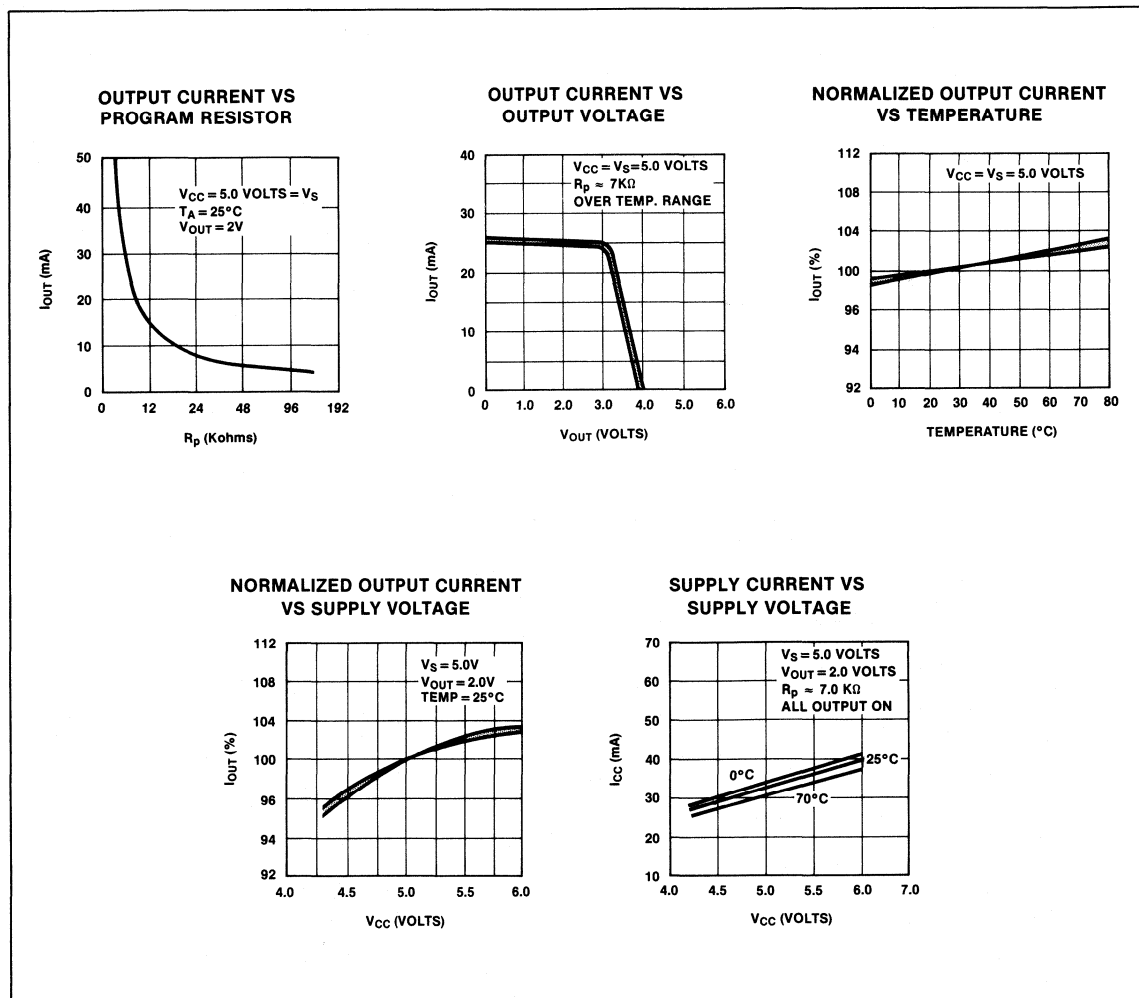
Assuming $V_S = V_{CC} = 5.25V$

$V_F = 2.0V$

$K_{DC} = 100\%$

$$P_d \text{ max} = 5.25 \times 50 + 3.25 \times 7 \times 30 \text{ mW} = 945 \text{ mW}$$

TYPICAL PERFORMANCE CURVES

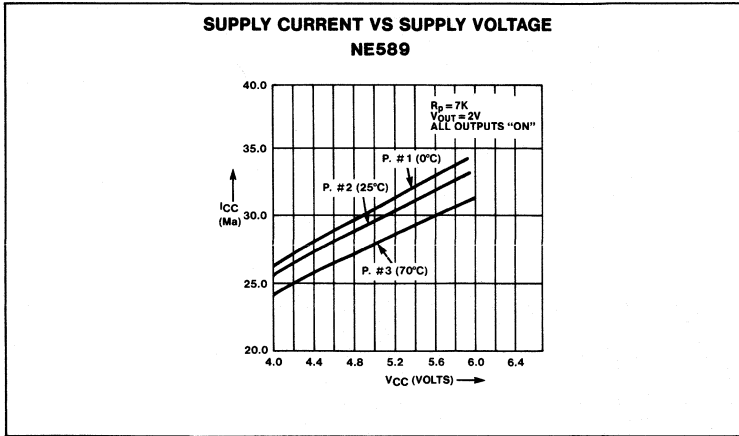


LED DECODER/DRIVER

NE589

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TYPICAL PERFORMANCE CURVES (Cont'd)



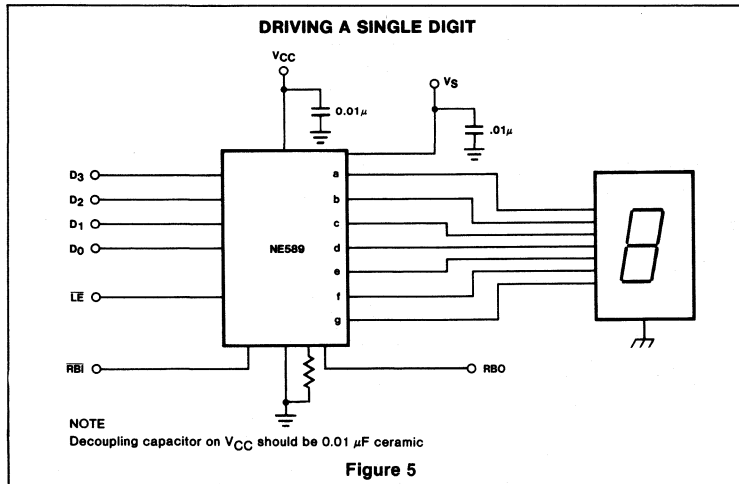
If a diode (or 2) is used to reduce voltage to the display, then the voltage appearing across the display driver will be independent of the number of "ON" segments and will be equal to

$$V_S - V_F - nV_D, V_D \approx 0.8V$$

Where n is the number of diodes used, power dissipation can be calculated in a similar manner.

In a multiplexed display system, the voltage drop across the digit driver must also be considered in computing device power dissipation. It may even be an advantage to use a digit driver which drops an appreciable voltage, rather than the saturating PNP transistors shown in figure 8. For example a darlington PNP or NPN emitter follower may be preferable. Figure 7 shows the NE591 as the digit driver in a multiplexed display system. The NE591 output drops about 1.8V which means that the power dissipation is evenly distributed between the two integrated circuits.

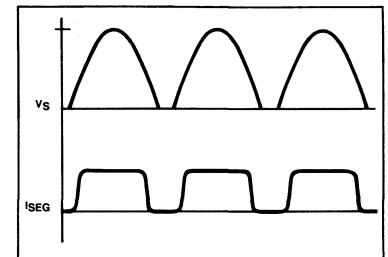
TYPICAL APPLICATIONS



NOTE
Decoupling capacitor on V_{CC} should be 0.01 µF ceramic

Figure 5

Where V_S and V_{CC} are two different supplies, the V_S supply may be optimized for minimum system power dissipation and/or cost. Clearly, good regulation in the V_S supply is totally unnecessary, and so this supply can be made much cheaper than the regulated 5V supply used in the rest of the system. In fact a simple unsmoothed full-wave rectified sine wave works extremely well if a slight loss in brightness can be tolerated. A transformer voltage of about 3-4.5V rms works well in most LED display systems. Waveforms are shown below:



The duty cycle for this system depends upon V_S, V_F and the output characteristics of the display driver.

With
V_S = 4.9V pk.
V_F = 2.0V

The duty cycle is approximately 60%.

However, the average power dissipation will be considerably less than this. Assuming 5 segments are on (the average for all output code combinations), then

$$P_{d\text{ av}} = 5.0 \times 30 + 3.00 \times 5 \times 25 \text{ mW} = 525 \text{ mW}$$

Operating temperature range limitations can be deduced from the power dissipation graph in figure 9.

However, a major portion of this power dissipation (P_{d max}) is because the current source output is operating with 3.25 V across it. In practice, the outputs operate satisfactorily down to 0.5V, and so the extra voltage may be dropped external to the integrated circuit.

Suppose the worst case V_{CC}/V_S supply is 4.75 to 5.25V, and that the maximum V_E for the LED display is 2.25V. Only 2.75V is required to keep the display active, and hence 2.0V may be dropped externally with a resistor from V_{CC} to V_S. The value of this resistor is calculated by:

$$R_S = \frac{2.0}{7 \times I_{\text{seg}}} \approx 10\Omega \text{ (} \frac{1}{2} \text{ W rating)}$$

assuming worst case I_{seg} of 30 mA
Hence now P_{d max} = V_{CC} × I_{CC} + (V_S - V_F - R_X × 7 × I_{seg}) × 7 × I_{seg} × K_{DC}
= 5.25 × 50 + 1.25 × 7 × 30 mW
= 525 mW

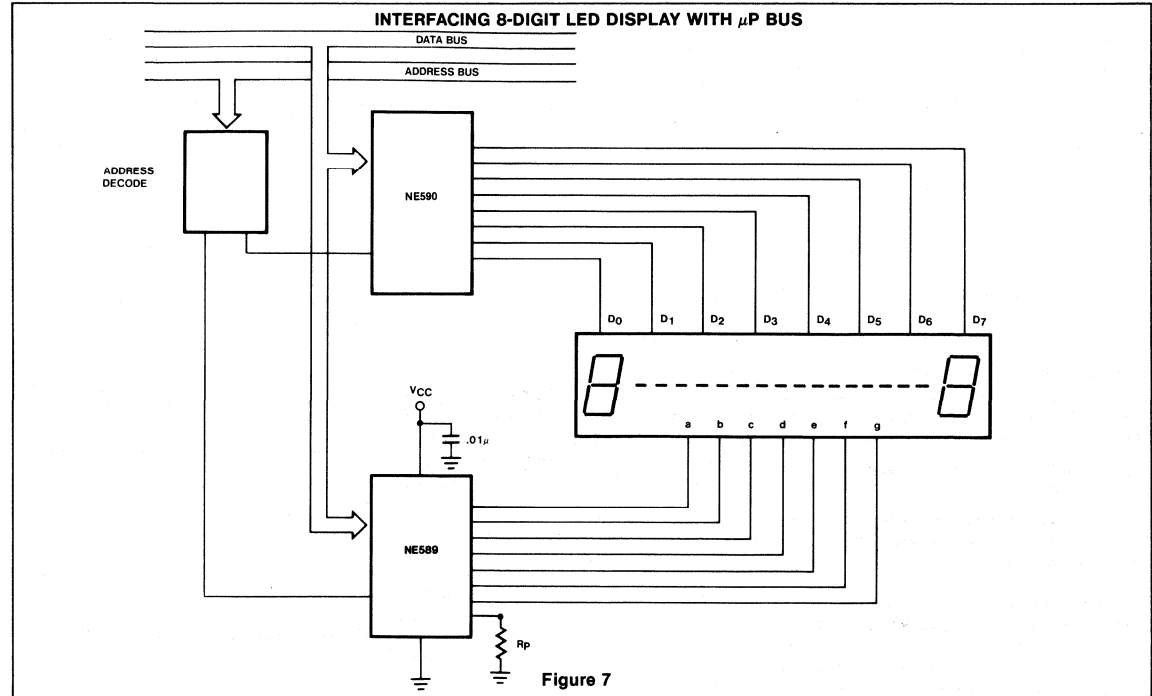
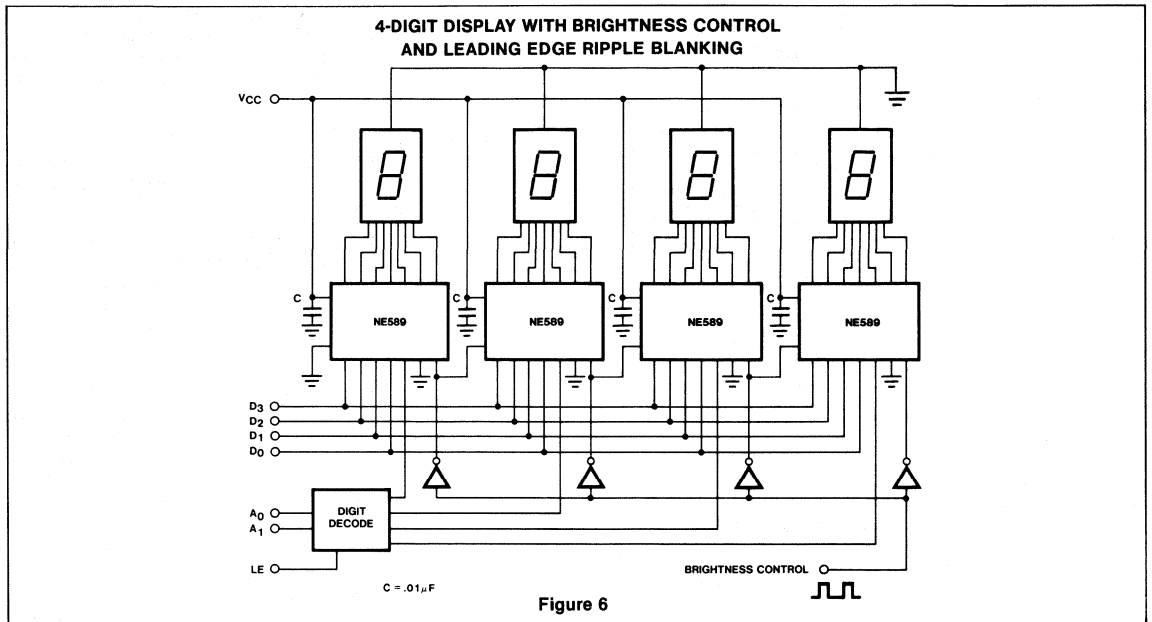
and P_{d av} = 5.0 × 30 + 1.25 × 5 × 25 = 306 mW

LED DECODER/DRIVER

NE589

Preliminary

TYPICAL APPLICATIONS (Cont'd)

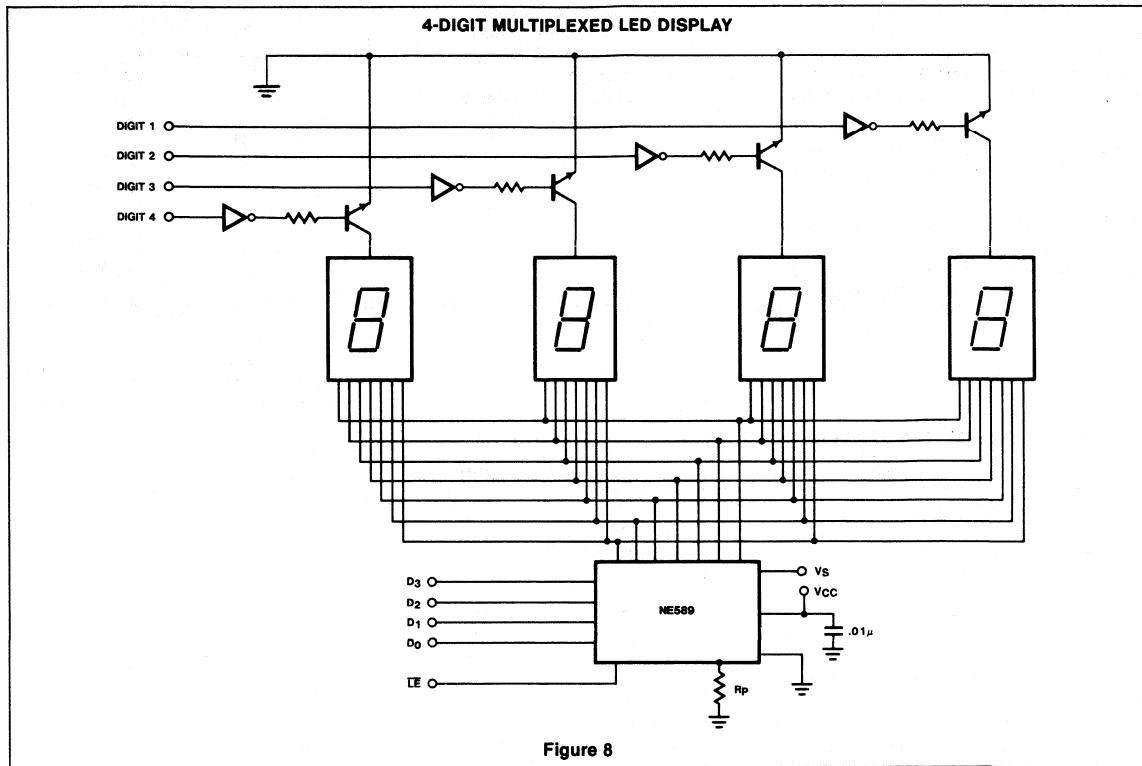


LED DECODER/DRIVER

NE589

Preliminary

TYPICAL APPLICATIONS (Cont'd)



VACUUM FLUORESCENT DISPLAY DRIVER

NE/SA594

DESCRIPTION

The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

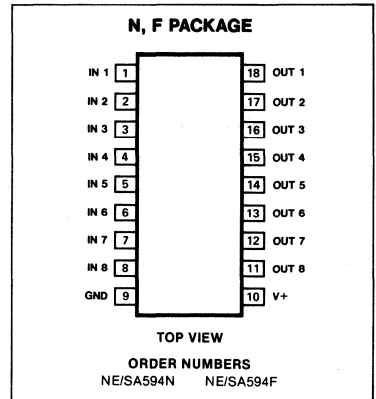
The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

FEATURES

- Digit and/or segment drivers
- Active output pull-down circuitry
- High output breakdown voltage
- Low supply voltage
- Input compatible with all logic outputs

PIN CONFIGURATION



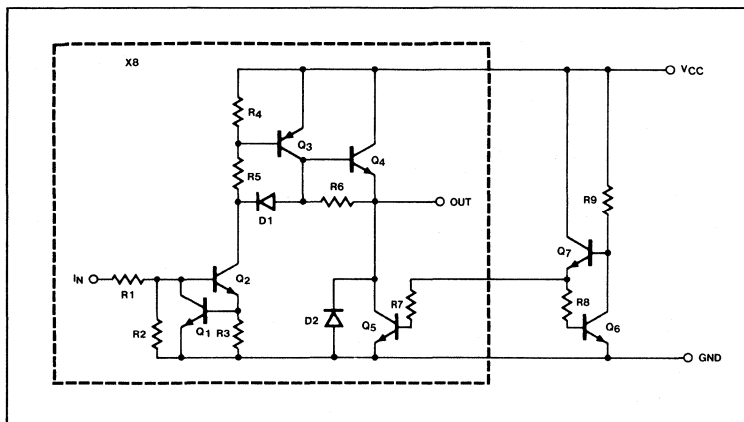
ABSOLUTE MAXIMUM RATINGS (at 25°C unless otherwise noted)

PARAMETER	RATING	UNIT	
VCC	Supply voltage	45	V
VOUT	Output voltage	VCC	
VIN	Input voltage	-0.3, +20	V
IOUT	Output current		
	Each output	50	mA
	All outputs	200	mA
Pd	Power dissipation* (at 25°C)	800	mW
TA	Operating temperature range		
	NE	0 to 70	°C
	SA	-40 to +85	°C
TSTG	Storage temperature range	-65 to +150	°C
TJ	Maximum junction temperature	150	°C
TSOLD	Lead soldering temperature (10 seconds)	300	°C

NOTE

*Derate N (Plastic) Package above 38°C at 7.14 mW/°C.
Derate F (Ceramic) Package above 75°C at 10.8 mW/°C.

EQUIVALENT SCHEMATIC



VACUUM FLUORESCENT DISPLAY DRIVER

NE/SA594

DC ELECTRICAL CHARACTERISTICS $V_{CC} = +4.75$ to $+40V$, T_A (NE) = 0 to $70^\circ C$, T_A (SA) = -40 to $+85^\circ C$ unless otherwise stated.

SA594	PARAMETER	TEST CONDITIONS		NE/SA594			UNIT
				Min	Typ	Max	
V_{CC}	Supply voltage range			4.75	35	40	V
I_{CCH}	Supply current (all outputs high)	$V_{CC} = 40V$	$V_{IN} = 3.5V$		3	6	mA
I_{CCL}	Supply current (all outputs low)	$V_{CC} = 40V$	$V_{IN} = 0.4V$		0.4	1	mA
V_{IN}	Input voltage range			0		15	V
V_{IH}	Input voltage to ensure logic '1'			2.6			V
V_{IL}	Input voltage to ensure logic '0'					0.8	V
I_{IH}	Input current to ensure logic '1'			100			μA
I_{IL}	Input current to ensure logic '0'					10	μA
I_{IN}	Input current		$V_{IN} = 2.6V$		60	130	μA
			$V_{IN} = 5.0V$		180	330	μA
			$V_{IN} = 15.0V$.68	1.3	mA
V_{OH}	Output high voltage	$V_{IN} = 3.5V$	$T_A = 25^\circ C$	$V_{CC}-1.5$	$V_{CC}-1.1$		V
		$I_{OUT} = -25mA$	Over Temp.	$V_{CC}-2$	$V_{CC}-1.3$		V
		V_{OUT} with respect to V_{CC}					
V_{OH}	Output high, no load voltage	$V_{IN} = 3.5V$	$I_{OUT} = 0, T_A = 25^\circ C$	$V_{CC}-1$	$V_{CC}-0.8$		V
		V_{OUT} with respect to V_{CC}					
V_{OFF}	Output 'OFF' voltage level	$V_{IN} = 0.8V$	$I_{OUT} = 0$		10	200	mV
I_{OH}	Available output current	$V_{CC} = 35V$	$V_{IN} = 3.5V$	-35			mA
		$V_{OUT} = 30V$	$T_A = 25^\circ C$				
I_{OUT}	Output pulldown current	$V_{CC} = V_{OUT} = 35V$	Inputs open	100	200	400	μA
I_{CEX}	Output leakage current	$T_A = 25^\circ C$	$V_{IN} = 0.4V$		-1		μA
		$V_{CC} = 40V$	$V_{OUT} = 0V$		-1		

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AC ELECTRICAL CHARACTERISTICS¹ $V_{CC} = 35V$, $T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	NE/SA594			UNIT
		Min	Typ	Max	
t_{pDLH}	Propagation delay - low to high output transition.		1	5	μS
t_{pDHL}	Propagation delay - high to low output transition.		3	10	μS
t_R	Output rise time		0.5	3	μS
t_F	Output fall time		1.5	5	μS

NOTE

1. See figure 1

VACUUM FLUORESCENT DISPLAY DRIVER

NE/SA594

SWITCHING TIMES OF DRIVERS

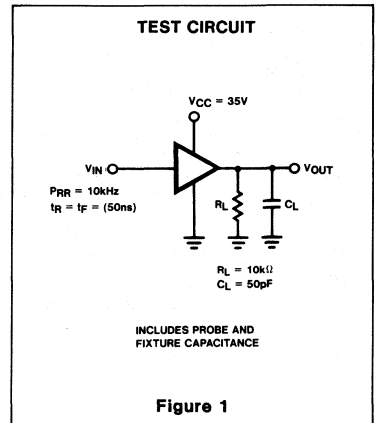
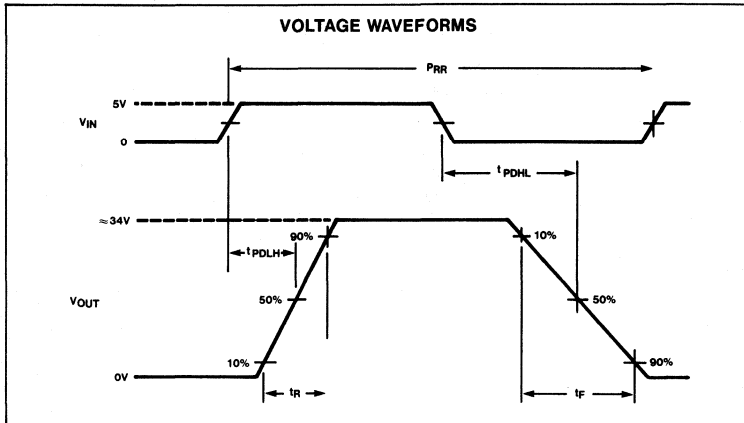
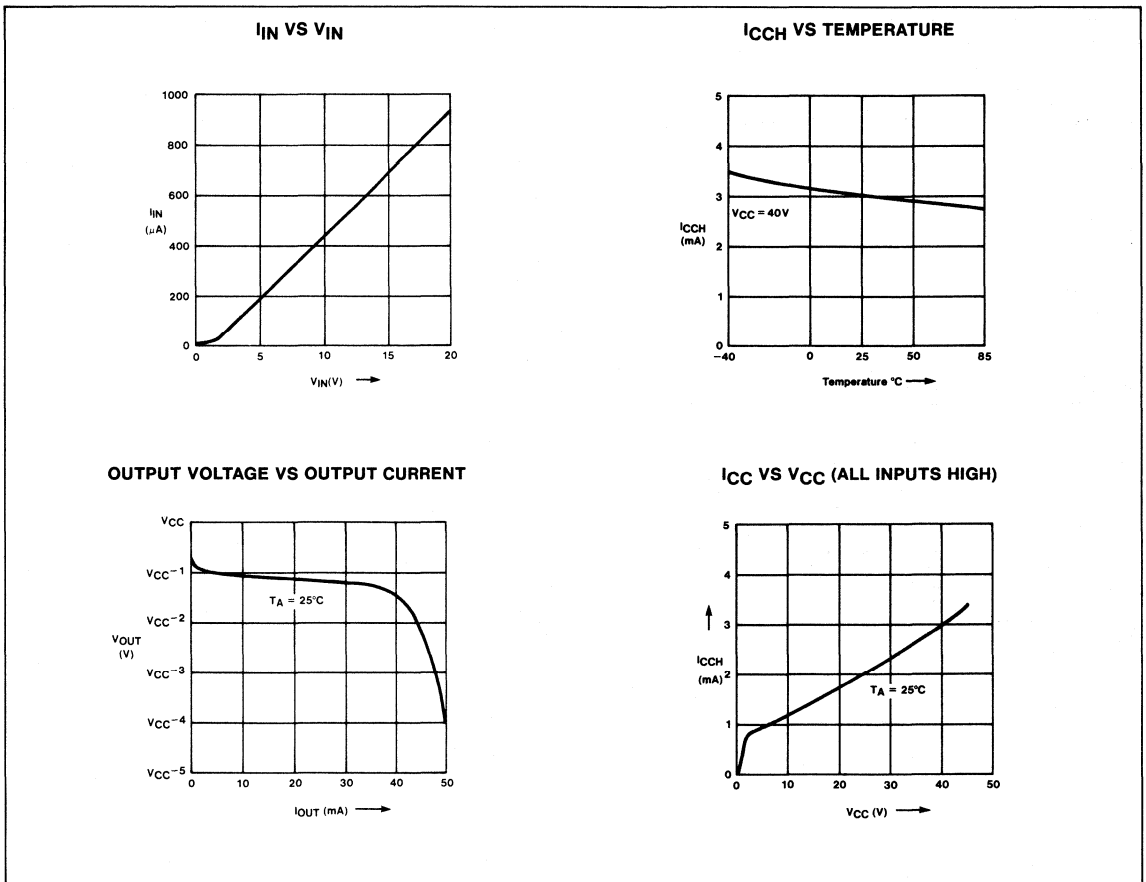


Figure 1

TYPICAL PERFORMANCE CHARACTERISTICS



VACUUM FLUORESCENT DISPLAY DRIVER

NE/SA594

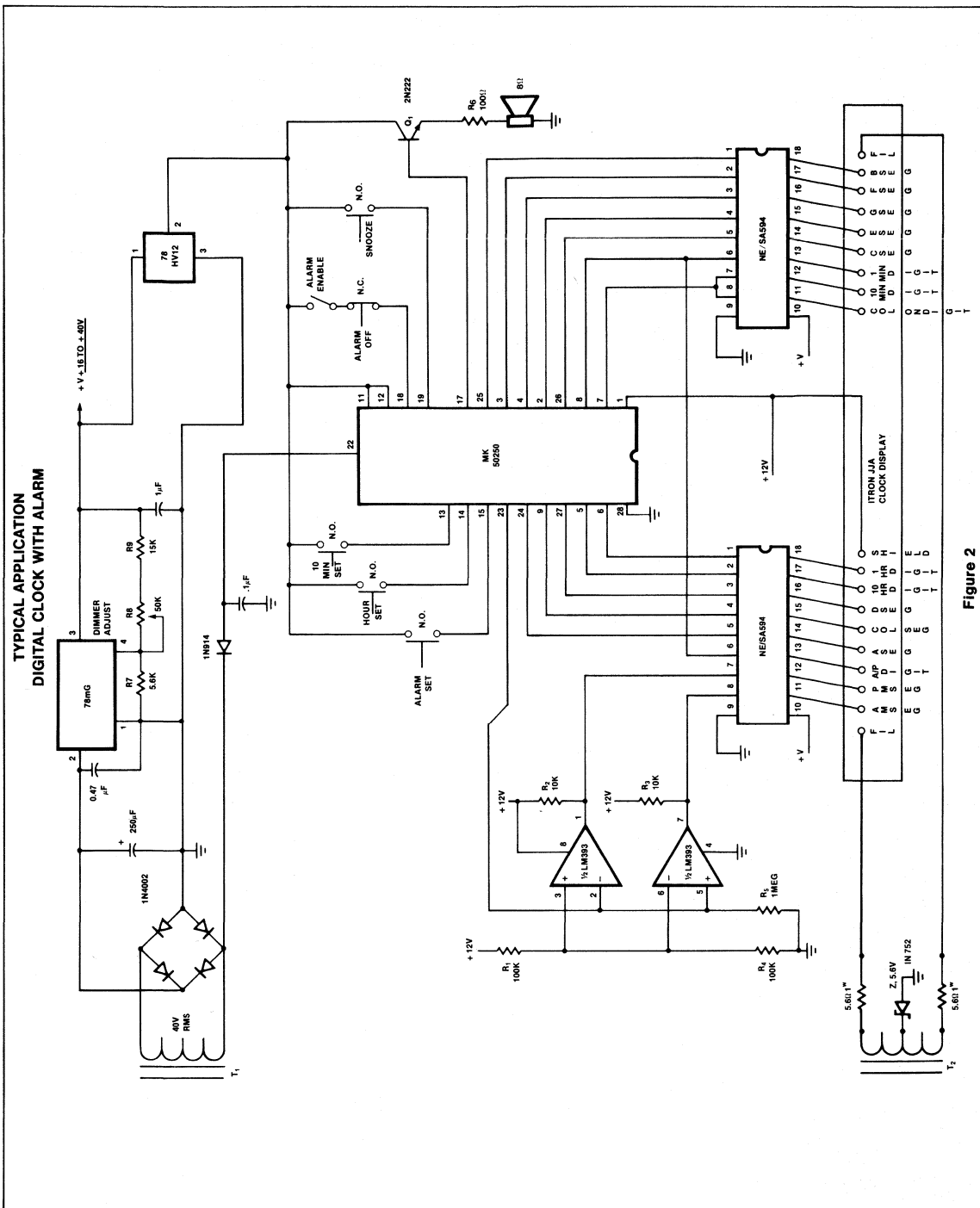


Figure 2

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Section 11 A/D and D/A Converters



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Section 11 — A/D and D/A Converters

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A/D AND D/A CONVERTERS—SYMBOLS AND DEFINITIONS

TA

Ambient temperature range. Range of the surrounding environment of the operating device.

TJ

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

TSTG

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

TSOLD

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low

1 is logic level high

X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

VCC (-VCC)

Supply Voltage. The range of power supply voltage over which the device will operate safely.

Accuracy

The maximum deviation of the DAC output relative to an ideal straight line drawn from zero to full scale.

Monotonicity

For a 1 LSB increase of input code, the output of a DAC either increases or remains the same.

Differential Linearity

The incremental error from an ideal 1 LSB analog output change when the digital input is changed 1 LSB; guaranteed monotonicity requires the differential linearity error be less than 1 LSB.

Absolute Accuracy

Error of a D/A converter output is the difference between the analog output expected and the actual output with a given code applied. Error of an A/D converter is the difference between the theoretical analog output required to produce a given output code and the actual input required to produce a given output code and the actual input required to produce that same code. The actual input is a range and the measured value is the midpoint of the measured band and the theoretical midpoint.

Resolution

The number of bits on the input or output of an A/D or D/A converter. The number of discrete steps or states is equal to 2^n when n is

the resolution of the converter. However, n bits of resolution does not guarantee n bits of accuracy.

Quantizing Error

In an A/D converter, there is an infinite number of possible input voltages, but only 2^n output codes (n = number of bits). Therefore, there will be an error as great as $1/2$ LSB because of this quantizing effect and the greatest error will occur at the transition voltage where the output changes state.

No Missing Codes

This is a property of an A/D converter that is related to, but is more stringent than monotonicity. If a converter is guaranteed to have no missing codes, there will be no output digital state that will be skipped when the input voltage is varied over the entire range.

Most Significant Bit (MSB)

The highest-order bit or the bit with the greatest weight.

Least Significant Bit (LSB)

The lowest-order bit or the bit with the least weight.

Gain Error

The error in the input-to-output ratio, usually expressed in percent of full scale range.

Offset Error

This is an error in the reference point of the transfer function. It appears as a constant amplitude error signal at a DAC output or an ADC input. It also appears as a constant frequency shift in the output of a V/F converter. It is nulled prior to adjusting gain error by setting the input to the most-negative input and adjusting the output to the proper value.

Settling Time

The time delay in a D/A converter between a change of input digital code and the effected change in the output signal. It is usually expressed in terms of how long it takes the output to settle to, and remain within, a certain error band around the final value and is usually specified for full-scale range changes.

Conversion Time

Time required for a complete conversion cycle of an A/D converter. Conversion time is a function of the number of bits (resolution) and the clock frequency.

Full Scale Tempco

The change in DAC full scale current or voltage with change in temperature expressed in ppm/°C.

Differential Non-Linearity Tempco

The non-linearity specification over a specified range of temperatures. This specification generally appears as the range of temperatures that the device is monotonic (DAC) or has no missing codes (ADC).

Leakage Current

In a current output D/A converter, there is a digital input code that ideally yields zero output current. If current flows with that input code, it is called leakage current. It is analogous to output voltage offset in a voltage-output D/A converter.

Power Supply Sensitivity

The change in DAC output current or voltage with changes in power supply voltage.

A/D AND D/A CONVERTERS—SYMBOLS AND DEFINITIONS

Output Voltage Compliance

The range of allowable voltage levels at the output of a D/A converter that does not degrade accuracy.

Compliance Voltage Range

For a current output DAC, the maximum range of voltage for which the current source will maintain its specified values.

NOTE

Refer to Section 5 (Interface Circuits) of the 1979 Analog Applications Manual for an in-depth explanation of Converters and their applications

SE/NE 5018 DAC

COMPETITION	INDUSTRY VALUE	KEY PARAMETER	SIGNETICS AVAILABLE VALUE	SIGNETICS ORIGINATED DEVICES	QR&A		COMMENTS
					SURE II	SUPR II	
AMD*	8	Resolution (Bits)	8	NE5018 SE5018 NE5019 SE5019	Yes Yes Yes Yes	Yes Yes Yes Yes	*Not pin for pin replacement. Do not have total capability of the NE5018 μ P compatible series.
Analog Devices*			Bits				
Datel	19	Linearity	0.1				
Fairchild*			%				
Harris*			2-300 μ sec	Settling Time $\frac{1}{2}$ LSB	2		
Precision Monolithics					μ sec		
National*	10-50	Gain TC	20				
			PPM/ $^{\circ}$ C				
	0-4	Current (Output)		NE/SE 5118 NE/SE 5119	Yes Yes	Yes Yes	
			mA				
	-10 to +18	Voltage (Output)	0-10 \pm 5	NE5018 SE5019	Yes Yes	Yes Yes	
			Volts				

8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

DAC-08 SERIES

FORMERLY: NE5007/5008-F,N
SE5008-F

DESCRIPTION

The DAC-08 series of 8-bit monolithic multiplying Digital-to-Analog Converters provide very high speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 20 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

Dual complementary outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. True high voltage compliance outputs allow direct output voltage conversion and eliminate output op amps in many applications.

All DAC-08 series models guarantee full 8-bit monotonicity and linearities as tight as 0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the $\pm 4.5V$ to $\pm 18V$ power supply range, with 33mW power consumption attainable at $\pm 5V$ supplies.

The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
T_A	Operating temperature range DAC-08, DAC-08A DAC-08C,E	$^{\circ}C$
t_{stg}	Storage temperature	$^{\circ}C$
P_D	Power dissipation	mW
	Lead soldering temperature (60sec)	$^{\circ}C$
	V_+ to V_- supply	V
V_{LC}	Logic inputs Logic threshold control Analog current outputs	V_- to V_- plus 36V V_- to V_+ See output current or output voltage performance curve
V_{14}, V_{15}	Reference inputs	V_- to V_+
V_{14} to V_{15}	Reference input differential voltage	± 18
I_{14}	Reference input current	5.0 mA

FEATURES

- Fast settling output current—85ns
- Full scale current prematched to ± 1 LSB
- Direct interface to TTL, CMOS, ECL, HTL, PMOS
- Relative accuracy to 0.1% maximum over temperature range
- High output compliance $-10V$ to $+18V$
- True and complemented outputs
- Wide range multiplying capability
- Low FS current drift— $\pm 10ppm/^{\circ}C$
- Wide power supply range— $\pm 4.5V$ to $\pm 18V$
- Low power consumption—33mW at $\pm 5V$

APPLICATIONS

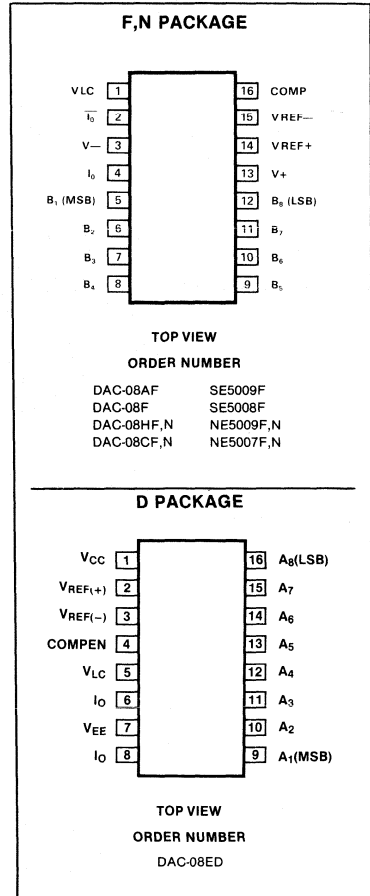
- 8-bit, $1\mu s$ A-to-D converters
- Servo-motor and pen drivers
- Waveform generators
- Audio encoders and attenuators
- Analog meter drivers
- Programmable power supplies
- CRT display drivers
- High speed modems
- Other applications where low cost, high speed and complete input/output versatility are required

ORDERING INFORMATION

RELATIVE ACCURACY	0 to 70°C	-55 to 125°C
0.39% FS	DAC-08CN DAC-08CF DAC-08EN	
0.19% FS	DAC-08EF DAC-08ED	DAC-08F
0.1% FS	DAC-08HF DAC-08HC	DAC-08AF

$T_A = 25^{\circ}C$ unless otherwise noted

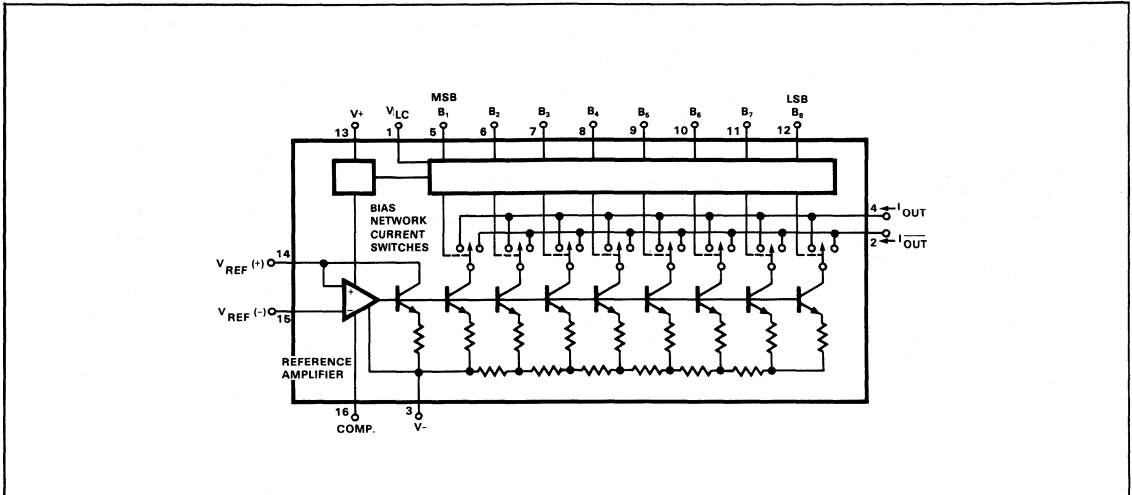
PIN CONFIGURATION



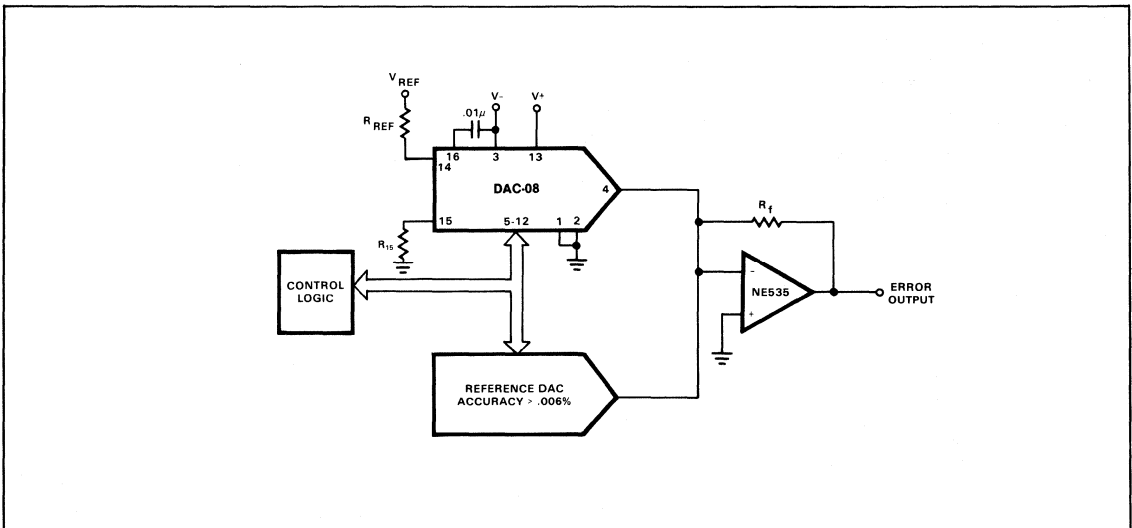
8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

DAC-08 SERIES

BLOCK DIAGRAM



TEST CIRCUIT



8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

DAC-08 SERIES

ELECTRICAL CHARACTERISTICS Pin 3 must be at least 3V more negative than the potential to which R₁₅ is returned.

V_{CC} = ± 15V, I_{REF} = 2.0mA, Output characteristics refer to both I_{OUT} and I_{OUT} unless otherwise noted. DAC-08C, E, H: T_A = 0°C to 70°C. DAC-08/08A: T_A = - 55°C to 125°C.

PARAMETER		TEST CONDITIONS	DAC-08C			DAC-08E DAC-08			DAC-08H DAC-08A			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Resolution		8	8	8	8	8	8	8	8	8	Bits
	Monotonicity*		8	8	8	8	8	8	8	8	8	Bits
	Relative accuracy	Over temperature range			±0.39			±0.19			±0.1	% FS
		Differential nonlinearity			±0.39			±0.19			±0.19	% FS
t _s	Settling time	To ± 1/2 LSB, all bits switched on or off, T _A = 0°C		70	135		70	135		70	135	ns
t _{PLH} t _{PHL}	Propagation delay	T _A = 25°C, each bit. All bits switched										ns
	Low-to-high High-to-low			35	60		35	60		35	60	
TCI _{FS}	Full scale tempco			±10			±10			±10	±50	ppm/°C
V _{OC}	Output voltage compliance	Full scale current change < 1/2 LSB	-10		+18	-10		+18	-10		+18	V
I _{FS4}	Full scale current	V _{REF} = 10.000V, R ₁₄ , R ₁₅ = 5.000kΩ,	1.94	1.99	2.04	1.94	1.99	2.04	1.984	1.992	2.000	mA
I _{FSS}	Full scale symmetry	I _{FS4} - I _{FS2}		±2.0	±16		±1.0	±8.0		±1.0	±4.0	µA
I _{ZS}	Zero scale current			0.2	4.0		0.2	2.0		0.2	1.0	µA
I _{FSR}	Full scale output current range	R ₁₄ R ₁₅ = 5.000kΩ										
		V _{REF} = + 15.0V, V ₋ = - 10V V _{REF} = + 25.0V, V ₋ = - 12V	2.1 4.2			2.1 4.2			2.1 4.2			
V _{IL} V _{IH}	Logic input levels	V _{LC} = 0V			0.8			0.8			0.8	V
	Low High		2.0			2.0			2.0			
I _{IL} I _{IH}	Logic input current	V _{LC} = 0V										µA
	Low High	V _{IN} = -10V to +0.8V V _{IN} = 2.0V to 18V		-2.0 0.002	-10 10		-2.0 0.002	-10 10		-2.0 0.002	-10 10	
V _{IS}	Logic input swing	V ₋ = -15V	-10		+18	-10		+18	-10		+18	V
V _{THR}	Logic threshold range	V _S = ±15V	-10		+13.5	-10		+13.5	-10		+13.5	V
I ₁₅	Reference bias current			-1.0	-3.0		-1.0	-3.0		-1.0	-3.0	µA
di/dt	Reference input slew rate		4.0	8.0		4.0	8.0		4.0	8.0		mA/µs
PSSI _{FS+} PSSI _{FS-}	Power supply sensitivity	I _{REF} = 1mA										%FS/%VS
	Positive Negative	V ₊ = 4.5 to 5.5V, V ₋ = -15V; V ₊ = 13.5 to 16.5V, V ₋ = -15V V ₋ = -4.5 to -5.5V, V ₊ = +15V; V ₋ = -13.5 to -16.5, V ₊ = +15V		0.0003 0.002	0.01 0.01		0.0003 0.002	0.01 0.01		0.0003 0.002	0.01 0.01	
I ₊ I ₋	Power supply current	V _S = ±5V, I _{REF} = 1.0mA		2.3	3.8		2.3	3.8		2.3	3.8	mA
	Positive Negative			-4.3	-5.8		-4.3	-5.8		-4.3	-5.8	
	Positive Negative		V _S = +5V, -15V, I _{REF} = 2.0mA		2.4	3.8		2.4	3.8		2.4	3.8
I ₊ I ₋	Positive Negative	V _S = +5V, -15V, I _{REF} = 2.0mA		-6.4	-7.8		-6.4	-7.8		-6.4	-7.8	
	Positive Negative	V _S = ±15V, I _{REF} = 2.0mA		2.5	3.8		2.5	3.8		2.5	3.8	
	Positive Negative	V _S = ±15V, I _{REF} = 2.0mA		-6.5	-7.8		-6.5	-7.8		-6.5	-7.8	
P _D	Power dissipation	±5V, I _{REF} = 1.0mA		33	48		33	48		33	48	mW
		+5V, -15V, I _{REF} = 2.0mA		108	136		108	136		108	136	
		±15V, I _{REF} = 2.0mA		135	174		135	174		135	174	

NOTE *NE5007 must have a minimum reference current of .8µA.

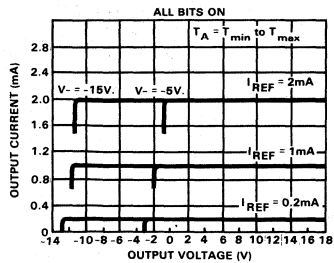


8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

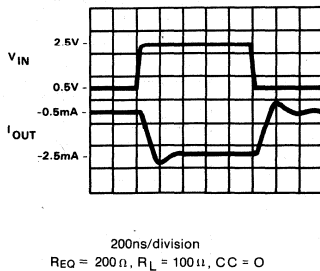
DAC-08 SERIES

TYPICAL PERFORMANCE CHARACTERISTICS

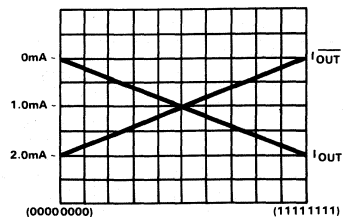
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



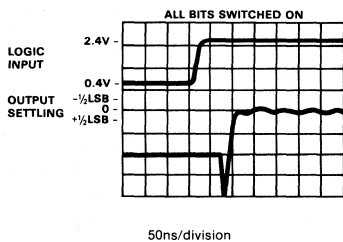
FAST PULSED REFERENCE OPERATION



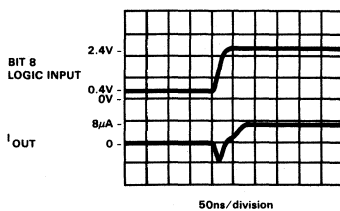
TRUE AND COMPLEMENTARY OUTPUT OPERATION



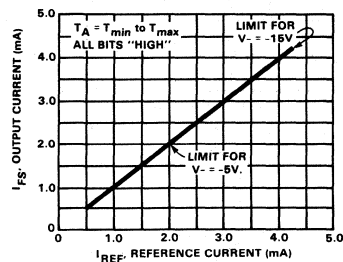
FULL SCALE SETTLING TIME



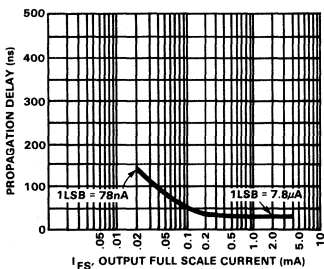
LSB SWITCHING



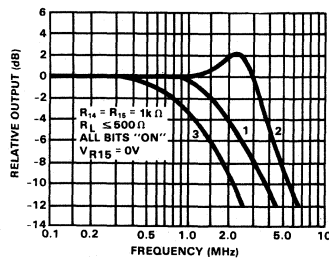
FULL SCALE CURRENT vs REFERENCE CURRENT



LSB PROPAGATION DELAY vs IFS



REFERENCE INPUT FREQUENCY RESPONSE



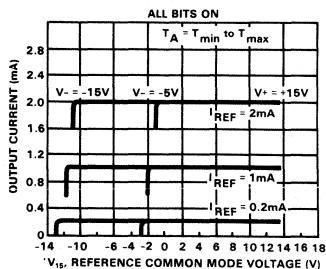
Curve 1: $CC = 15\text{pF}$, $V_{IN} = 2.0\text{V}$ p-p centered at +1.0V.
 Curve 2: $CC = 15\text{pF}$, $V_{IN} = 50\text{mV}$ p-p centered at +200mV.
 Curve 3: $CC = 0\text{pF}$, $V_{IN} = 100\text{mV}$ p-p centered at 0V and applied thru 50Ω connected to pin 14. +2.0V applied to R_{14} .

8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

DAC-08 SERIES

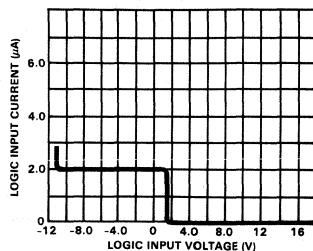
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

REFERENCE AMP COMMON MODE RANGE

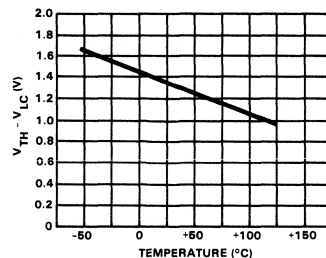


Positive common mode range is always (V+) - 1.5V

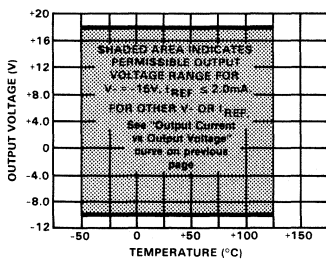
LOGIC INPUT CURRENT vs INPUT VOLTAGE



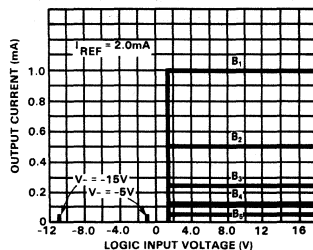
VTH - VLC vs TEMPERATURE



OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



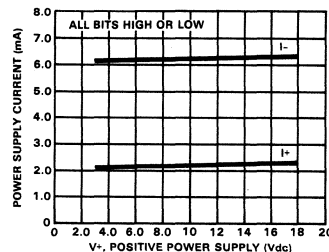
BIT TRANSFER CHARACTERISTICS



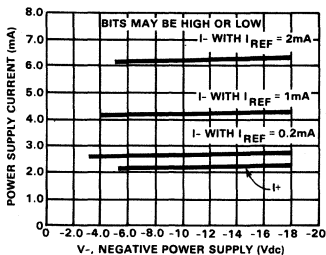
NOTE

B₁ through B₄ have identical transfer characteristics. Bits are fully switched, with less than 1/2 LSB error, at less than ±100mV from actual threshold. These switching points are guaranteed to lie between 0.8 and 2.0 volts over the operating temperature range (VLC = 0.0V).

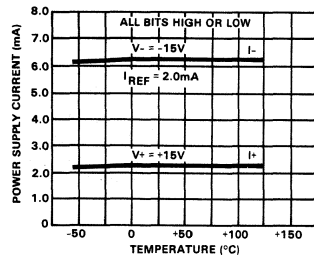
POWER SUPPLY CURRENT vs V+



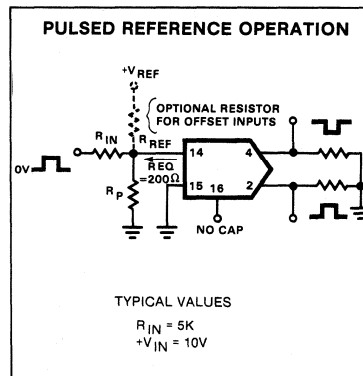
POWER SUPPLY CURRENT vs V-



POWER SUPPLY CURRENT vs TEMPERATURE



TYPICAL APPLICATION

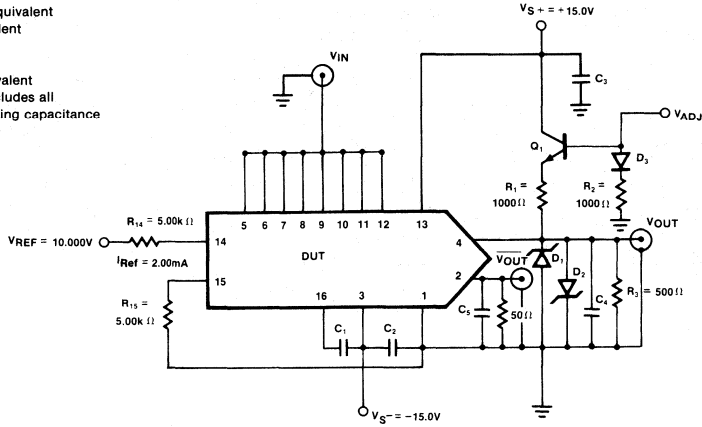


8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

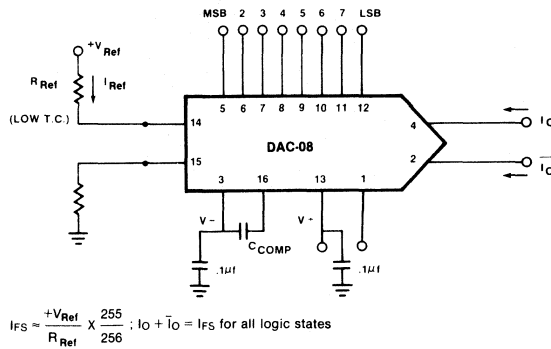
DAC-08 SERIES

SETTLING TIME AND PROPAGATION DELAY

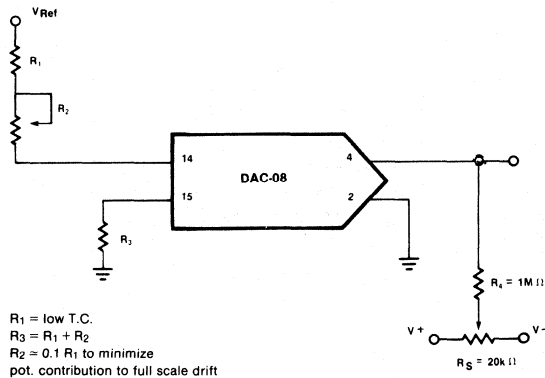
- D₁, D₂ = IN6263 or equivalent
- D₃ = IN914 or equivalent
- C₁ = 0.01 μf
- C₂, C₃ = 0.1 μf
- Q₁ = 2N3904 or equivalent
- C₄, C₅ = 15pf and includes all probe and fixturing capacitance



BASIC 5008/5009 CONFIGURATION



RECOMMENDED FULL SCALE AND ZERO SCALE ADJ.

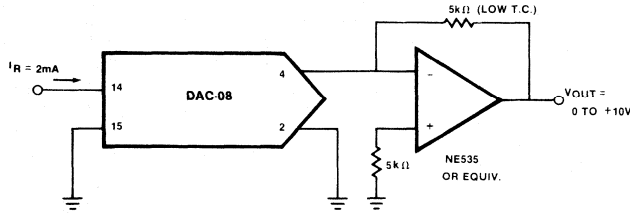


R₁ = low T.C.
 R₃ = R₁ + R₂
 R₂ = 0.1 R₁ to minimize pot. contribution to full scale drift

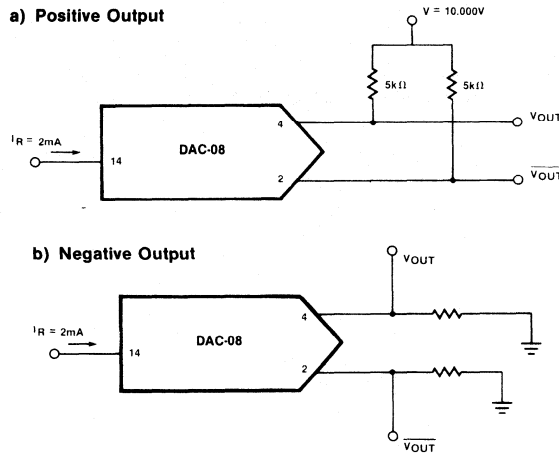
8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

DAC-08 SERIES

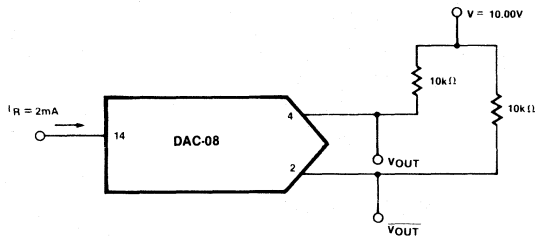
UNIPOLAR VOLTAGE OUTPUT FOR LOW IMPEDANCE OUTPUT



UNIPOLAR VOLT OUTPUT FOR HIGH IMPEDANCE OUTPUT



BASIC BIPOLAR OUTPUT OPERATION (OFFSET BINARY)



CODE CHART

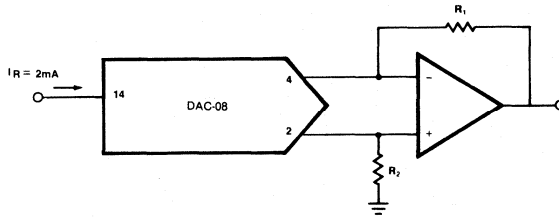
	B ₁	B ₂	B ₃	B ₄	B ₅	B ₆	B ₇	B ₈	V _{OUT}	$\overline{V_{OUT}}$
POS full scale	1	1	1	1	1	1	1	1	-9.920V	+10.000
POS f.s. - 1LSB	1	1	1	1	1	1	1	0	-9.840V	+9.920
+ Zero scale + 1LSB	1	0	0	0	0	0	0	1	-0.080V	+0.160
Zero scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero scale - 1LSB	0	1	1	1	1	1	1	1	0.080	0.000
Neg full scale - 1LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg full scale	0	0	0	0	0	0	0	0	+10.000	-9.920

11

8-BIT HIGH SPEED MULTIPLYING D/A CONVERTER

DAC-08 SERIES

SYMMETRICAL OFFSET BINARY (BIPOLAR)



$V_{OUT} = 0 \text{ to } \pm V^*$

$\pm V^*$ Range:
 $\pm 5V$ for $R_1 = R_2 = 2.5K$
 $\pm 10V$ for $R_1 = R_2 = 5.0K$

3 DIGIT BCD CONVERTER

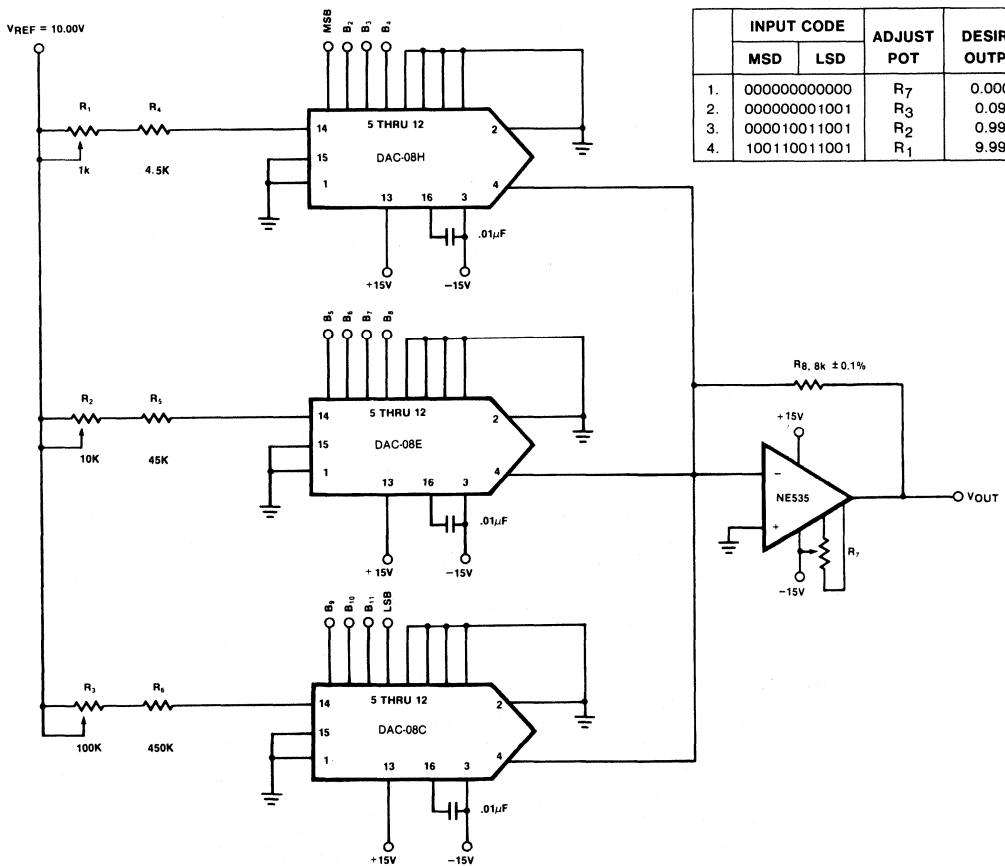
A 3 digit BCD converter, using inexpensive 8-bit binary DACs, can achieve $\pm 0.1\%$ accuracy. The circuit shown in Figure 20 utilizes three DACs, one for each decade, to provide 0 to 999 output steps. DAC 1 contains the first four significant digits controlling the hundreds digit; DAC 2 controls the tens digit and DAC 3 steps 0 to 9. The feedback resistor (R_7) sets the zero scale at 0.00V.

The input coding is the popular 8-4-2-1 coding; i.e. the weighting ratios are 8, 4, 2 and 1. The full scale (999) BCD code is input code 100110011001.

Full scale adjustment procedure.

In the sequence below, switch on the following code combinations and adjust the indicated potentiometer for the proper output.

3 DIGIT BCD CONVERTER WITH $\pm 0.1\%$ ACCURACY



	INPUT CODE		ADJUST POT	DESIRED OUTPUT
	MSD	LSD		
1.	000000000000	0000	R_7	0.000V
2.	000000001001	1001	R_3	0.09V
3.	000010011001	1001	R_2	0.99V
4.	100110011001	1001	R_1	9.99V

8-BIT MULTIPLYING D/A CONVERTER

MC1508-8/1408-8/1408-7

DESCRIPTION

The MC1508/MC1408 series of 8-bit monolithic digital-to-analog converters provide high speed performance with low cost. They are designed for use where the output current is a linear product of an 8-bit digital word and an analog reference voltage.

FEATURES

- Fast settling time—70ns (typ)
- Relative accuracy ±0.19% (max error)
- Non-inverting digital inputs are TTL and CMOS compatible
- High speed multiplying rate 4.0mA/μs (input slew)
- Output voltage swing +.5V to -5.0V
- Standard supply voltages + 5.0V and -5.0V to -15V
- Military qualifications pending

APPLICATIONS

- Tracking A-to-D converters
- 2½-digit panel meters and DVM's
- Waveform synthesis
- Sample and hold
- Peak detector
- Programmable gain and attenuation
- CRT character generation
- Audio digitizing and decoding
- Programmable power supplies
- Analog-digital multiplication
- Digital-digital multiplication
- Analog-digital division
- Digital addition and subtraction
- Speech compression and expansion
- Stepping motor drive

CIRCUIT DESCRIPTION

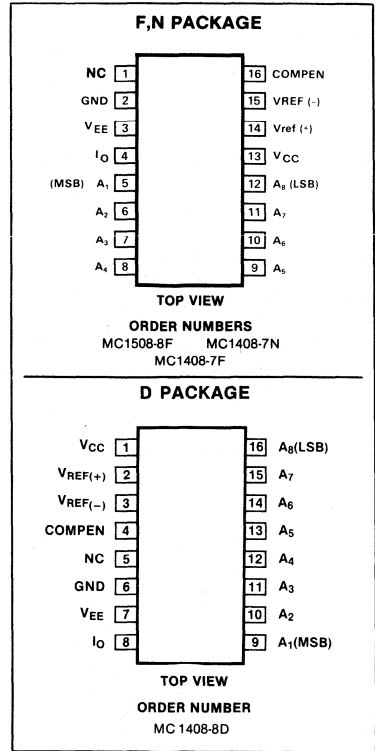
The MC1508/MC1408 consists of a reference current amplifier, and R-2R ladder, and 8 high speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are non-inverting in operation; therefore, a high state on the input turns on the specified output current component.

The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are tied to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992mA for a 2.0mA reference amplifier current if the NPN current source pair is perfectly matched.

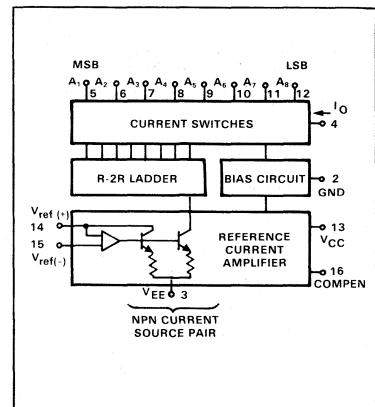
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS TA = +25°C unless otherwise specified

PARAMETER	RATING	UNIT
VCC	Power supply voltage	
V _{EE}	Positive	+5.5
V _{5-V12}	Negative	-16.5
V _O	Digital input voltage	+5.5, 0
I ₁₄	Applied output voltage	+0.5, -5.2
V _{14,V15}	Reference current	5.0
	Reference amplifier inputs	VCC, VEE
P _D	Power dissipation (package limitation)	
	Ceramic package	1000
	Plastic package	800
T _A	Operating temperature range	
	MC1508	-55 to +125
	MC1408	0 to +75
T _{stg}	Storage temperature range	-65 to +70

BLOCK DIAGRAM



8-BIT MULTIPLYING D/A CONVERTER

MC1508-8/1408-8/1408-7

Pin 3 must be 3V more negative than the potential to which R₁₅ is returned.

DC ELECTRICAL CHARACTERISTICS¹ V_{CC} = +5.0Vdc, V_{EE} = -15Vdc, $\frac{V_{ref}}{R_{14}} = 2.0\text{mA}$
 unless otherwise specified.

MC1508: T_A = -55°C to 125°C. MC1408: T_A = 0°C to 75°C

PARAMETER	TEST CONDITIONS	MC1508-8			MC1408-8			MC1408-7			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
E _r	Relative accuracy	Error relative to full scale I _o , Figure 3			±0.19			±0.19			%
t _s	Setting time ¹	To within 1/2 LSB, includes t _{PLH} , T _A = +25°C, Figure 4			70			70			ns
t _{PLH} t _{PHL}	Propagation delay time Low-to-high High-to-low	T _A = +25°C, Figure 4			30 100			30 100			ns
TC _{IO}	Output full scale current drift	-20			-20			-20			PPM/°C
V _{IH} V _{IL}	Digital input logic level (MSB) High Low	Figure 5			2.0 0.8			2.0 0.8			Vdc
I _{IH} I _{IL}	Digital input current (MSB) High Low	Figure 5			0 -0.4			0 -0.4			mA
I ₁₅	Reference input bias current	Pin 15, Figure 5			-1.0 -5.0			-1.0 -5.0			μA
I _{OR}	Output current range	Figure 5			0 2.0			2.1 4.2			mA
I _O	Output current	Figure 5			1.9 1.99			2.1 1.99			mA
I _{O(min)}	Off-state	V _{ref} = 2.000V, R ₁₄ = 1000Ω			0 4.0			0 4.0			μA
V _O	Output voltage compliance	All bits low			-0.55, +0.5 -5.0, +0.5			-0.55, +0.5 -5.0, +0.5			Vdc
SRI _{ref}	Reference current slew rate	Figure 6			4.0			4.0			mA/μs
PSRR ₍₋₎	Output current power supply sensitivity	I _{ref} = 1mA			0.5 2.7			0.5 2.7			μA/V
I _{CC} I _{EE}	Power supply current Positive Negative	All bits low, Figure 5			+13.5 -7.5			+22 -13			mA
V _{CCR} V _{VEER}	Power supply voltage range Positive Negative	T _A = +25°C, Figure 5			+4.5 -4.5			+5.0 -15			Vdc
P _D	Power dissipation	All bits low, Figure 5			105 190			170 305			mW
		All bits high, Figure 5			90 160			90 160			

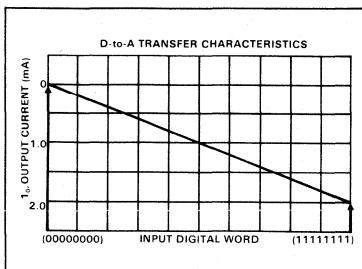
NOTES

1. All bits switched

8-BIT MULTIPLYING D/A CONVERTER

MC1508-8/1408-8/1408-7

TYPICAL PERFORMANCE CHARACTERISTICS



FUNCTIONAL DESCRIPTION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current (I_{14}) must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 1. The reference voltage source supplies the full current I_{14} . For bipolar reference signals, as in the multiplying mode, R_{15} can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R_{15} with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R_{14} to maintain proper phase margin; for R_{14} values of 1.0, 2.5 and 5.0k Ω , minimum capacitor values are 15, 37, and 75pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R_{14} is grounded and the reference voltage is applied to R_{15} as shown in Figure 2. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0V above the V_{EE} supply. Bipolar input signals may be handled by connecting R_{14} to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply which drives logic is to be used as the reference, R_{14} should be decoupled

by connecting it to +5.0V through another resistor and bypassing the junction of the 2 resistors with 0.1 μ F to ground. For reference voltages greater than 5.0V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.55 to +0.5V at +25°C, due to the current switching methods employed in the MC1508/MC1408. When a current switch is turned off, the positive voltage on the output terminal can turn on the output diode and increase the output current level. When a current switch is turned on, the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is 1 diode voltage below ground when pin 1 is grounded, so a negative voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1508/MC1408 may be extended to -5.0V by opening the circuit at pin 1. The negative supply voltage must be more negative than -10V. Using a full scale current of 1.992mA and load resistor of 2.5k Ω between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 Ω do not significantly affect performance, but 2.5k Ω load increases worst case settling time to 1.2 μ s (when all bits are switched on). Refer to the subsequent text section on settling time for more details on output loading.

If a power supply value between -5.0V and -10V is desired, a voltage of between 0 and -5.0V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2mA may be used only for negative supply voltages more negative than -7.0V, due to the increased voltage drop across the resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each

output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1508/MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1508/MC1408 has a very low full scale current drift with temperature.

The MC1508/ \pm MC1408 series is guaranteed accurate to within $\pm 1/2$ LSB at +25°C at a full scale output current of 1.992mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0mA, with the loss of 1 LSB = 8.0 μ A which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 3. The 12-bit converter is calibrated for a full scale output current of 1.992mA. This is an optional step since the MC1508/MC1408 accuracy is essentially the same between 1.5 and 2.5mA. Then the MC1508/MC1408 circuits' full scale current is trimmed to the same value with R_{14} so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. Sixteen-bit accuracy implies a total error $\pm 1/2$ of 1 part in 65,536, or $\pm 0.00076\%$, which is much more accurate than the $\pm 0.19\%$ specification provided by the MC1508/MC1408.

Multiplying Accuracy

The MC1508/MC1408 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under worst case conditions, these 8 amplifiers can contribute a total of 1.6 μ A extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μ A to 4.0mA, the 1.6 μ A contributes an error of 0.1 LSB. This is well within 8-bit accuracy.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1508/MC1408 is monotonic for all values of reference current above 0.5mA. The

8-BIT MULTIPLYING D/A CONVERTER

MC1508-8/1408-8/1408-7

recommended range for operation with a dc reference current is 0.5 to 4.0mA.

Settling Time

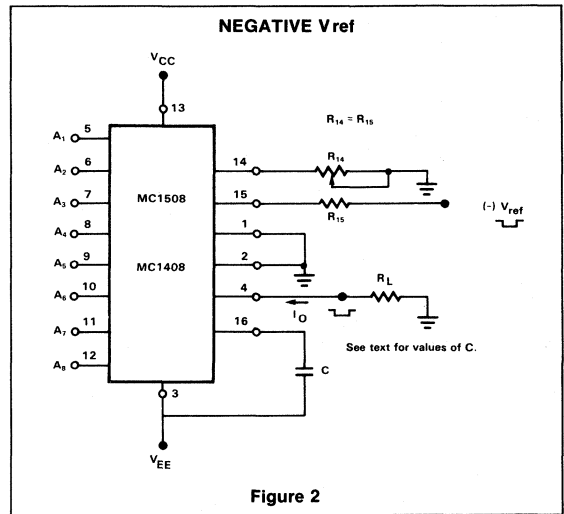
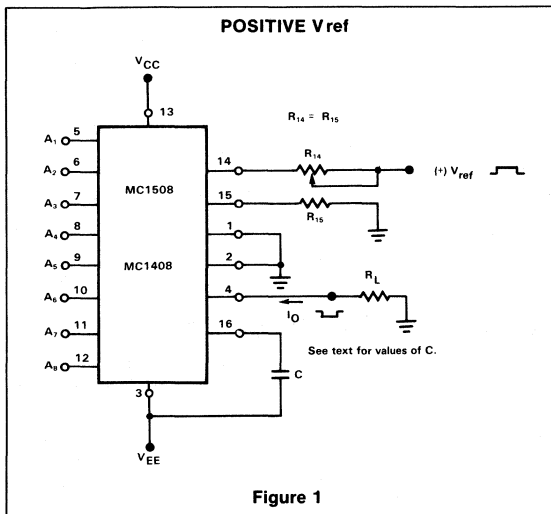
The worst case switching condition occurs when all bits are switched on, which corresponds to a low-to-high transition for all bits. This time is typically 70ns for settling to within $\pm 1/2$ LSB for 8-bit accuracy and 200ns to $1/2$ LSB for 7-bit accuracy. The turnoff is typically under 100ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25pF$.

The slowest single switch is the least significant bit, which turns on and settles in 65ns and turns off in 80ns. In applications where the D-to-A converter functions in a positive going ramp mode, the worst case switching condition does not occur, and a settling time of less than 70ns may be realized. Bit A7 turns on in 50ns and off in 35ns, while bit A6 turns on in 60ns and off in 80ns.

The test circuit of Figure 4 requires a smaller voltage swing for the current switches due

to internal voltage clamping in MC1508/MC1408. A $1.0k\Omega$ load resistor from pin 4 to ground gives a typical settling time of 400ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications. Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, $100\mu F$ supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

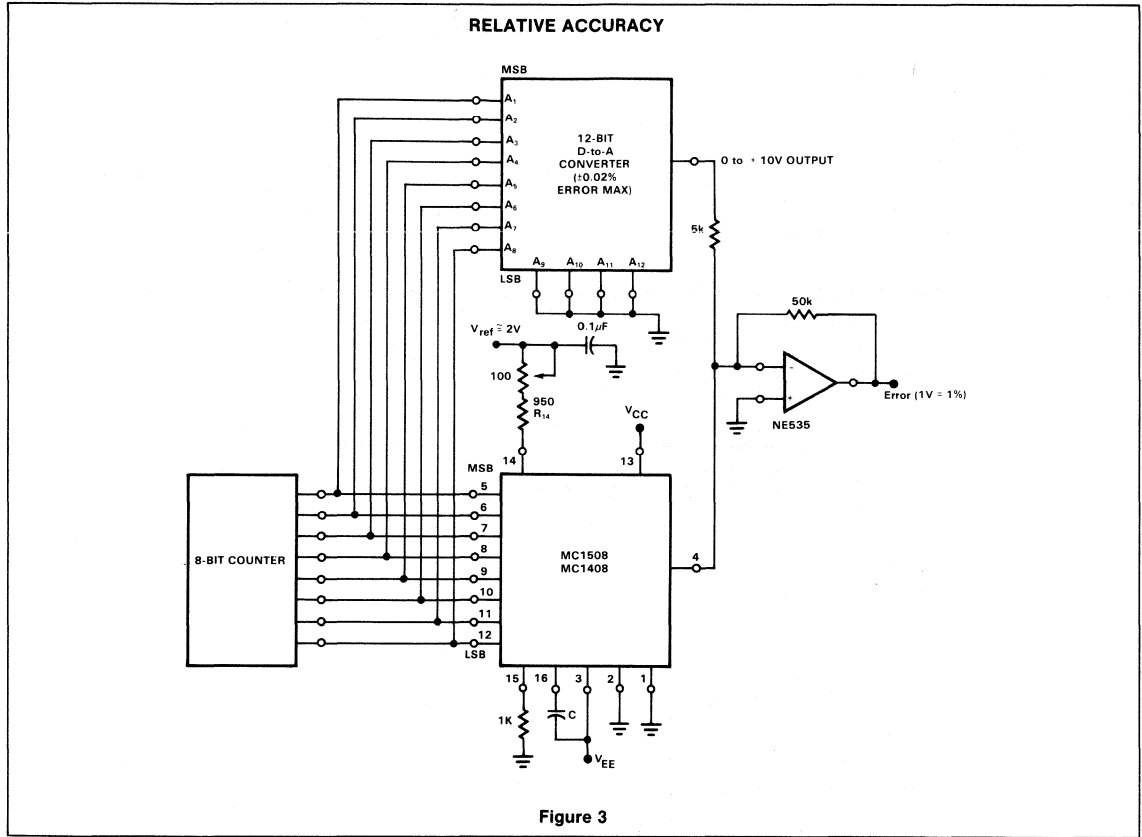
TEST CIRCUITS



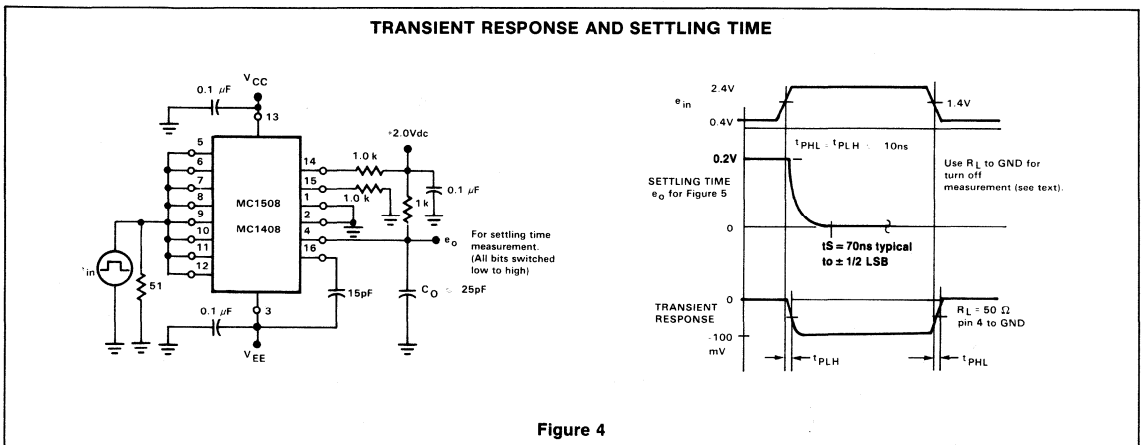
8-BIT MULTIPLYING D/A CONVERTER

MC1508-8/1408-8/1408-7

TEST CIRCUITS (Cont'd)



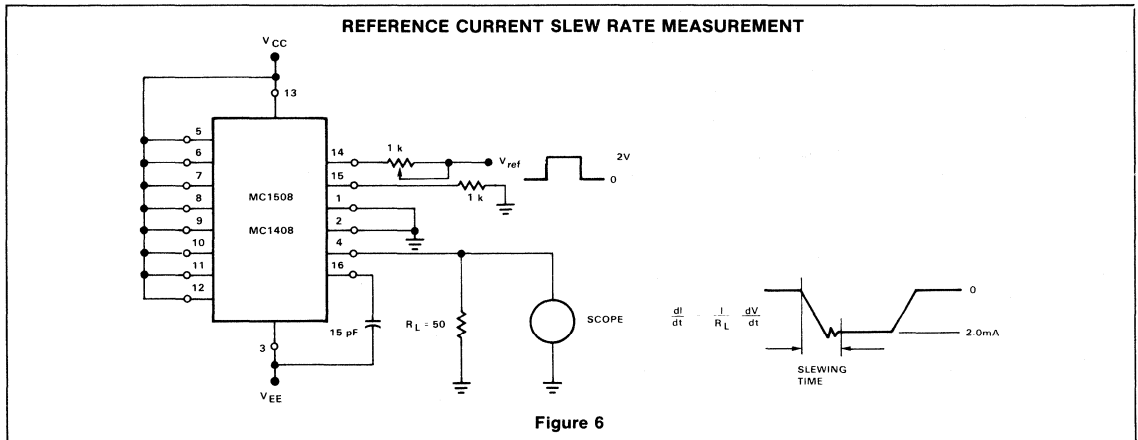
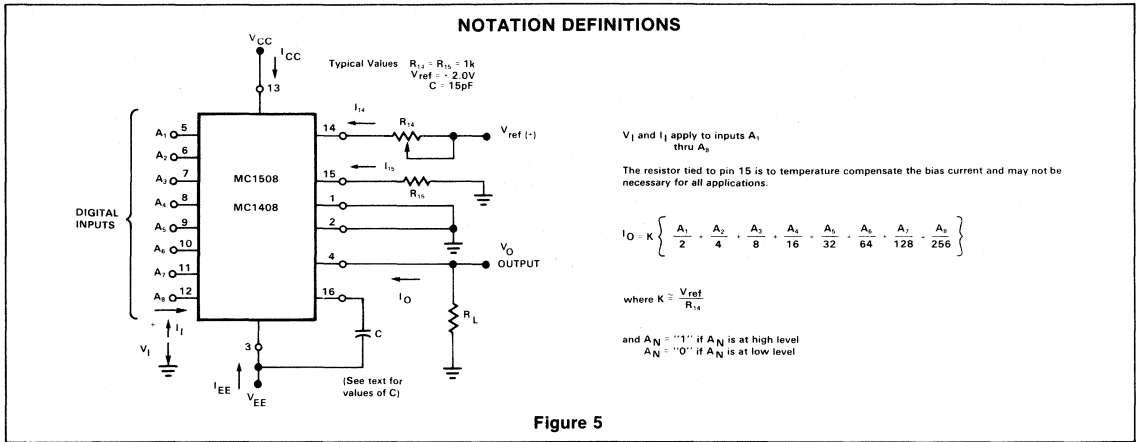
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8-BIT MULTIPLYING D/A CONVERTER

MC1508-8/1408-8/1408-7

TEST CIRCUITS (Cont'd)



8-BIT μ P-COMPATIBLE D/A CONVERTER

SE/NE5018

DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the \overline{LE} input is in the low state. When \overline{LE} goes high, the input data present at the moment of transition is latched and retained until \overline{LE} again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

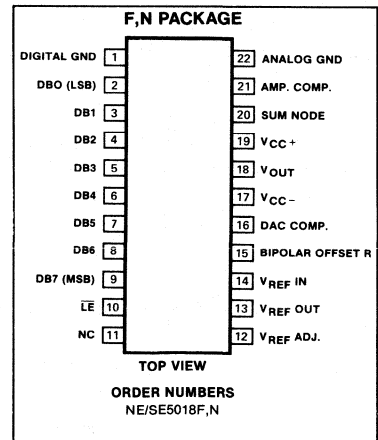
FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to $\pm 1/2$ LSB (.19%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 8085, 6800 and many other μ P's

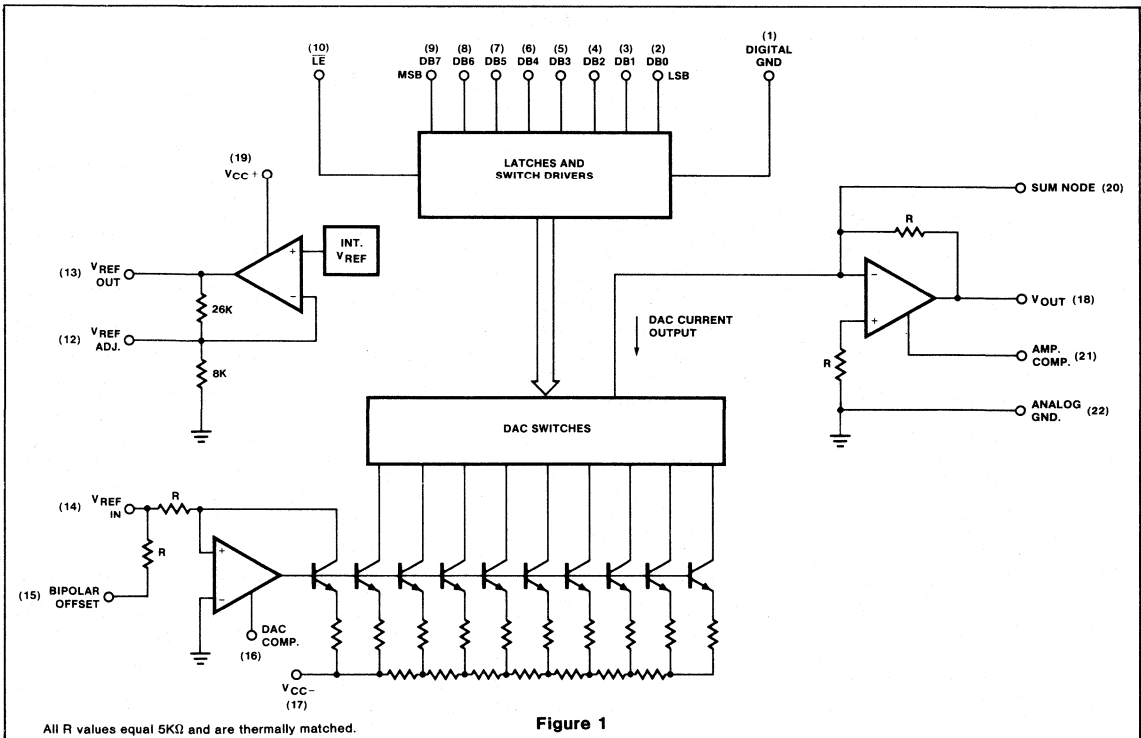
APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

PIN CONFIGURATION



BLOCK DIAGRAM



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8-BIT μ P-COMPATIBLE D/A CONVERTER

SE/NE5018

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC+}	Positive supply voltage	18	V
V _{CC-}	Negative supply voltage	-18	V
V _{IN}	Logic input voltage	0 to 18	V
V _{REFIN}	Voltage at V _{REF} input	12	V
V _{REFADJ}	Voltage at V _{REF} adjust	0 to V _{REF}	V
V _{SUM}	Voltage at sum node	12	V
I _{REFSC}	Short-circuit current to ground at V _{REF} OUT	Continuous	
I _{OUTSC}	Short-circuit current to ground or either supply at V _{OUT}	Continuous	
P _D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T _A	Operating temperature range		
	SE5018	-55 to +125	°C
	NE5018	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

V_{CC+} = +15V, V_{CC-} = -15V, SE5018. -55°C ≤ T_A ≤ 125°C,NE5018. 0°C ≤ T_A ≤ 70°C unless otherwise specified!

Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE5018			NE5018			UNIT
		Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Relative accuracy				±0.19			±0.19	%FS
V _{CC+}	Positive supply voltage	11.4	15		11.4	15		V
V _{CC-}	Negative supply voltage	-11.4	-15		-11.4	-15		V
V _{IN(1)}	Logic "1" input voltage	2.0			2.0			V
V _{IN(0)}	Logic "0" input voltage			0.8			0.8	V
I _{IN(1)}	Logic "1" input current		0.1	10		0.1	10	μA
I _{IN(0)}	Logic "0" input current		-2.0	-10		-2.0	-10	μA
V _{FS}	Full scale output voltage	9.50	9.961	10.50	9.50	9.961	10.50	V
V _{FS}	Full scale output voltage	4.5	+4.961	5.5	4.5	+4.961	5.5	V
V _{ZS}	Zero scale voltage	-5.04	-5.000	-4.960	5.04	-5.000	4.960	mV
		-30	5	+30	-30	5	+30	
I _{OS}	Output short circuit current		15	40		15	40	mA
PSR ⁺ (out)	Output power supply rejection (+)		.001	.01		.001	.01	%FS/ %VS
PSR ⁻ (out)	Output power supply rejection (-)		.001	.01		.001	.01	%FS/ %VS
TC _{FS}	Full scale temperature coefficient		20			20		ppm/°C
TC _{ZS}	Zero scale temperature coefficient		5			5		ppm/°C

8-BIT μ P-COMPATIBLE D/A CONVERTER

SE/NE5018

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC+} = +15V$, $V_{CC-} = -15V$, SE5018. $-55^{\circ}C \leq T_A \leq 125^{\circ}C$, NE5018. $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified.¹
 Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE/5018			NE5018			UNIT			
		Min	Typ	Max	Min	Typ	Max				
I_{REF}	Reference output current	Note 8 $T_A = 25^{\circ}C$ $V_{REF OUT} = 0V$						3	mA		
I_{REFSC}	Reference short circuit current							15	30	mA	
$PSR^{+}(REF)$	Reference power supply rejection (+)	$V^- = -15V, 13.5V \leq V^+ \leq 16.5V$, $I_{REF} = 1.0mA$.003	.01	%VR/ %VS	
$PSR^{-}(REF)$	Reference power supply rejection (-)	$V^+ = 15V, -13.5V \leq V^- \leq 16.5V$.003	.01	%VR/ %VS	
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$ $T_A = 25^{\circ}C$						4.9	5.0	5.25	V
TC_{REF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$ $T_A = 25^{\circ}C$							60		ppm/ $^{\circ}C$
Z_{IN}	DAC V_{REF} IN input impedance	$I_{REF} = 1.0mA$ $T_A = 25^{\circ}C$						4.15	5.0	5.85	K Ω
I_{CC+}	Positive supply current	$V_{CC+} = 15V$						7	14		mA
I_{CC-}	Negative supply current	$V_{CC-} = -15V$						-10	-15		mA
P_D	Power dissipation	$I_{REF} = 1.0mA, V_{CC} = \pm 15V$						255	435		mW

NOTE

1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS² $V_{CC} = \pm 15V, T_A = 25^{\circ}C$

PARAMETER	TO	FROM	TEST CONDITIONS	SE/NE5018			UNIT
				Min	Typ	Max	
T_{SLH}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits low to high ³			μs
T_{SHL}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits high to low ⁴			μs
t_{plh}	Propagation delay	Output	Input	All bits switched low to high ³			300
t_{phl}	Propagation delay	Output	Input	All bits switched high to low ⁴			150
t_{plsb}	Propagation delay	Output	Input	1 LSB change ^{3,4}			150
t_{plh}	Propagation delay	Output	\overline{LE}	low to high transition ⁵			300
t_{phl}	Propagation delay	Output	\overline{LE}	high to low transition ⁶			150
t_s	Set-up time	\overline{LE}	Input	2, 7			100
t_h	Hold time	Input	\overline{LE}	2, 7			50
t_{pw}	Latch enable pulse width			2, 7			150

NOTES

2. Refer to Figure 3.

3. See Figure 6.

4. See Figure 7.

5. See Figure 8.

6. See Figure 9.

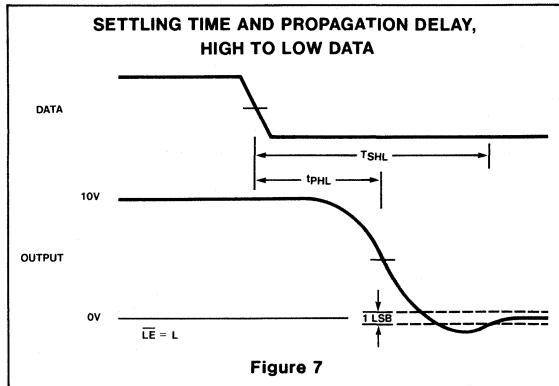
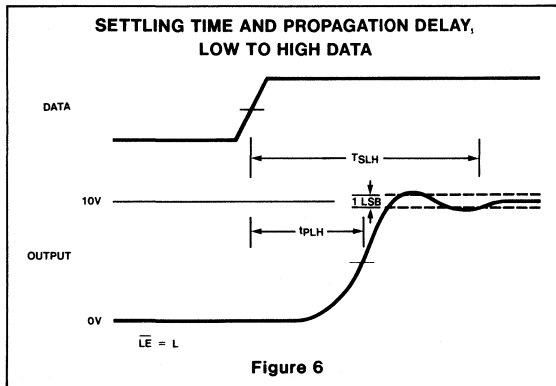
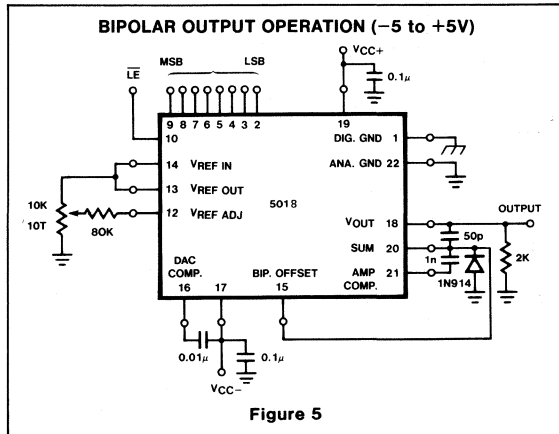
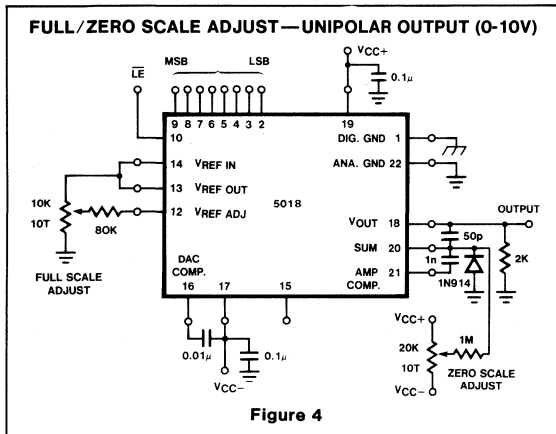
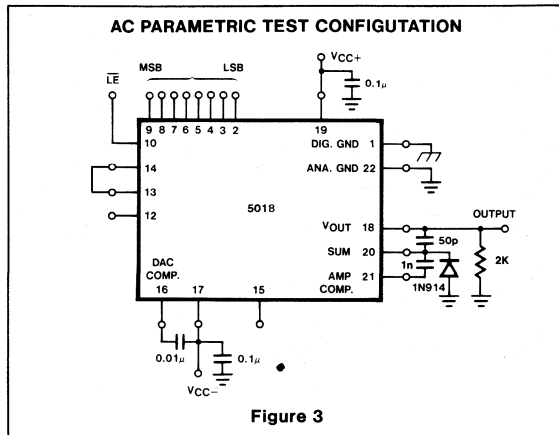
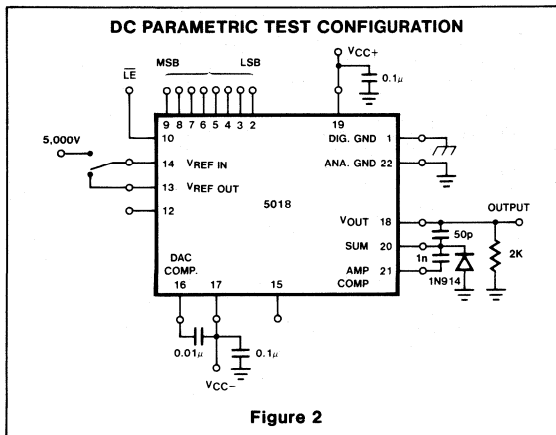
7. See Figure 10.

8. For reference currents > 3mA, use of an external buffer is required.

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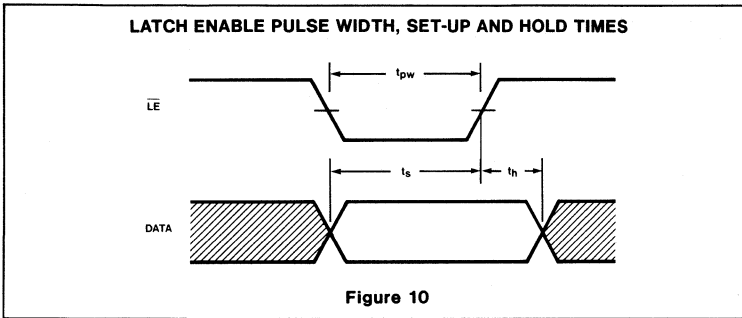
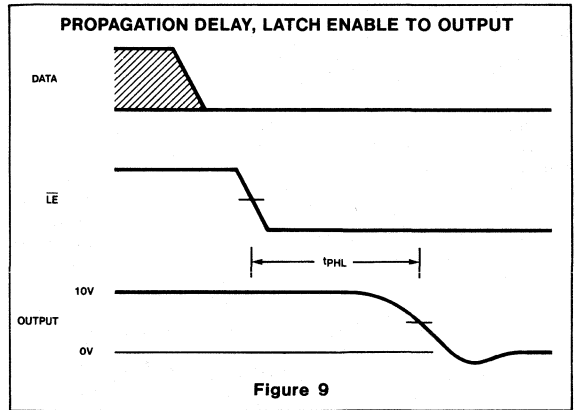
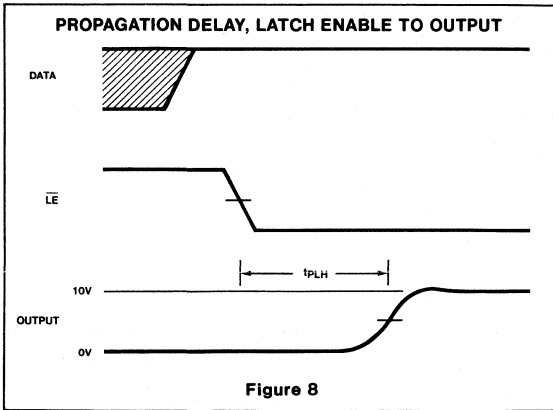
8-BIT μ P-COMPATIBLE D/A CONVERTER

SE/NE5018



8-BIT μ P-COMPATIBLE D/A CONVERTER

SE/NE5018



8-BIT μ P-COMPATIBLE D/A CONVERTER

SE/NE5019

DESCRIPTION

The NE5019 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the \overline{LE} input is in the low state. When \overline{LE} goes high, the input data present at the moment of transition is latched and retained until \overline{LE} again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

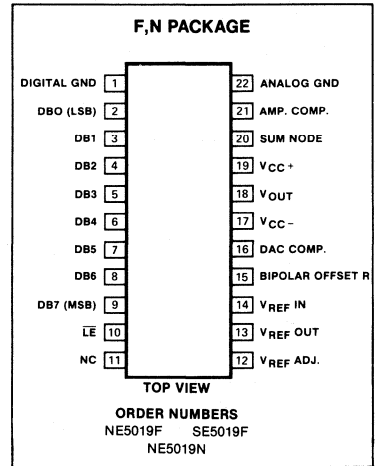
FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Output buffer amplifier
- Accurate to $\pm 1/4$ LSB (.1%)
- Monotonic to 8 bits
- Amplifier and reference both short-circuit protected
- Compatible with 8085, 6800 and many other μ P's

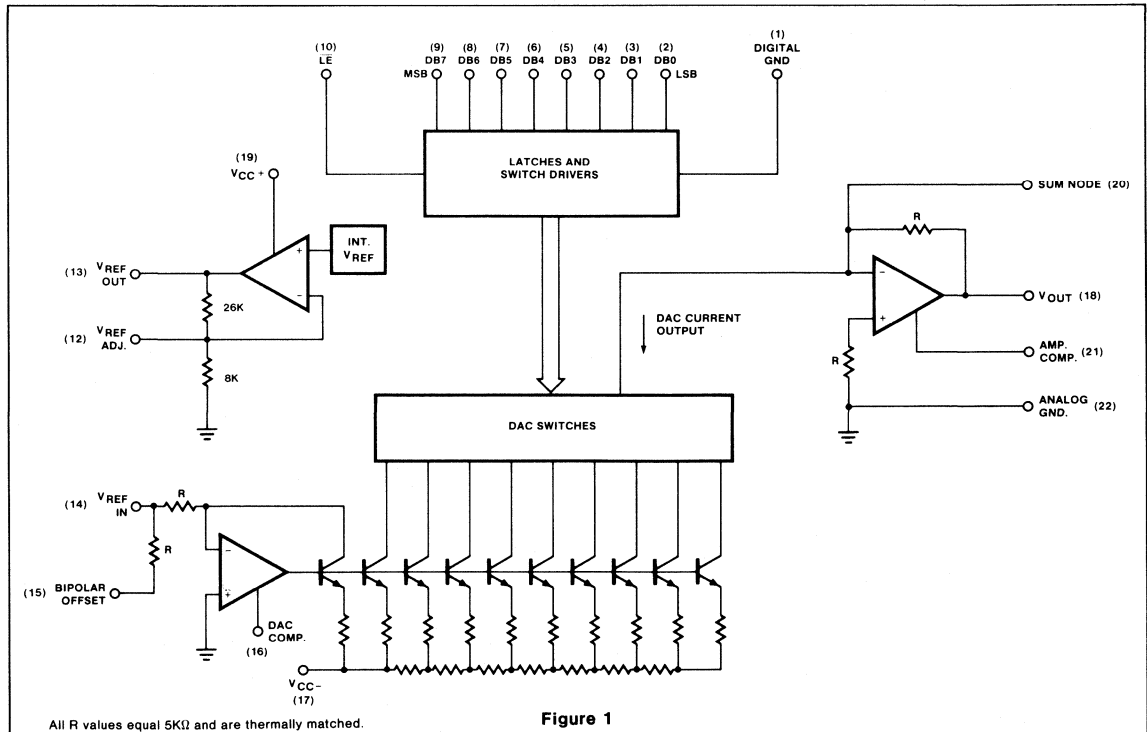
APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication

PIN CONFIGURATION



BLOCK DIAGRAM



8-BIT μ P-COMPATIBLE D/A CONVERTER

SE/NE5019

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC+}	Positive supply voltage	18	V
V _{CC-}	Negative supply voltage	-18	V
V _{IN}	Logic input voltage	0 to 18	V
V _{REFIN}	Voltage at V _{REF} input	12	V
V _{REFADJ}	Voltage at V _{REF} adjust	0 to V _{REF}	V
V _{SUM}	Voltage at sum node	12	V
I _{REFSC}	Short-circuit current to ground at V _{REF} OUT	Continuous	
I _{OUTSC}	Short-circuit current to ground or either supply at V _{OUT}	Continuous	
P _D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T _A	Operating temperature range		
	SE5019	-55 to +125	°C
	NE5019	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

V_{CC+} = +15V, V_{CC-} = -15V, SE5019. -55°C ≤ T_A ≤ 125°C,NE5019. 0°C ≤ T_A ≤ 70°C unless otherwise specified.†

†Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE5019			NE5019			UNIT
		Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Relative accuracy				±0.1			±0.1	%FS
V _{CC+}	Positive supply voltage	11.4	15		11.4	15		V
V _{CC-}	Negative supply voltage	-11.4	-15		-11.4	-15		V
V _{IN(1)}	Logic "1" input voltage	2.0			2.0			V
V _{IN(0)}	Logic "0" input voltage			0.8			0.8	V
I _{IN(1)}	Logic "1" input current		0.1	10		0.1	10	μA
I _{IN(0)}	Logic "0" input current		-2.0	-10		-2.0	-10	μA
V _{FS}	Full scale output voltage	9.50	9.961	10.50	9.50	9.961	10.50	V
V _{FS}	Full scale output voltage	4.5	+4.961	5.5	4.5	+4.961	5.5	V
V _{ZS}	Zero scale voltage	-5.040	-5.000	-4.960	-5.040	-5.000	-4.960	mV
I _{OS}	Output short circuit current		15	40		15	40	mA
PSR+(out)	Output power supply rejection (+)		.001	.01		.001	.01	%FS / %VS
PSR-(out)	Output power supply rejection (-)		.001	.01		.001	.01	%FS / %VS
TC _{FS}	Full scale temperature coefficient		20			20		ppm/°C
TC _{ZS}	Zero scale temperature coefficient		5			5		ppm/°C

NOTE

1. Refer to Figure 2.

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8-BIT μ P-COMPATIBLE D/A CONVERTER

SE/NE5019

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC+} = +15V$, $V_{CC-} = -15V$, SE5019. $-55^{\circ}C \leq T_A \leq 125^{\circ}C$,
NE5019. $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified.¹
Typical values are specified at $25^{\circ}C$

PARAMETER	TEST CONDITIONS	SE5019			NE5019			UNIT		
		Min	Typ	Max	Min	Typ	Max			
I_{REF}	Reference output current			3			3	mA		
I_{REFSC}	Reference short circuit current		15	30		15	30	mA		
PSR+REF	Reference power supply rejection (+)	V ₋ = -15V, 13.5V \leq V ₊ \leq 16.5V, $I_{REF} = 1.0mA$.003	.01		.003	.01	%VR/ %VS	
PSR-REF	Reference power supply rejection (-)	V ₊ = 15V, -13.5V \leq V ₋ \leq 16.5V,		.003	.01		.003	.01	%VR/ %VS	
V_{REF}	Reference voltage	$I_{REF} = 1.0mA$ $T_A = 25^{\circ}C$		4.9	5.0	5.25	4.9	5.0	5.25	V
T_{CREF}	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$ $T_A = 25^{\circ}C$			60			60	ppm/ $^{\circ}C$	
Z_{IN}	DAC V_{REFIN} input impedance	$I_{REF} = 1.0mA$ $T_A = 25^{\circ}C$		4.15	5.0	5.85	4.15	5.0	5.85	K Ω
I_{CC+}	Positive supply current	$V_{CC+} = 15V$			7	14		7	14	mA
I_{CC-}	Negative supply current	$V_{CC-} = -15V$			-10	-15		-10	-15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$			255	435		255	435	mW

NOTE

1. Refer to Figure 2.

AC ELECTRICAL CHARACTERISTICS² $V_{CC} = \pm 15V$, $T_A = 25^{\circ}C$

PARAMETER	TO	FROM	TEST CONDITIONS	SE/NE5019			UNIT
				Min	Typ	Max	
T_{SLH}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits low to high ³			μs
T_{SHL}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits high to low ⁴			μs
t_{pLH}	Propagation delay	Output	Input	All bits switched low to high ³			ns
t_{pHL}	Propagation delay	Output	Input	All bits switched high to low ⁴			ns
t_{pLSB}	Propagation delay	Output	Input	1 LSB change ^{3,4}			ns
t_{pLH}	Propagation delay	Output	\overline{LE}	low to high transition ⁵			ns
t_{pHL}	Propagation delay	Output	\overline{LE}	high to low transition ⁶			ns
t_s	Set-up time	\overline{LE}	Input	2, 7		100	ns
t_h	Hold time	Input	\overline{LE}	2, 7		50	ns
t_{pw}	Latch enable pulse width			2, 7		150	ns

NOTES

2. Refer to Figure 3.

3. See Figure 6.

4. See Figure 7.

5. See Figure 8.

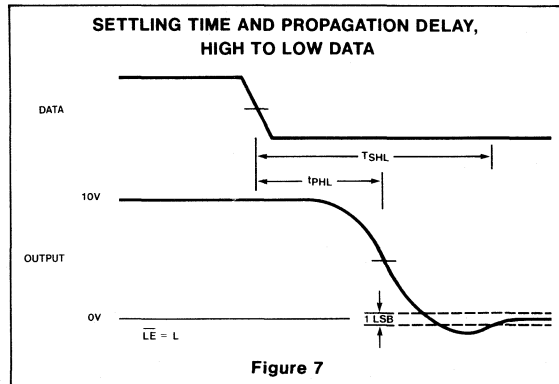
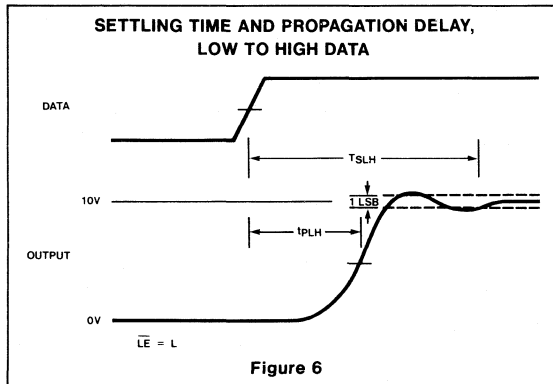
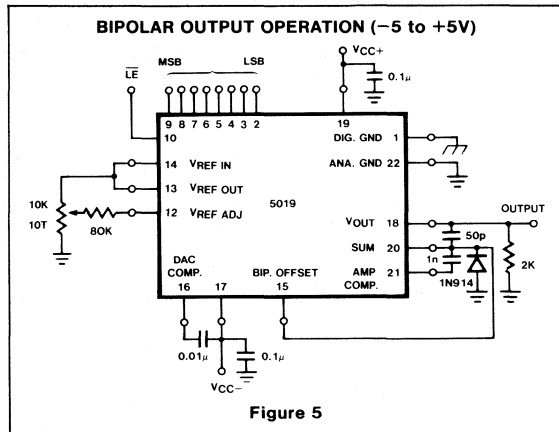
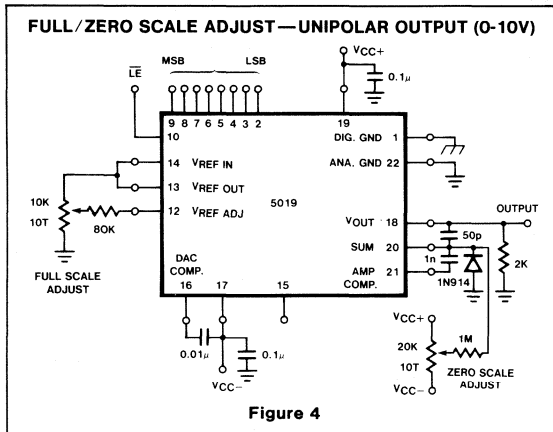
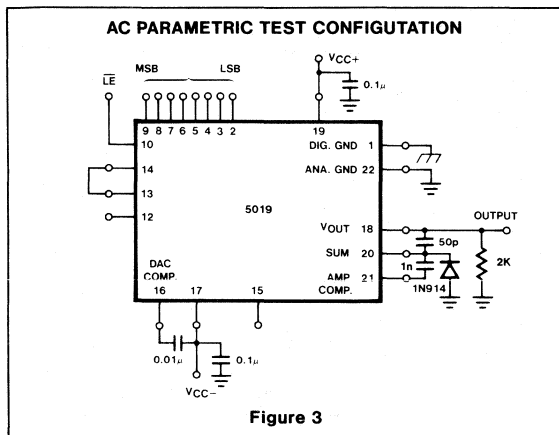
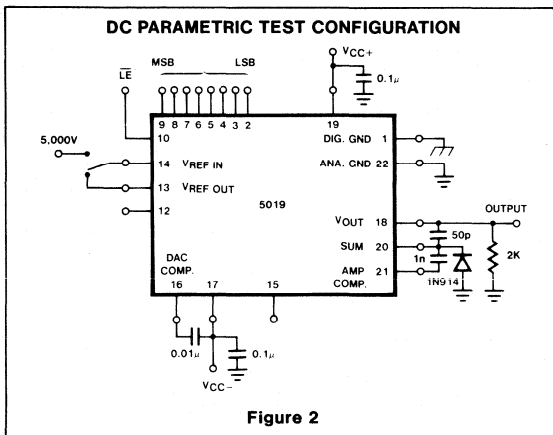
6. See Figure 9.

7. See Figure 10.

8. For reference currents $> 3mA$, use of an external buffer is required.

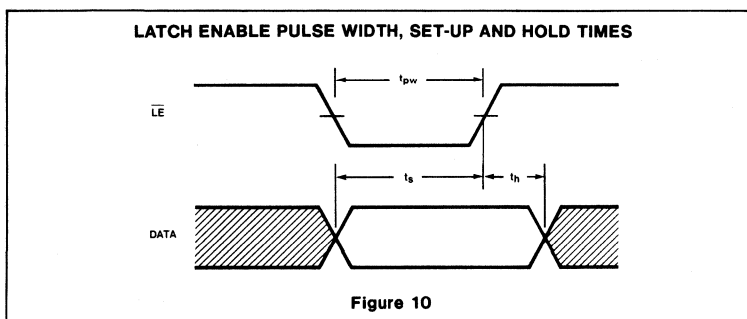
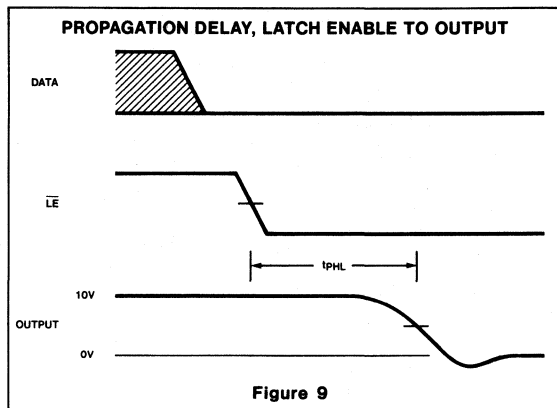
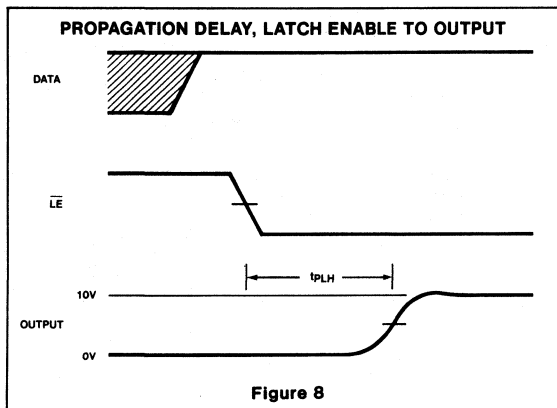
8-BIT μ P-COMPATIBLE D/A CONVERTER

SE/NE5019



8-BIT μ P-COMPATIBLE D/A CONVERTER

SE/NE5019



10-BIT μ P-COMPATIBLE D/A CONVERTER

NE5020

DESCRIPTION

The NE5020 is a microprocessor-compatible monolithic 10-bit digital to analog converter subsystem. This device offers 10-bit resolution and $\pm 0.1\%$ accuracy and monotonicity guaranteed over full operating temperature range.

Low loading latches, adjustable logic thresholds and addressing capability allow the NE5020 to directly interface with most microprocessor and logic controlled systems.

The NE5020 contains internal voltage reference, DAC switches and resistor ladder. Also, the input buffer and output summing amplifier are included. In addition, the matched application resistors for scaling either unipolar or bipolar output values are included on a single monolithic chip.

The result is a near minimum component count 10-bit resolution DAC system.

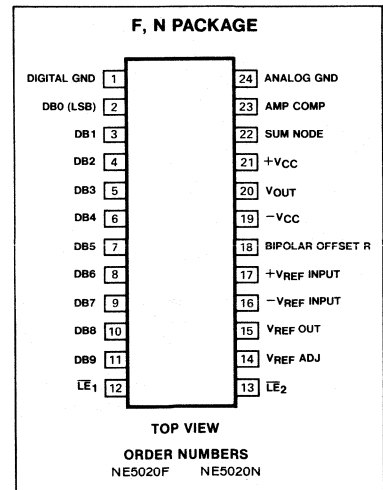
FEATURES

- 10-bit resolution
- Guaranteed monotonicity over operating range
- $\pm 0.1\%$ relative accuracy
- Unipolar (0V to +10V) and Bipolar ($\pm 5V$) output range
- Logic bus compatible
- 5 μ sec settling time

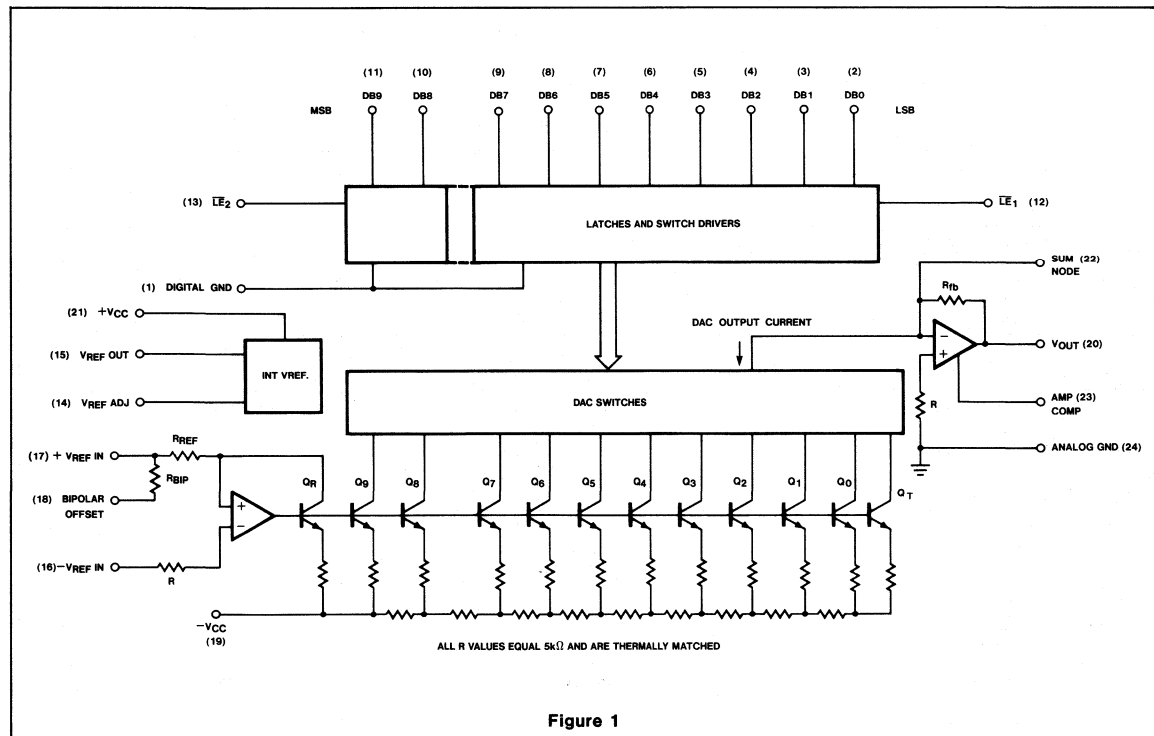
APPLICATIONS

- Precision 10-bit D/A converters
- 10-bit Analog to Digital converters
- Programmable power supplies
- Test equipment
- Measurement instruments

PIN CONFIGURATION



BLOCK DIAGRAM



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10-BIT μ P-COMPATIBLE D/A CONVERTER

NE5020

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC+}	Positive supply voltage	18	V
V _{CC-}	Negative supply voltage	-18	V
V _{IN}	Logic input voltage	0 to 18	V
V _{REF IN}	Voltage at +V _{REF} input	12	V
V _{REF ADJ}	Voltage at V _{REF} adjust	0 to V _{REF}	V
V _{SUM}	Voltage at sum node	12	V
I _{REFSC}	Short-circuit current to ground at V _{REF} OUT	Continuous	
I _{OUTSC}	Short-circuit current to ground or either supply at V _{OUT}	Continuous	
P _D	Power dissipation*		
	-N package	800	mW
	F package	1000	mW
T _A	Operating temperature range		
	NE5020	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS

V_{CC+} = +15V, V_{CC-} = -15V, 0°C ≤ T_A ≤ 70°C unless otherwise specified.¹
 Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	NE5020			UNIT	
		Min	Typ	Max		
Resolution				10	Bits	
Monotonicity				10	Bits	
Relative accuracy				±0.1	%FS	
V _{CC+}	Positive supply voltage	11.4	15	16.5	V	
V _{CC-}	Negative supply voltage	-11.4	-15	-16.5	V	
V _{IN(1)}	Logic "1" input voltage				V	
V _{IN(0)}	Logic "0" input voltage				V	
I _{IN(1)}	Logic "1" input current		0.1	10	μA	
I _{IN(0)}	Logic "0" input current		-2.0	-10	μA	
V _{FS}	Full scale output voltage		9.5	9.9902	10.5	V
V _{FS}	Full scale output voltage		4.5	4.9902	5.5	V
V _{ZS}	Zero scale voltage		-5.040	-5.000	-4.960	mV
I _{OS}	Output short circuit current			5	+30	mA
PSR+(out)	Output power supply rejection (+)			±15	±40	mA
PSR-(out)	Output power supply rejection (-)					mA
TC _{FS}	Full scale temperature coefficient					ppmFS / °C
TC _{ZS}	Zero scale temperature coefficient					ppmFS / °C

NOTE

1. Refer to Figure 2.

10-BIT μ P-COMPATIBLE D/A CONVERTER

NE5020

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC+} = +15V$, $V_{CC-} = -15V$, $0^\circ C \leq T_A \leq 70^\circ C$ unless otherwise specified.¹
Typical values are specified at $25^\circ C$

PARAMETER	TEST CONDITIONS	NE5020			UNIT
		Min	Typ	Max	
I_{REF}^2 $I_{REF\ SC}$	Reference output current Reference short circuit current $T_A = 25^\circ C$ $V_{REF\ OUT} = 0V$		15	3 30	mA mA
$PSR+_{REF}$ $PSR-_{REF}$	Reference power supply rejection (+) Reference power supply rejection (-) $V- = -15V, 13.5V \leq V+ \leq 16.5V$, $I_{REF} = 1.0mA$ $V+ = 15V, -13.5V \leq V- \leq 16.5V$,		.003 .003	.01 .01	%VR/ %VS %VR/ %VS
V_{REF} T_{CREF}	Reference voltage Reference voltage temperature coefficient $I_{REF} = 1.0mA, T_A = 25^\circ C$ $I_{REF} = 1.0mA$	4.9	5.0 60	5.25	V ppm/ $^\circ C$
Z_{IN}	DAC V_{REFIN} input impedance $I_{REF} = 1.0mA$		5.0		k Ω
I_{CC+} I_{CC-}	Positive supply current Negative supply current $V_{CC+} = 15V$ $V_{CC-} = -15V$		7 -10	14 -15	mA mA
P_D	Power dissipation $I_{REF} = 1.0mA, V_{CC} = \pm 15V$		255	435	mW

NOTE

1. Refer to Figure 2.
2. For $I_{REF\ OUT}$ greater than 3mA, an external buffer is required.

AC ELECTRICAL CHARACTERISTICS³ $V_{CC} = \pm 15V$, $T_A = 25^\circ C$

PARAMETER	TO	FROM	TEST CONDITIONS	NE5020			UNIT
				Min	Typ	Max	
T_{SLH} T_{SHL}	$\pm \frac{1}{2}$ LSB $\pm \frac{1}{2}$ LSB	Input Input	All bits low to high ⁴ All bits high to low ⁵		5 5		μs μs
t_{plh} t_{phl}	Output Output	Input Input	All bits switched low to high ⁴ All bits switched high to low ⁵		300 150		ns ns
t_{plsb} t_{plh}	Output Output	Input \overline{LE}	1 LSB change ^{4,5} low to high transition ⁶		150 300		ns ns
t_{phl}	Output	\overline{LE}	high to low transition ⁷		150		ns
t_s	\overline{LE}	Input	3, 8	100			ns
t_h	Input	\overline{LE}	3, 8	50			ns
t_{pw}			3, 8	150			ns

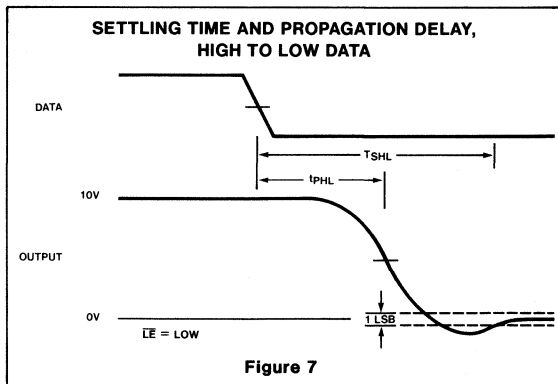
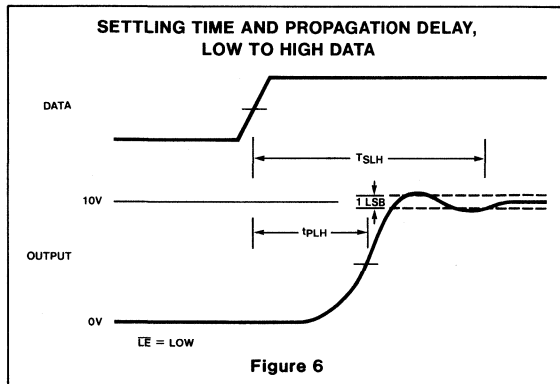
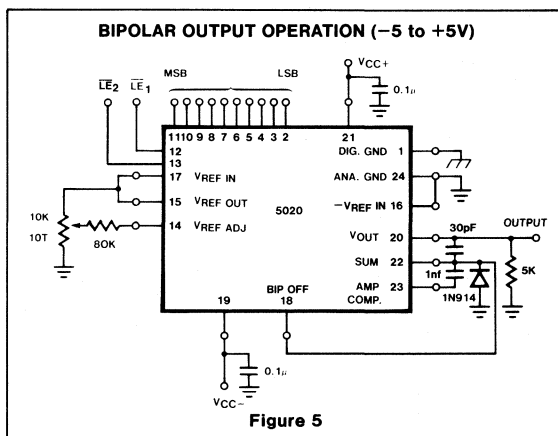
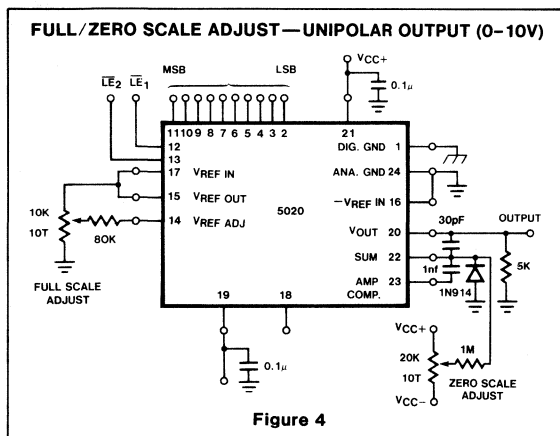
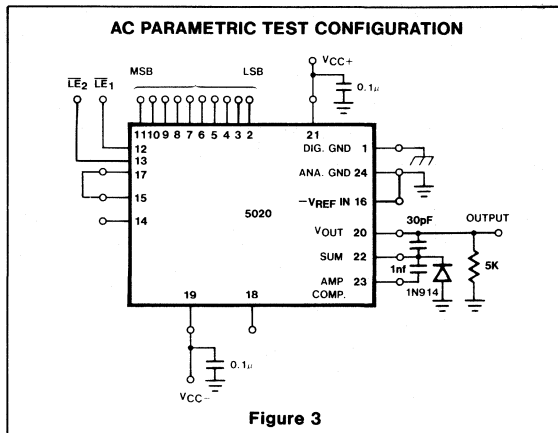
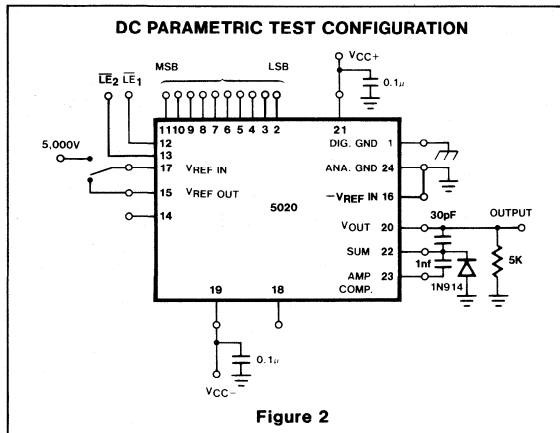
NOTES

3. Refer to Figure 3.
4. See Figure 6.
5. See Figure 7.
6. See Figure 8.
7. See Figure 9.
8. See Figure 10.

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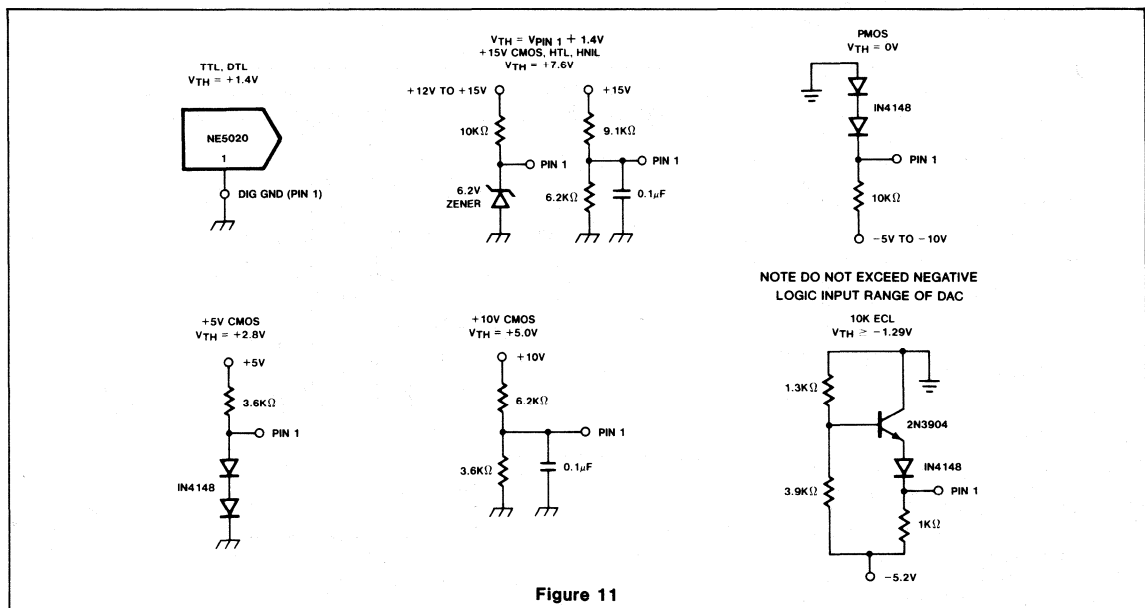
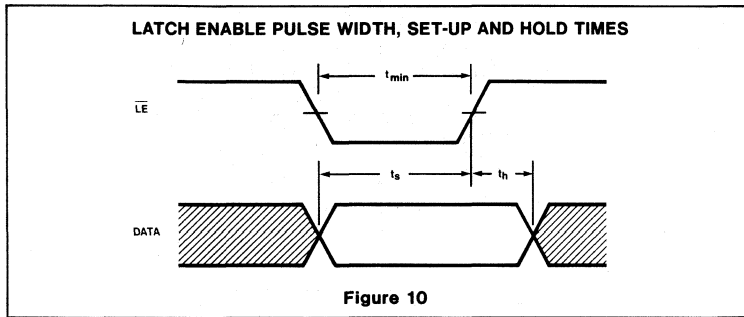
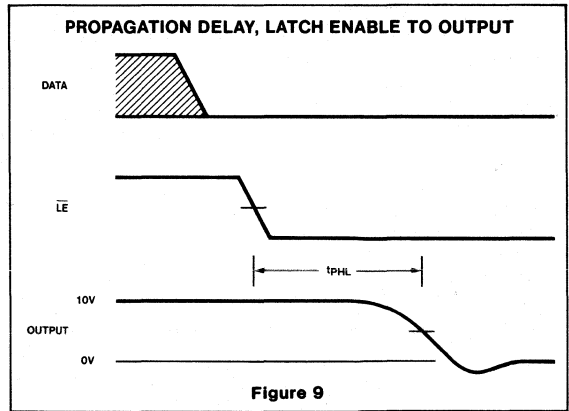
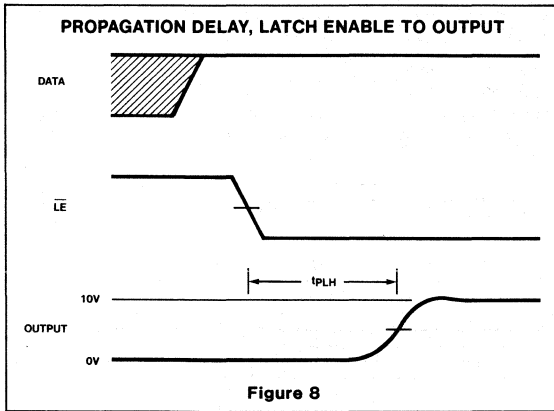
10-BIT μ P-COMPATIBLE D/A CONVERTER

NE5020



10-BIT μ P-COMPATIBLE D/A CONVERTER

NE5020



10-BIT μ P-COMPATIBLE D/A CONVERTER

NE5020

CIRCUIT DESCRIPTION

The NE5020 provides ten data latches, an internal voltage reference, application resistors, and a scaled output voltage, in addition to the basic DAC components (see block diagram, figure 1).

Latch Circuit

Digital interface with the NE5020 is readily accomplished through the use of two latch enable ports (\overline{LE}_1 and \overline{LE}_2) and ten data input latches. \overline{LE}_2 controls the two most significant bits of data (DB_9 and DB_8) while \overline{LE}_1 controls the eight lesser significant bits (DB_7 through DB_0). Both the latch enable ports (\overline{LE}) and the data inputs are static and threshold sensitive. When the latch enable ports (\overline{LE}) are high (Logic '1') the data inputs become very high impedances and essentially disappear from the data bus. Addressing the \overline{LE} with a low (Logic '0') the latches become active and adapt the logic states present on the data bus. During this state, the output of the DAC will change to the value proportional to the data bus value. When the latch enable returns to a high state, the selected set of data inputs (i.e., depending on which \overline{LE} goes high) 'memorize' the data bus logic states and the output changes to the unique output value corresponding to the binary word in the latch.

The data inputs are inactive and high impedance (typically requiring $-2\mu A$ for low (.8V max) or $0.1\mu A$ for high (2.0V min)) when the \overline{LE} is high. Any changes on the data bus with \overline{LE} high will have no effect on the DAC output.

The digital logic inputs (\overline{LE} and DB) for the NE5020 utilize a differential input logic system with a threshold level of +1.4 volts with respect to the voltage level on the digital ground pin (Pin 1). Figure 11 details several bias schemes used to provide the proper threshold voltage levels for various logic families.

To be compatible with a bus orientated system the DAC should respond in as short a period as possible to insure full utilization of the microprocessor, controller and I/O control lines. Figure 10 shows the typical timing requirements of the latch and data lines. This figure indicates that data on the data bus should be stable for at least 50nsec after \overline{LE} is changed to a high state.

The independent \overline{LE} (\overline{LE}_1 and \overline{LE}_2) lines allow for direct interface from an 8 bit data bus (see figure 12). Data for the two MSB's is supplied and stored when \overline{LE}_2 is activated low and returned high according to the NE5020 timing requirements. Then \overline{LE}_1 is activated low and the remaining eight LSB's of data are transferred into the DAC. With

\overline{LE}_1 returning high the loading of ten bit data word from an eight bit data bus is complete.

Occasionally the analog output must change to its data value within one data address operation. This is no problem using the NE5020 on a 16 bit bus or any other data bus with 10 or greater data bits.

This can be accomplished from an 8 bit data bus by utilizing an external latch circuit to preload the two MSB data values. Figure 13 shows the circuit configuration.

After preloading (via \overline{LE} pre-load) the external latch with the two MSB values, \overline{LE}_2 is activated low and the eight LSB's and the

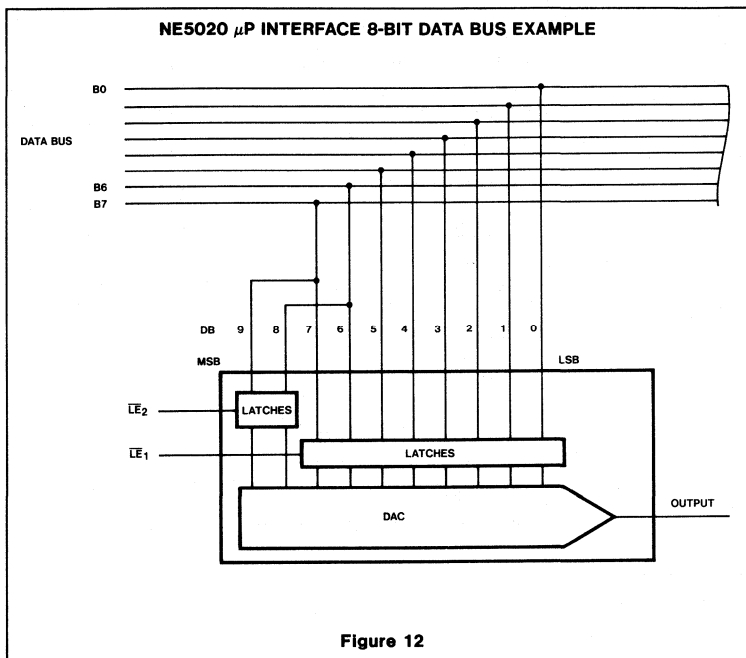


Figure 12

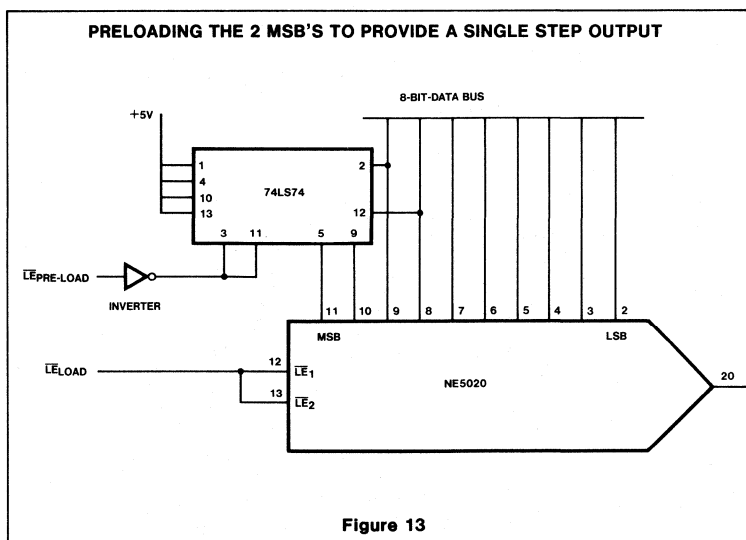


Figure 13

10-BIT μ P-COMPATIBLE D/A CONVERTER

NE5020

two MSB's are concurrently loaded into the DAC in one address operation. This permits the DAC output to make its appropriate change at one time.

Reference Interface

The NE5020 contains an internal bandgap voltage reference which is designed to have a very low temperature coefficient and excellent long term stability characteristics.

The internal bandgap reference (1.23V) is buffered and amplified to provide the 5 volt reference output. Providing a V_{REFADJ} (pin 14) allows trimming of the reference output. Utilization of the adjust circuit shown in figure 16 performs not only V_{REF} adjustment but also full scale output adjust. Notice that the V_{REFADJ} pin is essentially the sum node of an op amp and is sensitive to excessive node capacitance. Any capacitance on the node can be minimized by placing the external resistors as close as possible to the V_{REFADJ} pin and observing good layout practices.

The V_{REF} out node can drive loads greater than the DAC V_{REF} input requirements and can be used as an excellent system voltage reference. However, to minimize load effects on the DAC system accuracy, it is recommended that a buffer amplifier is used.

Input Amplifier

The DAC reference amplifier is a high gain internally compensated op amp used to convert the input reference voltage to a precision bias current for the DAC ladder network.

Figure 1 details the input reference amplifier and current ladder. The voltage to current converter of the DAC amp will generate a 1mA reference current through Q_R with a 5 volt V_{REF} . This current sets the input bias to the ladder network. Data bit 9 (DB_9)(Q_9), when turned on, will mirror this current and will contribute 1mA to the output. DB_8 (Q_8) will contribute $\frac{1}{2}$ of that value or 0.5mA and so on. These current values act as current sinks and will add at the sum node to produce a DAC ladder to sum node function of:

$$I_{OUT} = \frac{2V_{REF}}{R_{REF}} \left(\frac{DB_9}{2} + \frac{DB_8}{4} + \frac{DB_7}{8} + \frac{DB_6}{16} + \frac{DB_5}{32} + \frac{DB_4}{64} + \frac{DB_3}{128} + \frac{DB_2}{256} + \frac{DB_1}{512} + \frac{DB_0}{1024} \right)$$

Because of the fixed internal compensation of the reference amp, the slew rate is limited to typically $0.7V/\mu\text{sec}$ and source impedances at the V_{REF} INPUT greater than $5k\Omega$ should be avoided to maintain stability.

The $-V_{REF}$ INPUT pin is uncommitted to allow utilization of negative polarity reference voltages. In this mode $+V_{REF}$ INPUT is grounded and the negative reference is tied directly to the $-V_{REF}$ INPUT. The $-V_{REF}$ INPUT contains a $5k\Omega$ resistor that matches a like resistor in the $+V_{REF}$ INPUT to reduce voltage offset caused by op amp input bias currents.

Output Amplifier and Interface

The NE5020 provides an on chip output op amp to eliminate the need for additional external active circuits. Its two stage design with feed forward compensation allows it to slew at $15V/\mu\text{sec}$ and settle to within $\pm \frac{1}{2}$ LSB in $5\mu\text{sec}$. These times are typical when driving the rated loads of $R_L \geq 5k$ and $C_L \leq 50pF$ with recommended values of $C_{FF} = 1nF$ and $C_{FB} = 30pF$. Typical input offset voltages of 5mV and 50k open loop gain insure an accurate current to voltage conversion is performed when using the on chip R_{FB} resistor. R_{FB} is matched to R_{REF} and R_{BIP} to maintain accurate voltage gain over operating conditions. The diode shown from ground to sum node prevents the DAC current switches from saturating the op amp during large signal transitions which would otherwise increase the settling time.

The output op amp also incorporates output short circuit protection for both positive and negative excursions. During this fault condition I_{OUT} will limit at $\pm 15mA$ typical. Recovery from this condition to rated accuracy will be determined by duration of short circuit and die temperature stabilization.

Bipolar Output Voltage

The NE5020 includes a thermally matched resistor, R_{BIP} , to offset the output voltage by 5 volts to obtain $-5V$ to $+5V$ output voltage range operation. This is accomplished by shorting pins 18 and 22 (see figure 14). This connection produces a current equal to $(V_{REF IN} - V_{sum node}) \div R_{BIP}$, (1mA nominal), which is injected into the sum node. Since full scale current out is approximately 2mA (1.9980mA), $(2mA - 1mA)5k = 5V$ will appear at the output. For zero DAC output currents, 1mA is still injected into sum mode and $V_{OUT} = -(5k)(1mA) = -5V$. Zero scale adjust and full scale adjust are performed as described below, noting that full scale voltage is now approximately +5 volts, zero scale adjust may be used to trim $V_{OUT} = 0.00$ with the MSB high or $V_{OUT} = -5.0V$ with all bits off.

Zero Scale Adjustment

The method of trimming the small offset error that may exist when all data bits are low is shown in figure 15. The trim is the result of injecting a current from resistor R_2 that counteracts the error current. Adjusting potentiometer R_1 until V_{OUT} equals 0.000 volts in the unipolar mode or -5.000 volts in the bipolar mode (see bipolar section) accomplishes this trim.

Full Scale Adjustment

A recommended full scale adjustment circuit when using the internal voltage reference is shown in figure 16. Potentiometer R_3 is adjusted until V_{OUT} equals 9.99023V. In many applications where the absolute accu-

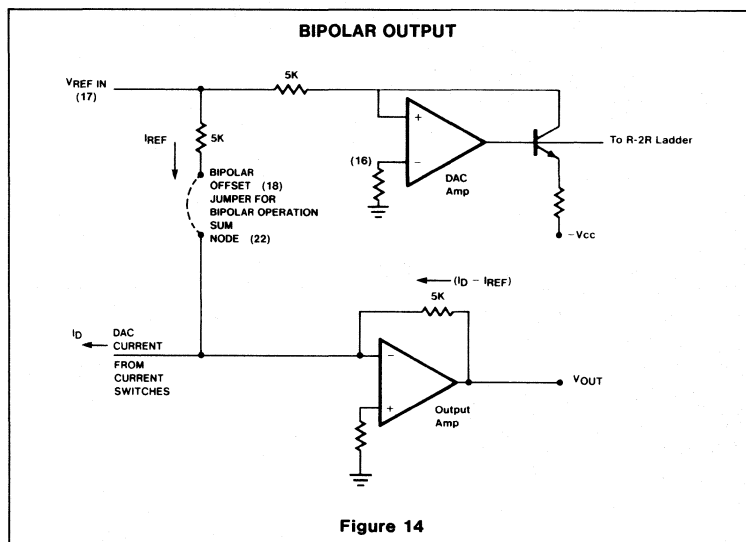


Figure 14

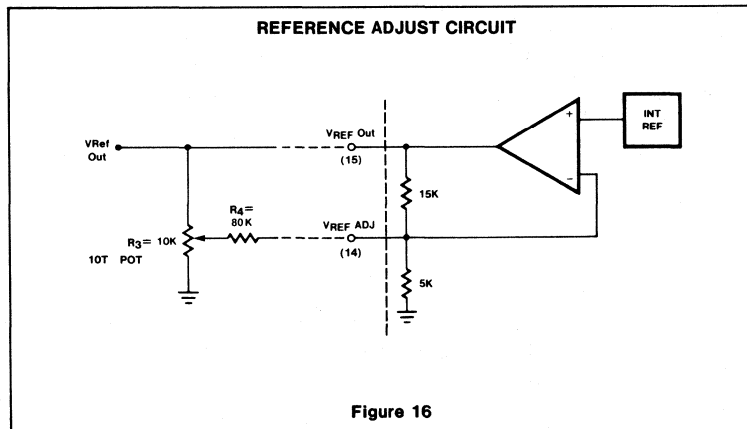
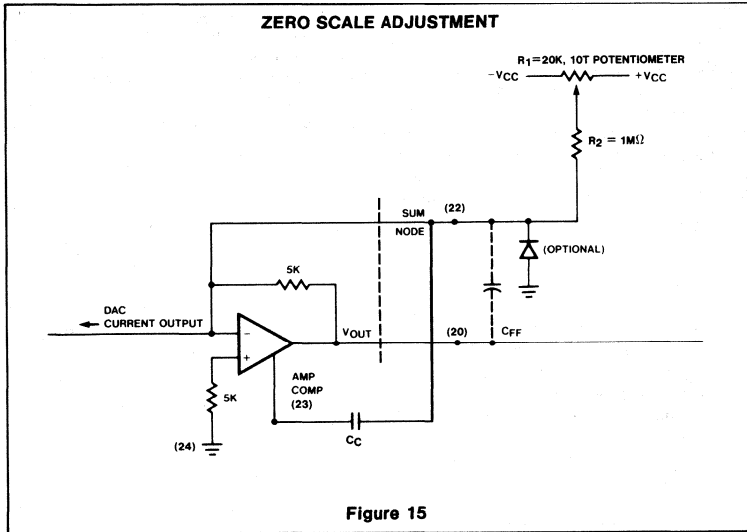
10-BIT μ P-COMPATIBLE D/A CONVERTER

NE5020

racy of full scale is of low importance when compared to the other system accuracy factors, then this adjustment circuit is optional.

As resistors R_{REF} , R_{fb} and R_{BIP} shown in figure 1 are integrated in close proximity,

they match and track in value closely over wide ambient temperature variations. Typical matching is less than $\pm 0.3\%$ which implies that typical full scale (or gain) error is less than $\pm 0.3\%$ of ideal full scale value.



8-BIT GENERAL PURPOSE A/D CONVERTER

NE5034

DESCRIPTION

The NE5034 is a high-speed microprocessor-compatible 8-bit Analog-to-Digital converter. It uses the successive approximation technique, and includes the comparator, reference DAC, SAR, an internal clock and three-state buffers all on the same chip.

The converter can accommodate a wide analog input voltage range, bipolar or unipolar, selectable through external input resistors. An external capacitor controls the internal clock frequency, providing conversion times down to 17 μ s. Faster conversion times are possible using an external clock.

Microprocessor interfacing requirements are simple, allowing analog-to-digital conversion with a minimum of external components.

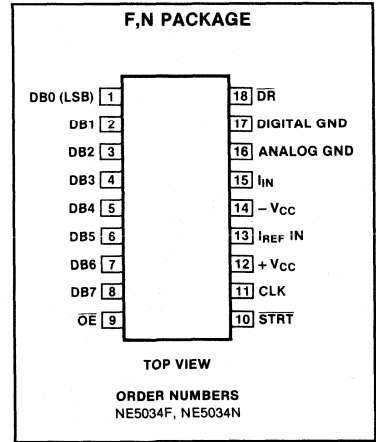
FEATURES

- 8-bit resolution and accuracy
- Accepts unipolar or bipolar inputs
- Three-state output buffers for easy microprocessor interface
- Choice of internal or external clocking
- Short conversion time, 17 μ s typical using internal clock

APPLICATIONS

- All microprocessor-based monitoring and control systems requiring analog signal inputs.
- Typical applications include: Automated process control, machine tools, robots, test and measurement instruments, environmental controls
- Other applications include: Ratiometric A/D conversion, very high resolution A/D conversion systems requiring high speed 8-bit building blocks

PIN CONFIGURATION

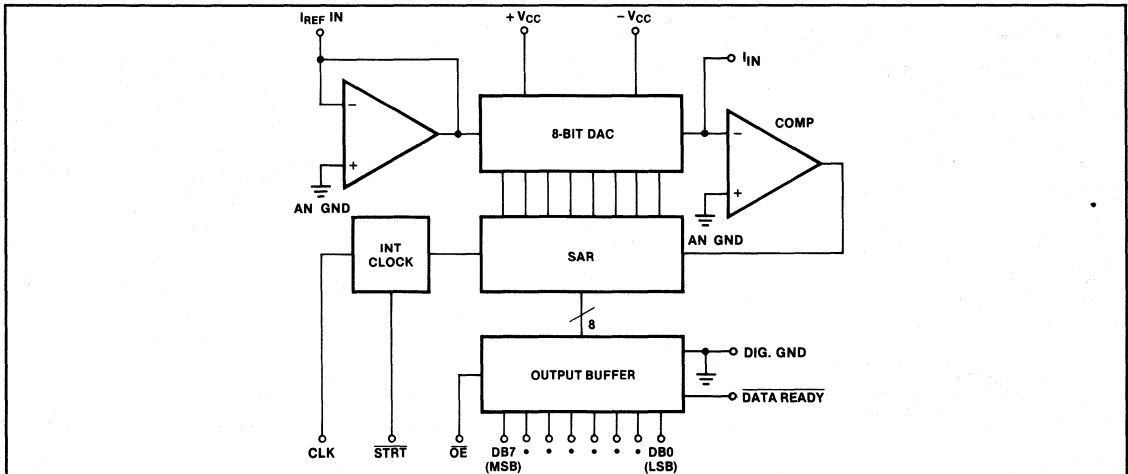


ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC+} Positive supply voltage	0 to +6	V
V _{CC-} Negative supply voltage	0 to -15	V
I _{REF} Reference current	1.5	mA
I _{IN} Analog input current	5.0	mA
V _O Data output voltage	6.0	V
Analog GND to Digital GND	1.0	V
V _L Logic input voltage	-1 to V _{CC+}	V
P _D Power dissipation	N package	800
	F package	1000
T _A Operating temperature range	0 to +70	°C
T _{STG} Storage temperature range	-65 to +150	°C
T _{SOLD} Lead soldering temperature (10 seconds)	300	°C

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BLOCK DIAGRAM



8-BIT GENERAL PURPOSE A/D CONVERTER

NE5034

DC ELECTRICAL CHARACTERISTICS + $V_{CC} = 5.0V$, $-V_{CC} = -12V$, $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		8	8	8	Bits
Relative accuracy error ^{1, 2}				± 1/2	LSB
V_{CC+} Positive supply range		4.75	5.0	5.25	V
V_{CC-} Negative supply range		-11.4	-12	-12.6	V
E_{FS} Full scale gain error	$I_{REF} = 1.0mA$, $T_A = 25^{\circ}C$		± 2	± 5	LSB
E_{ZS} Zero scale offset error	$I_{REF} = 1.0mA$, $T_A = 25^{\circ}C$		± 0.5	± 1	LSB
Ps_r Power supply rejection ³	$I_{REF} = 1.0 mA$, $V_{CC} + 4.75$ to $+ 5.25V$, $V_{CC} - 11.4$ to $- 12.6V$			± 1/2	LSB
V_{IH} Logic 1 input voltage (\overline{STRT} and \overline{OE})		2.0			V
V_{IH} Logic 1 input voltage ext. clock		2.4			V
V_{IL} Logic 0 input voltage (\overline{STRT} and \overline{OE})				0.8	V
V_{IL} Logic 0 input voltage ext clock				0.7	V
I_{IH} Logic 1 input current (\overline{STRT} and \overline{OE})	$V_{IN} = 2.4V$			20	μA
I_{IH} Logic 1 input current ext clock	$V_{IN} = 2.4V$		100		μA
I_{IL} Logic 0 input current (\overline{STRT} and \overline{OE})	$V_{IN} = 0.4V$		-20	-100	μA
I_{IL} Logic 0 input current ext. clock	$V_{IN} = 0.7V$		-100		μA
V_{OL} Logic 0 output voltage	$I_{OL} = 1.6mA$, $\overline{OE} = 0.8V$			0.4	V
V_{OH} Logic 1 output voltage	$I_{OH} = 400\mu A$, $\overline{OE} = 0.8V$	2.4			V
I_{OZ} Three-state leakage	$\overline{OE} = 2.0V$, $V_{OL} = 0V$ or $5V$		± 10		μA
I_{CC+} Positive supply current	$V_{CC} + 5V$, $V_{CC} - 12V$		18	36	mA
I_{CC-} Negative supply current	$V_{CC} + 5V$, $V_{CC} - 12V$		-11	-22	mA

NOTES

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero scale to full scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 8-bit level which is 0.39% of the full scale voltage.
3. MAX change in full scale.

AC ELECTRICAL CHARACTERISTICS $V_+ = +5V$, $V_- = -12V$, $T_A = 25^{\circ}C$

SYMBOL & PARAMETER	TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal clock frequency			$C_L = 60pF$ (See Figure 1)		500		KHz
External clock frequency						700	KHz
T_w \overline{STRT} pulse width			Clock freq. = 500KHz	400			ns
External clock pulse width positive/negative				600			ns
Set up time ¹			See Figure 3	300			ns
t_p (out data) propagation delay	data out	\overline{OE}	See Figure 2		50	200	ns
t_p (out \overline{DR}) propagation delay	data ready out	8th clock	See Figure 3		700		ns
t_p (3-state) propagation delay 3-state	high impedance o/p	\overline{OE}	See Figure 2		60	200	ns
t_p (DB0) propagation delay	DB0	\overline{DR}	See Figure 3			500	ns
t_p (SDR) \overline{STRT} low to \overline{DR} high	data ready high	\overline{STRT} low	See Figure 3		700		ns

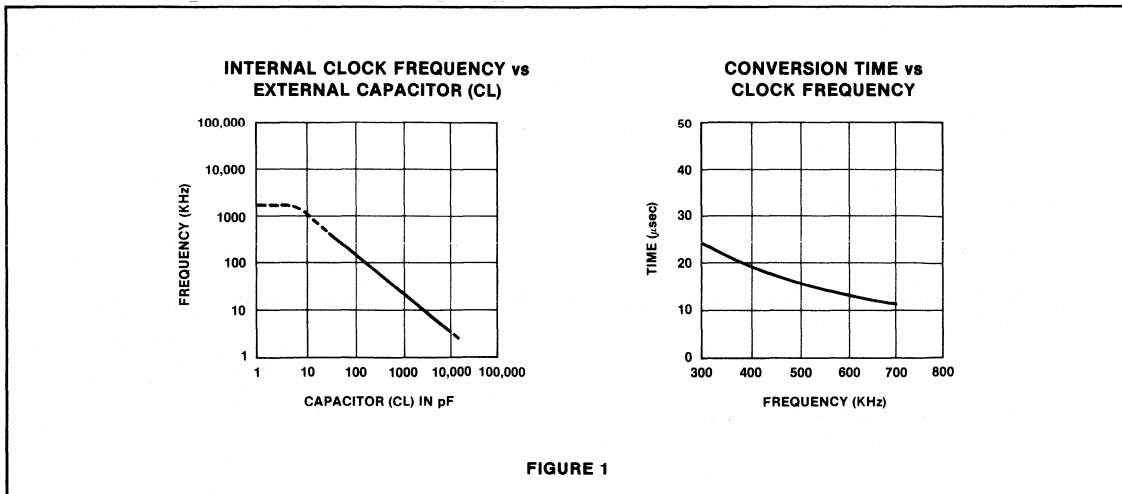
NOTE

1. See description of "Set up time".

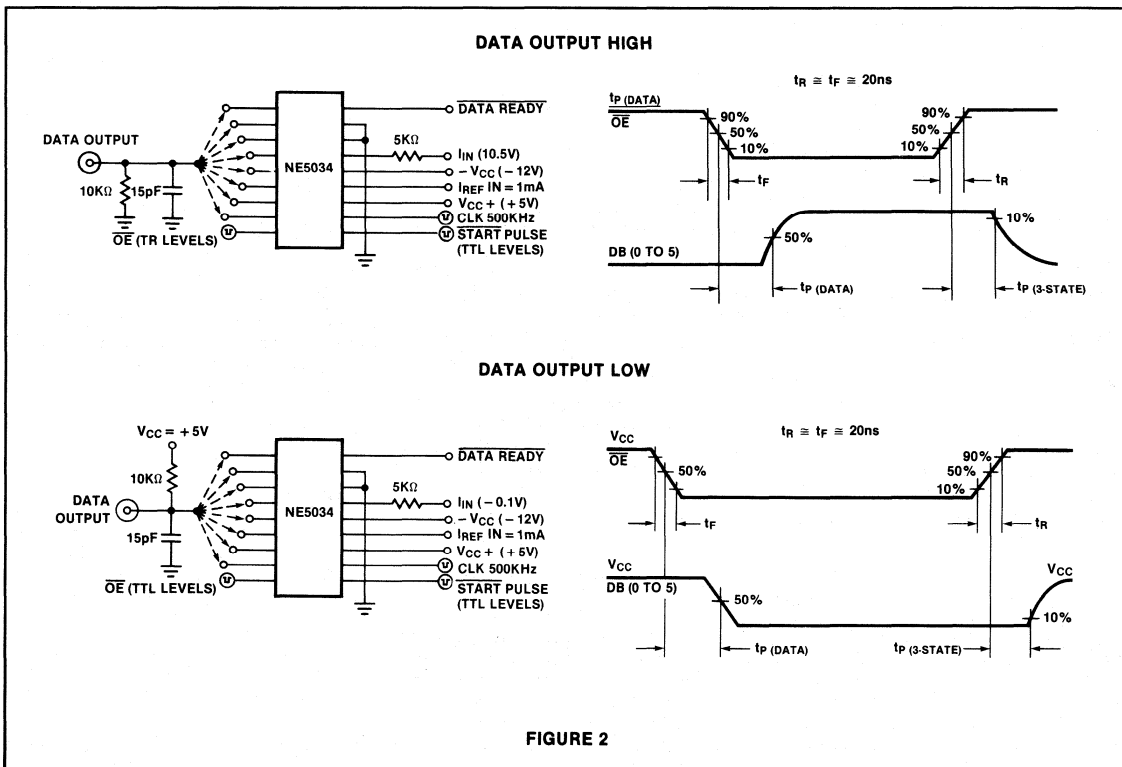
8-BIT GENERAL PURPOSE A/D CONVERTER

NE5034

TYPICAL PERFORMANCE CHARACTERISTICS



TEST LOAD CIRCUITS



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8-BIT GENERAL PURPOSE A/D CONVERTER

NE5034

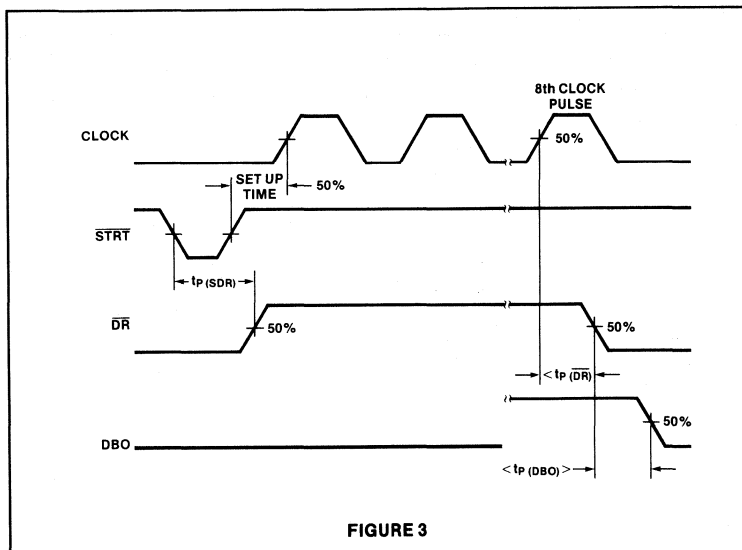


FIGURE 3

The comparator determines whether the output current of the DAC is greater or less than the input current converted from the unknown analog input voltage through an external input resistor. If the DAC output current is greater, the data latch for the trial bit is reset to a '0'; if it is less, the trial data bit stays at '1'. After all the bits from DB7 to DB0 have been tried, the SAR contains a valid 8-bit binary output code which accurately represents the unknown analog input to within $\pm 1/2$ LSB ($\pm 0.2\%$). This binary output will now remain in the SAR until another STRT pulse is applied.

During the successive-approximation sequence, the DATA READY signal remains at '1'. Upon completion of the conversion, the signal goes to a '0', indicating that data is valid and ready. If the \overline{OE} input is left at a '0' during the conversion, the DATA OUTPUT shows the conversion sequence (see short cycle section). When the \overline{OE} line is made a logic '1', the output buffers will go to a high impedance state and will remain so until the \overline{OE} is returned to a '0' state.

FUNCTIONAL PIN DEFINITIONS

DATA READY (\overline{DR})

This is an output pin used to indicate that a conversion is in progress. \overline{DR} goes to a logic "1" when STRT is at a logic "0". At the completion of a conversion \overline{DR} returns to a logic "0". There is a delay (MAX 0.5 μ s) from the time \overline{DR} goes to "0" to the time DBO data is valid.

DB0-DB7

Eight three-state data outputs each with a drive capability of one TTL load. DB0 is the LSB and DB7 is the MSB.

 \overline{OE}

Output enable input. When \overline{OE} is at a logic "1" the data outputs assume a high impedance state. With \overline{OE} at a logic "0", data is placed on the outputs. Data appearing on the outputs is only valid if both \overline{OE} and \overline{DR} are at logic "0" (see note on \overline{DR} timing).

STRT

This pin is used to reset the converter and start a new conversion. A logic "0" applied to this pin for a minimum of 400ns will reset the converter to a condition with DB7 at a logic "1" and all other Data outputs at logic "0". It will also cause \overline{DR} to go to a logic "1" (see timing diagrams for delay times). Conversion will start with the 1st clock pulse after STRT returns to a

logic "1" (see notes on set up time required). A STRT pulse while a conversion is taking place will cause the conversion to be aborted and the converter will reset. (See notes on short-cycle operation.)

CLK IN

An external capacitor between this pin and ground generates the internal clock pulses. (See diagram for clock frequency vs capacitor value). In order to synchronize the internal clock, to the start pulse a diode (small signal type e.g., 1N914) should be connected between STRT and CLK IN (see Figures 4 and 5). Without this diode the start pulse could occur at a time which could cause one of the conditions described in the Note on "set up" time. Applying an external TTL-or MOS-compatible clock to this pin slaves the NE5034 to external clock frequency. In this case, the diode is not required but the "set up" time requirements should be noted.

BASIC CIRCUIT DESCRIPTION

The NE5034 is an 8-bit A/D converter which incorporates the successive-approximation conversion method. Upon receipt of the STRT pulse, successive bits, beginning with the MSB (DB7), are applied to the input of the internal 8-bit current output DAC by the I^2L successive-approximation register (SAR) (see Block Diagram).

TIMING DESCRIPTION

The timing diagram shown in Figure 7 shows the successive trial and decisions for each data bit.

With STRT at a logic "0" the converter is reset to a condition with DB7 at a logic "1", DR at a logic "1" and DB0-DB6 at logic "0".

Conversion starts after STRT returns to a logic "1". Starting with DB7 each bit is tried in turn, with the decision point being at the time of the positive going edge of the clock. Starting with the first positive edge after STRT returns to logic "1" (see note on "set up" time). The 8th positive going edge makes the decision on DB0 (LSB) and also causes \overline{DR} to return to a logic "0" to indicate the conversion is complete. (See note on \overline{DR} timing.)

SHORT-CYCLE OPERATION

In applications where less than 8 bits of resolution are required the NE5034 can be operated to achieve shorter conversion times. No hard wire changes are required to perform "short-cycling".

Conversion to X number of bits is completed at the end of $X + 0.5$ clock cycles (after a start pulse) \overline{DR} will still be at a logic "1" state.

\overline{OE} can be used to 3-state the outputs even during short-cycle operation.

8-BIT GENERAL PURPOSE A/D CONVERTER

NE5034

BASIC SET-UP DIAGRAM UNIPOLAR INPUT VALUES (0--10V)

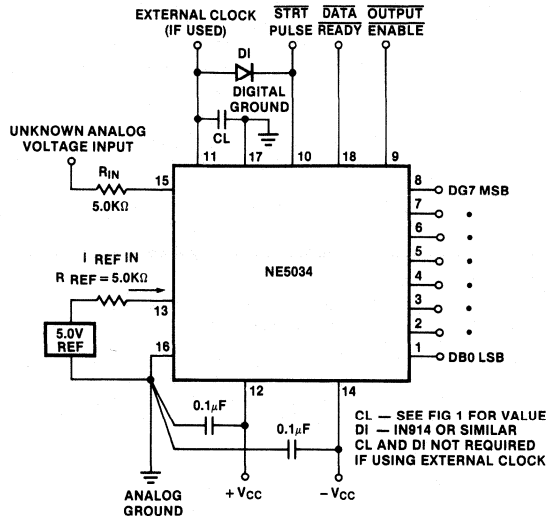


FIGURE 4.

BASIC SET-UP DIAGRAM BIPOLAR INPUT VALUES ($\pm 10V$ RANGE)

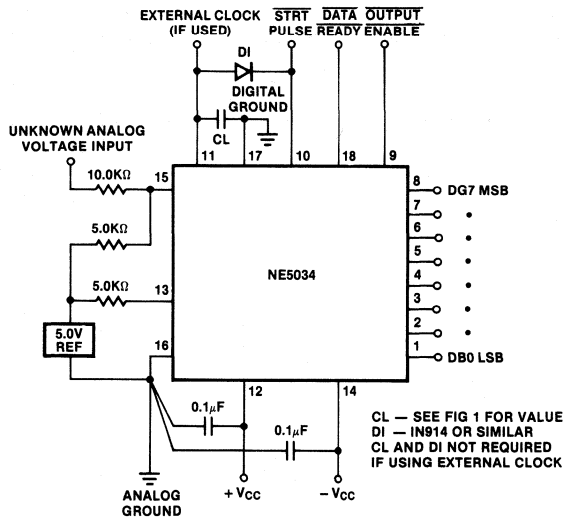


FIGURE 5.

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8-BIT GENERAL PURPOSE A/D CONVERTER

NE5034

SET UP TIME

When using an external clock, the positive going edge of the start pulse must be synchronized to the clock pulse. There is a "set up" time of 300ns required between the time of the start pulse returning to a logic "1" and the next positive going edge of the clock.

If the positive edge of the start pulse occurs less than 300ns prior to the positive clock edge, one of the following conditions will occur:

- The converter recognizes the clock pulse and converts as normal.
- The conversion starts one clock pulse later.
- The conversion never starts, this will be indicated by the fact that \overline{DR} does not return to logic "0". In this case a new start pulse will be required.

DATA READY (\overline{DR}) TIMING

After \overline{DR} returns to a logic "0" indicating a conversion is complete there is a time delay of 500ns before the data at $DB0$ output (the Least Significant Bit) is valid.

ZERO OFFSET (NEGATIVE FULL SCALE) CALIBRATION PROCEDURES

- Apply continuous start pulses to the \overline{STRT} input.
- Apply 1/2 LSB in the case of unipolar operation, or 1/2 LSB above - FS in the case of bipolar operation to the analog input.

- Observe all data outputs after each conversion is completed.
- Adjust the potentiometer connected to I_{IN} (see Figure 6) until the LSB flickers between '0' and '1', and all other data outputs remain '0' following each conversion.

FULL SCALE (POSITIVE FULL SCALE) CALIBRATION:

- Apply continuous start pulses to the \overline{STRT} input.
- Apply full scale minus 1 1/2 LSB to the analog input.
- Observe all data outputs after each conversion is completed.
- Adjust the voltage applied to $V_{REF IN}$ (Figure 4) until the LSB varies between '0' and '1', and all other data outputs stay '1' after each conversion.

NOTE:

- Where an input of 1/2 LSB is called for, the voltage is equal to $\frac{FS}{256}$.
- The sequence of calibration should be:
 - Zero offset
 - Full scale adjust
 - Zero offset
 - Full scale adjust

OPERATING PRECAUTIONS:

Analog and digital grounds should have separate returns. Noise and jitter on digital ground will degrade accuracy unless the input is referenced to a 'clean' analog ground.

UNIPOLAR BINARY OPERATION:

A standard connection for a 0 to 10V unipolar binary operation, with $V_{REF IN}$ equal to +5 volts, is shown in Figure 4. The NE5034 can quantize full scale ranges of 1V to 10V. It should be noted, however, that for smaller full scale ranges, the accuracy and speed will degrade.

The input voltage versus output code relationship for unipolar operation is shown in Table 1. The full scale range is 2 times $I_{REF IN}$.

Table 1. Unipolar—Binary

ANALOG INPUT NOTES 1, 2, 3	DIGITAL OUTPUT CODE	
	MSB	LSB
FS—1 LSB	1 1 1 1 1 1 1 1	1
FS—2 LSB	1 1 1 1 1 1 1 0	0
3/4 FS	1 1 0 0 0 0 0 0	0
1/2 FS + 1 LSB	1 0 0 0 0 0 0 1	1
1/2 FS	1 0 0 0 0 0 0 0	0
1/2 FS—1 LSB	0 1 1 1 1 1 1 1	1
1/4 FS	0 1 0 0 0 0 0 0	0
1 LSB	0 0 0 0 0 0 0 1	1
0	0 0 0 0 0 0 0 0	0

Table 2. Bipolar—Offset Binary

ANALOG INPUT NOTES 1, 3, 4	DIGITAL OUTPUT CODE	
	MSB	LSB
+(FS—1 LSB)	1 1 1 1 1 1 1 1	1
+(FS—2 LSB)	1 1 1 1 1 1 1 0	0
+(1/2 FS)	1 1 0 0 0 0 0 0	0
+(1 LSB)	1 0 0 0 0 0 0 1	1
0	1 0 0 0 0 0 0 0	0
-(1 LSB)	0 1 1 1 1 1 1 1	1
-(1/2 FS)	0 1 0 0 0 0 0 0	0
-(FS—1 LSB)	0 0 0 0 0 0 0 1	1
-FS	0 0 0 0 0 0 0 0	0

BIPOLAR (OFFSET BINARY) OPERATION:

A standard connection for a -5 to +5V or -10 to +10V bipolar operation is shown in Figure 5.

NOTES:

- Analog inputs shown are nominal center values of code.
- "FS" is full scale; i.e., $2I_{REF IN}$ (Unipolar mode).
- 1 LSB equals (2^{-8}) (FS).
- "FS" is full scale; i.e., $I_{REF IN}$ (Bipolar mode).

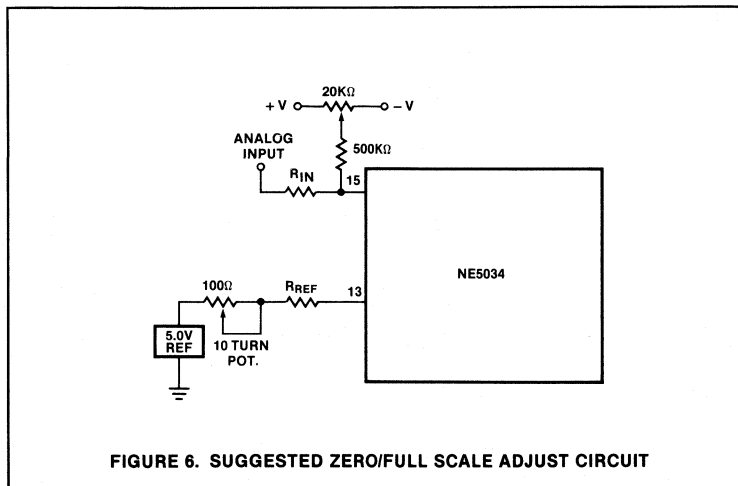
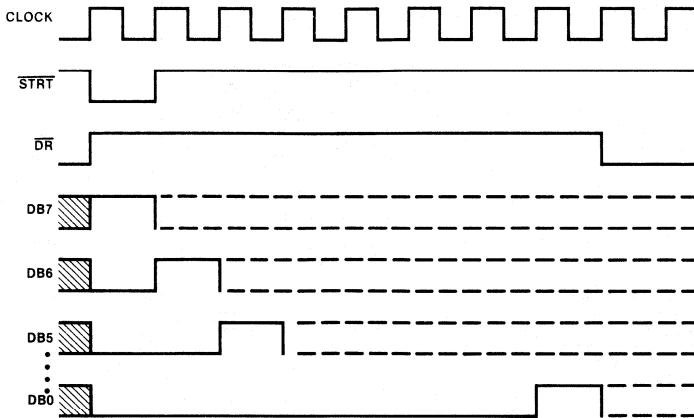


FIGURE 6. SUGGESTED ZERO/FULL SCALE ADJUST CIRCUIT

8-BIT GENERAL PURPOSE A/D CONVERTER

NE5034



NOTE
1. OE = Logic "0"
2. See "Short-Cycle" section

FIGURE 7. NE5034 TIMING DIAGRAM

6-BIT A/D CONVERTER (SERIAL OUTPUT)

NE5036

Preliminary

DESCRIPTION

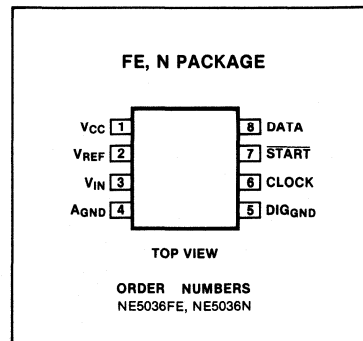
The NE5036 is an easy to use, low cost, successive approximation Analog to Digital converter, fabricated in Bipolar/I²L technology, and packaged in a convenient 8-pin mini dip package.

With an external reference voltage, the NE5036 will accept input voltages between 0V and V_{REF}. Holding the START pin low for at least 8 clock pulses in duration will provide the 6-bit result of the conversion in a serial format.

FEATURES

- Three-state output buffer for easy μ Processor interfacing
- Fast successive approximation converter, 23 μ sec
- T²L compatible inputs and outputs
- Easy interface to CMOS μ Processors
- Guaranteed no missing codes over full operating range
- Single supply operation, +5V
- High impedance analog inputs
- Positive true binary serial output

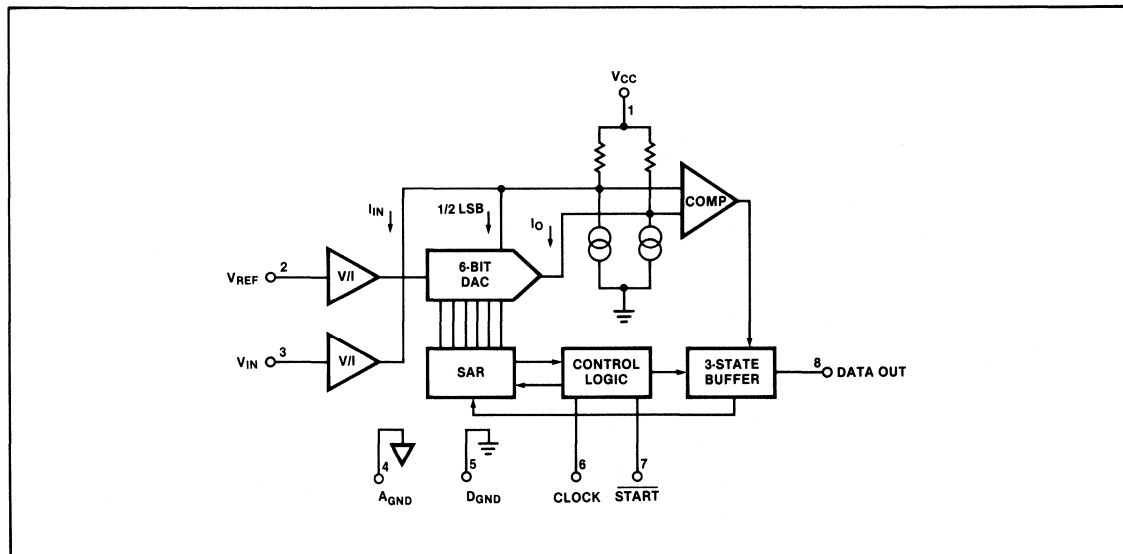
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC}	Power supply voltage	7 V
V _{REF}	Reference voltage	7 V
V _{IN (Analog)}	Analog input voltage	7 V
V _{IN (Digital)}	Digital input voltage (START & CLOCK)	7 V
D _{OUT}	Data output pin	
	Three-state mode	7 V
	Enabled mode	20 mA
Δ GND	Analog GND to digital GND	± 1 V
T _A	Operating temperature range	0 to 70 °C
T _{Stg}	Storage temperature range	-65 to 150 °C
t _{Sold}	Lead soldering temperature	300 °C
P _D	Power dissipation	
	FE package	220 mW
	N package	220 mW

BLOCK DIAGRAM



6-BIT A/D CONVERTER (SERIAL OUTPUT)

NE5036

Preliminary

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V$; $V_{REF} = 2.0V$; Clock = 350kHz; $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified. Typical values are specified at 25°C.

SYMBOL AND PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			6	6	6	Bits
Relative accuracy ^{1,2}				1/4	1/2	LSB
V_{CC}	Positive supply voltage		+ 4.75	+ 5.0	+ 5.50	V
ϵ_{FS}	Full scale gain error ^{2,3,4}	$V_{REF} = 2.0V, T_A = 25^{\circ}C$		± 1	± 2	LSB
ϵ_{ZS}	Zero scale offset error ²	$V_{REF} = 2.0V, T_A = 25^{\circ}C$		$\pm 1/2$	- 1/2, + 2	LSB
P_{SR}	Power supply rejection Max change in full scale ²	$V_{REF} = 2.0V$ $4.75V \leq V_{CC} \leq 5.5V$		$\pm 1/2$	± 1	LSB
I_{IN}	Analog input bias current	$0 \leq V_{IN} \leq 2.5V$		1	10	μA
I_{REF}	Reference bias current	$0 \leq V_{REF} \leq 2.5V$		1	10	μA
R_{IN}	Analog input resistance		3	30		M Ω
V_{IH}	Logic '1' input voltage		2.0			V
V_{IL}	Logic '0' input voltage				0.8	V
I_{IH}	Logic '1' input current				10	μA
I_{IL}	Logic '0' input current				10	μA
I_{OH}	Logic '1' output current	$2.4V \leq V_{OH}$	300			μA
I_{OL}	Logic '0' output current	$V_{OL} \leq 0.4V$	1.6			mA
I_{OZ}	Three-state leakage current				± 40	μA
I_{CC}	Positive supply current			14	24	mA

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V$; $V_{REF} = 2.0V$; Clock = 350kHz; $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified. Typical values are specified at 25°C. (Refer to test figures.)

SYMBOL AND PARAMETER		TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}	Max clock frequency				350			kHz
T_{CONV}	Conversion time						8	Clock cycles
t_W	Clock pulse width				1.3			μS
t_S	Setup time, \overline{START} to clock ⁶	Clock	\overline{START}		500			ns
$t_{P(OUT)}$	Propagation delay ⁵	Data out	Clock	$T_A = 25^{\circ}C, t_r = t_f < 20ns$			600	ns
$t_{P(3-STATE)}$	Propagation delay ⁵	Data (3-State)	\overline{START}	$T_A = 25^{\circ}C, t_r = t_f < 20ns$			600	ns

NOTES

1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on the straight line drawn from zero scale to full scale of the device.
2. Specifications given in LSB's refer to the weight of the least significant bit at the bit level which is 1.56% of the full scale voltage.
3. Full scale gain error is the deviation of the code transition point (111110 to 111111) from its ideal value (accounting for offset error at 000000).
4. The analog input voltage (V_{IN}) range is from 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC} . (For optimum performance V_{REF} can be any value from 1.5V to 2.5V.)
5. The time between the specified reference points on the clock and the output waveforms with the output changing (low to high or high to low).
6. The high to low transition of the \overline{START} pulse should occur at least 500ns prior to the negative edge of the clock pulse to insure its recognition. The \overline{START} pulse should stay high for at least 500ns between conversions to guarantee proper recognition.

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6-BIT A/D CONVERTER (SERIAL OUTPUT)

NE5036

Preliminary

CIRCUIT DESCRIPTION

NE5036 is a complete 6-bit, serial output, A/D converter which incorporates the successive approximation method. The chip includes the internal control logic, the successive approximation register (SAR), 6-bit DAC, comparator and the output buffer. An externally generated clock source (max freq = 350 kHz) must be provided to pin 6. An external reference voltage supplied to pin 2 sets the full scale range of the A/D converter as shown in the Block Diagram.

Upon the $\overline{\text{START}}$ pin going low, successive approximation conversion commences after the first low going edge of the clock pulse. Successive bits, beginning with the MSB (D5) are applied to the input of the internal 6-bit current output DAC by the I²L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, converted

from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to 0 and simultaneously the output buffer goes to 0. If it is less that bit stays at 1 and the output buffer goes to 1. After the second high to low transition of the clock pulse, the MSB (D5) data is valid. On successive clock pulses, successive bits are tried and the output buffer represents that bit. $\overline{\text{START}}$ has to stay low for at least 8 clock pulses for the conversion to be completed and to access the 6-bit result of the conversion. A conversion in process can be interrupted by issuing another $\overline{\text{START}}$ pulse.

When $\overline{\text{START}}$ is in a high state, the output buffer is in a high impedance state.

The timing diagram for the device is shown in Figure 1.

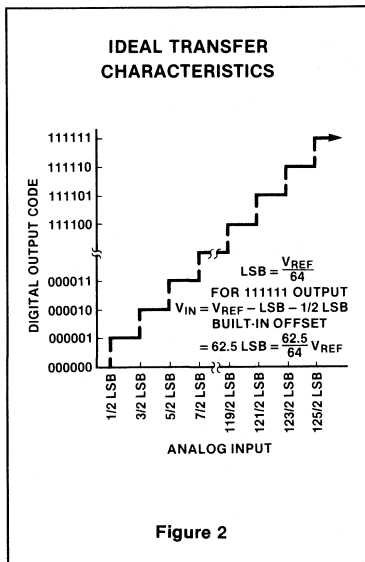
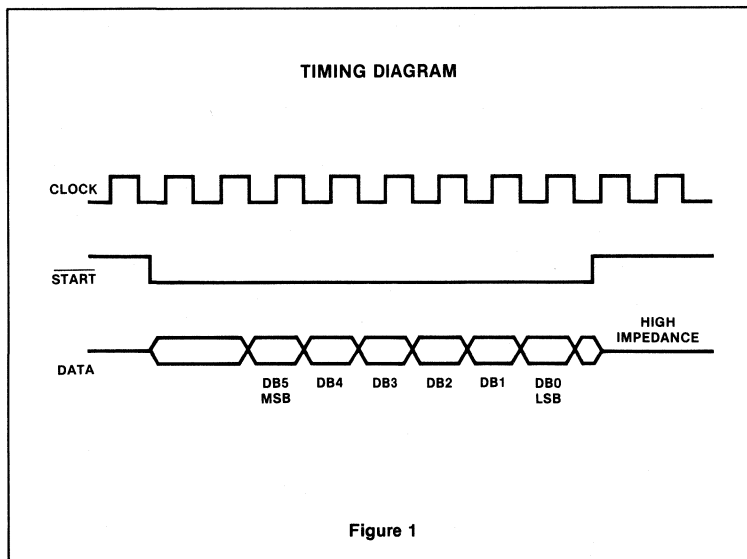
TRANSFER CHARACTERISTICS

The NE5036 is designed to have a nominal 1/2 LSB offset, so that the code transition points are located 1/2 LSB on either side of the exact analog input for a given code. Thus the first transition (000000 to 000001) will occur at an input of 1/2 LSB (15.63mV with a V_{REF} of 2.0V), plus any offset. Subsequent transition (to full scale — 111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

The ideal transfer characteristic of NE5036 is shown in Figure 2.

LAYOUT PRECAUTIONS

Analog ground (pin 4) and Digital ground (pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The leads to the analog inputs should be kept as short as possible to minimize input noise pickup. Input bypass capacitors from the analog inputs to ground will eliminate noise pickup. Power supplies should be decoupled with at least 1μF, located close to the device to minimize noise spikes on V_{CC}.



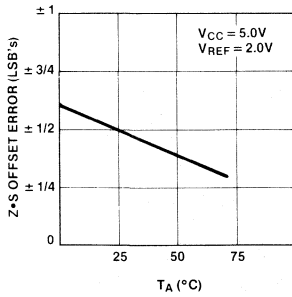
6-BIT A/D CONVERTER (SERIAL OUTPUT)

NE5036

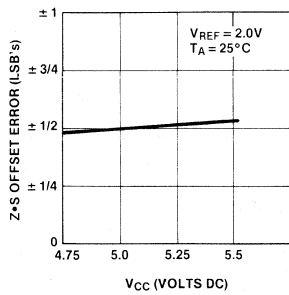
Preliminary

TYPICAL PERFORMANCE CHARACTERISTICS

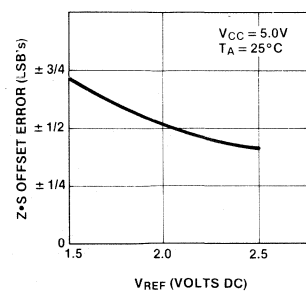
ZERO SCALE OFFSET ERROR vs TEMPERATURE



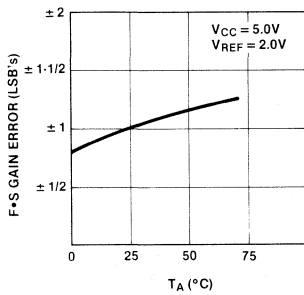
ZERO SCALE OFFSET ERROR vs VCC



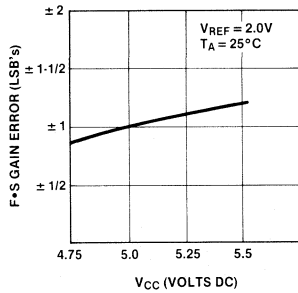
ZERO SCALE OFFSET ERROR vs VREF



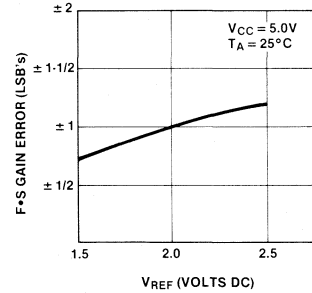
FULL SCALE GAIN ERROR vs TEMPERATURE



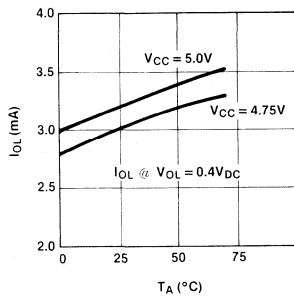
FULL SCALE GAIN ERROR vs VCC



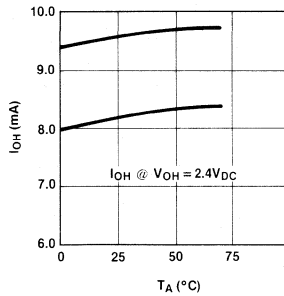
FULL SCALE GAIN ERROR vs RREF



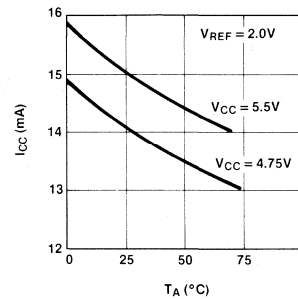
IO_L vs TEMPERATURE (DATA OUTPUT)



IO_H vs TEMPERATURE (DATA OUTPUT)



ICC vs TEMPERATURE



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6-BIT A/D CONVERTER (SERIAL OUTPUT)

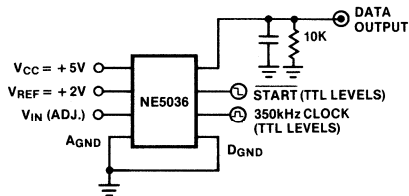
NE5036

Preliminary

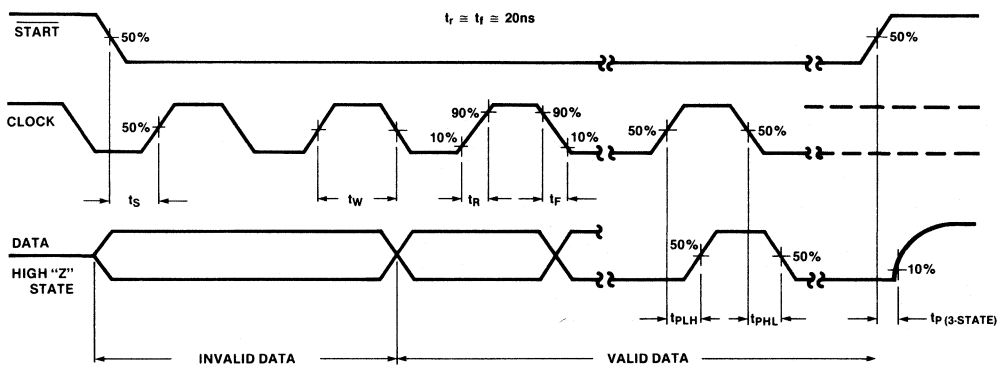
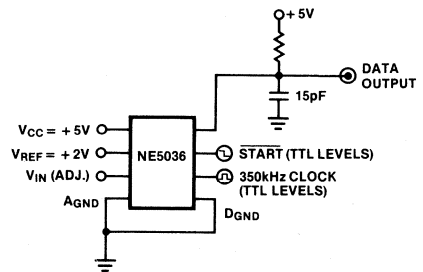
AC TEST CIRCUITS AND WAVEFORMS

PROPAGATION DELAY TIME t_p (DATA)

DATA OUTPUT (LOW TO HIGH)



DATA OUTPUT (HIGH TO LOW)



6-BIT A/D CONVERTER (PARALLEL OUTPUTS)

NE5037

Preliminary

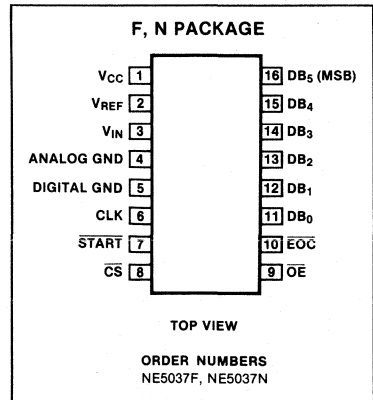
DESCRIPTION

The NE5037 is a low cost, complete successive approximation analog to digital (A/D) converter, fabricated in Bipolar/1²L technology. With an external reference voltage, the NE5037 will accept input voltages between 0V and V_{REF}. An external START pulse of at least 300ns in duration will provide the 6-bit result of the conversion in parallel format. Full conversion with no missing codes occurs in 9 μ s.

FEATURES

- T²L compatible inputs and outputs
- Three state output buffer
- Easy interface to CMOS μ Processors
- Fast conversion — 9 μ s
- Guaranteed no missing codes over full temp range
- Single supply operation, +5V
- Positive true binary outputs
- High impedance analog inputs

PIN CONFIGURATION

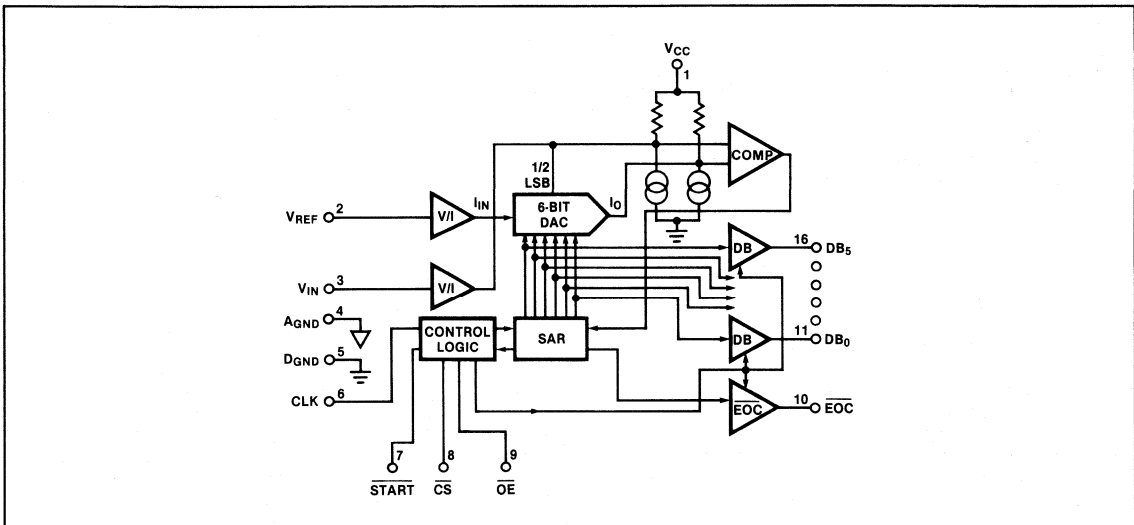


ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _{CC}	Power supply voltage	7	V
V _{REF}	Reference voltage	7	V
V _{IN (Analog)}	Analog input voltage	7	V
V _{IN (Digital)}	Digital input voltage (\overline{CS} , \overline{OE} , \overline{START} , CLK)	7	V
D _{OUT}	Data outputs (DB0 to DB5)		
	Three-state mode	7	V
	Enabled mode (each output)	5	mA
\overline{EOC}	End of conversion	V _{CC}	
Δ GND	Analog GND to digital GND	± 1	V
T _A	Operating temperature range	0 to 70	$^{\circ}$ C
T _{STG}	Storage temperature range	-65 to 150	$^{\circ}$ C
t _{SOLD}	Lead soldering temperature (10 seconds)	300	$^{\circ}$ C
P _D	Power dissipation		
	F package	220	mW
	N package	220	mW

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BLOCK DIAGRAM



6-BIT A/D CONVERTER (PARALLEL OUTPUTS)

NE5037

Preliminary

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V$; $V_{REF} = 2.0V$; Clock = 1MHz; $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified. Typical values are specified at $25^{\circ}C$.

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		6	6	6	Bits
Relative accuracy ^{1,2}			1/4	1/2	LSB
V_{CC} Positive supply voltage		+ 4.75	+ 5.0	+ 5.50	V
ϵ_{FS} Full scale gain error ^{2,3,4}	$V_{REF} = 2.0V$, $T_A = 25^{\circ}C$		± 1	± 2	LSB
ϵ_{ZS} Zero scale offset error ²	$V_{REF} = 2.0V$, $T_A = 25^{\circ}C$		$\pm 1/2$	- 1/2, + 2	LSB
P_{SR} Power supply rejection Max change in full scale ²	$V_{REF} = 2.0V$ $4.75V \leq V_{CC} \leq 5.5V$		$\pm 1/2$	± 1	LSB
I_{IN} Analog input bias current	$0 \leq V_{IN} \leq 2.5V$		1	10	μA
I_{REF} Reference bias current	$0 \leq V_{REF} \leq 2.5V$		1	10	μA
R_{IN} Analog input resistance		3	30		M Ω
V_{IH} Logic '1' input voltage		2.0			V
V_{IL} Logic '0' input voltage				0.8	V
I_{IH} Logic '1' input current				10	μA
I_{IL} Logic '0' input current				10	μA
I_{OH} Logic '1' output current ⁵	$2.4V \leq V_{OH}$	300			μA
I_{OL} Logic '0' output current ⁵	$V_{OL} \leq 0.4V$	1.6			mA
I_{OZ} Three-state leakage current				± 40	μA
I_{CC} Positive supply current			18	24	mA

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V$; $V_{REF} = 2.0V$; Clock = 1MHz; $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified. Typical values are specified at $25^{\circ}C$. (Refer to AC test figures.)

SYMBOL AND PARAMETER	TO	FROM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX} Maximum clock frequency				1			MHz
t_W Start pulse width						300	ns
Minimum positive/negative clock pulse width						300	ns
T_{CONV} Conversion time						9	Clock cycles
t_P (OUT DATA) Propagation delay ⁶	Data out	\overline{OE}	$T_A = 25^{\circ}C$, $t_r = t_f \leq 20ns$			500	ns
t_P (OUT EOC) Propagation delay ⁷	EOC	Clock	$T_A = 25^{\circ}C$, $t_r = t_f \leq 20ns$			800	ns
t_P (3-STATE) Propagation delay, 3-state	3-State Data	\overline{OE}	$T_A = 25^{\circ}C$, $t_r = t_f \leq 20ns$			500	ns

NOTES

- Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero scale to full scale of the device.
- Specifications given in LSB's refer to the weight of the least significant bit at the 6 bit level which is 1.56% of the full scale voltage.
- Full scale gain error is the deviation of the full scale code transition point (111110 to 111111) from its ideal value.
- The analog input voltage (V_{IN}) range is 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC} . (For optimum performance, V_{REF} can be any value from 1.5V to 2.5V.)
- The data outputs have active pull-ups. The \overline{EOC} line is open collector with a nominal 5k Ω internal pull-up resistor.
- Propagation delay of data outputs is defined as the delay in the data outputs reading their final value after the low going edge of \overline{OE} .
- Propagation delay of \overline{EOC} is defined as the delay in \overline{EOC} going low, following the low going edge of the 9th clock pulse after the start pulse.

CIRCUIT DESCRIPTION

NE5037 is a complete 6-bit, parallel output, microprocessor compatible, A/D converter which incorporates the successive approximation method. The chip includes the internal control logic, the successive approximation register (SAR), 6-bit DAC, comparator and output buffers. An externally generated clock source (max frequency = 1MHz) must be provided to pin 6.

An external reference voltage supplied to pin 2 sets the full scale range of the A/D converter.

The \overline{CS} pin must be at a low level prior to the start of the conversion process. Upon receipt of a \overline{START} pulse the internal control logic resets the SAR. On the first low going edge of the clock pulse, successive approximation conversion commences. Successive bits beginning with the MSB

(D5) are supplied to the input of the internal 6-bit current output DAC by the I²L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to '0' and simultaneously the corresponding

6-BIT A/D CONVERTER (PARALLEL OUTPUTS)

NE5037

Preliminary

output buffer goes to '0'. If it is less, that bit stays at '1' and the output buffer also stays at '1'. On successive clock pulses, successive bits of the DAC are tried and the corresponding output buffer represents the bits of the DAC. On the eighth low going edge of the clock pulse (after the receipt of the start pulse). The \overline{EOC} pin goes low, thereby indicating that the conversion is complete. The output data is now valid. In order to access the result of the conversion, the \overline{OE} pin must be set to a low level. \overline{EOC} is reset to a high state when \overline{OE} is low. When \overline{OE} is in a '1' state, the output buffers are in a high impedance state.

Refer to Figure 1 for the timing diagram.

TRANSFER CHARACTERISTICS

The ideal transfer characteristic of the NE5037 is shown in Figure 2.

The NE5037 is designed to have a nominal $\frac{1}{2}$ LSB offset so that the code transition points are located $\frac{1}{2}$ LSB on either side of the exact analog inputs for a given code.

Thus the first transition (000000 to 000001) will occur at an input of $\frac{1}{2}$ LSB (15.63mV with a V_{REF} of 2.0V). Subsequent transitions will occur at nominal increments of 1 LSB. The last transition (to full scale—111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

LAYOUT PRECAUTIONS

Analog ground (pin 4) and Digital ground (pin 5) are not connected internally and should be connected together as close to the device as possible, for optimum performance. The circuit will operate with as much as $\pm 200mV$ between the two grounds but some degradation will occur. The leads to the analog inputs should be kept as short as possible to minimize noise pickup. Input bypass capacitors from the analog inputs to ground will eliminate noise pickup. Power supplies should be decoupled with at least $1\mu F$ located close to the device to minimize noise spikes.

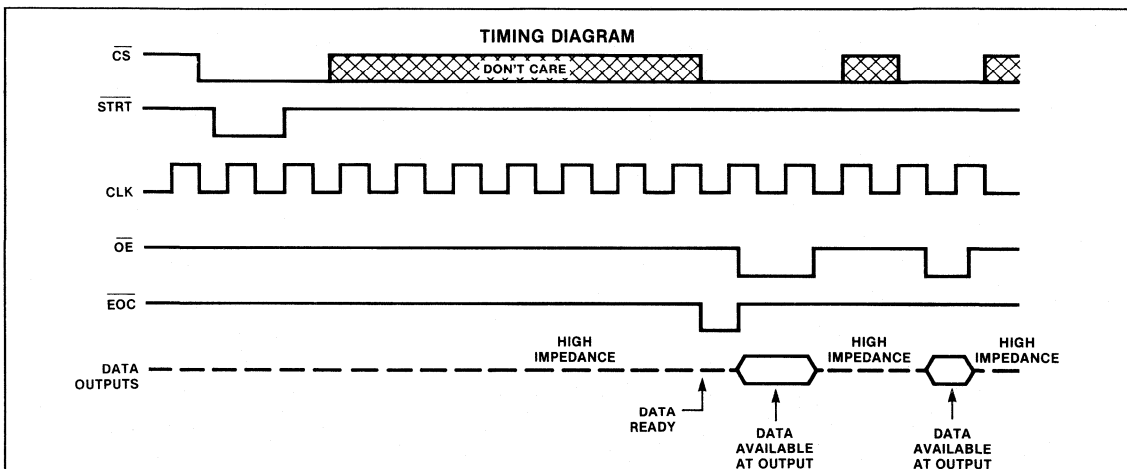


Figure 1

IDEAL TRANSFER CHARACTERISTICS

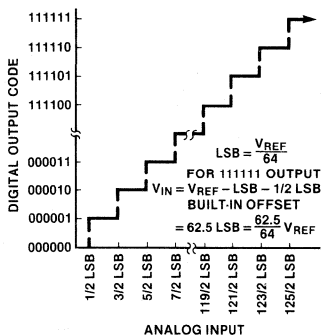


Figure 2

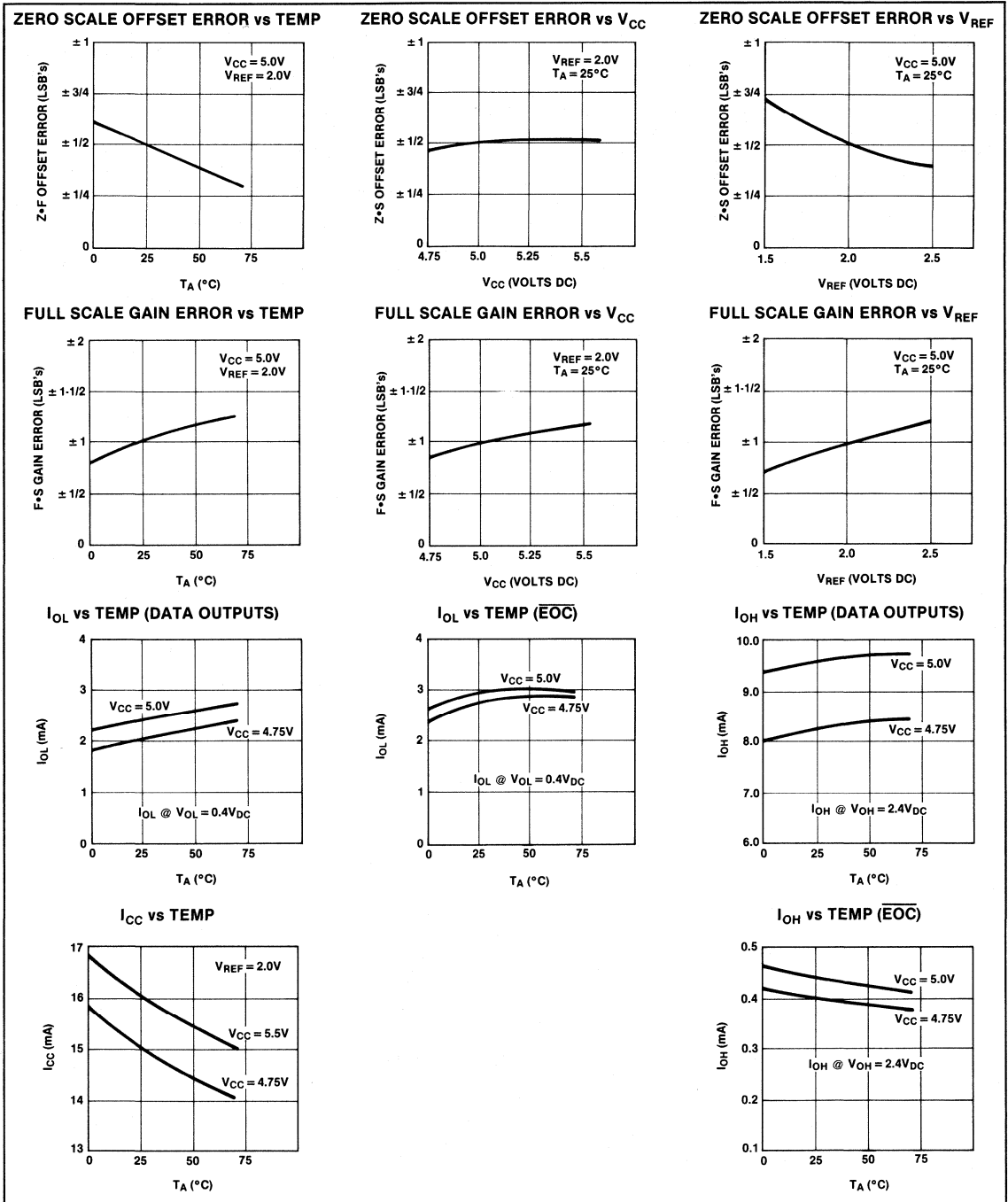
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6-BIT A/D CONVERTER (PARALLEL OUTPUTS)

NE5037

Preliminary

TYPICAL PERFORMANCE CHARACTERISTICS



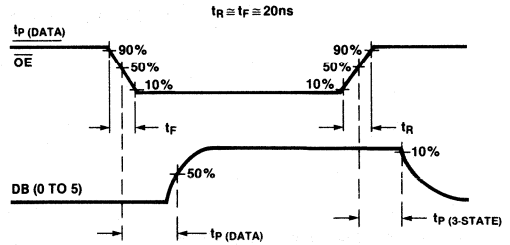
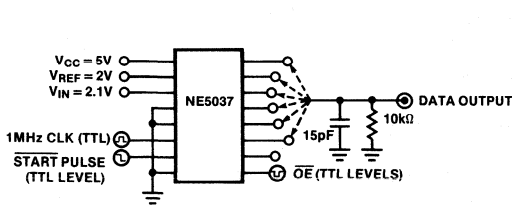
6-BIT A/D CONVERTER (PARALLEL OUTPUTS)

NE5037

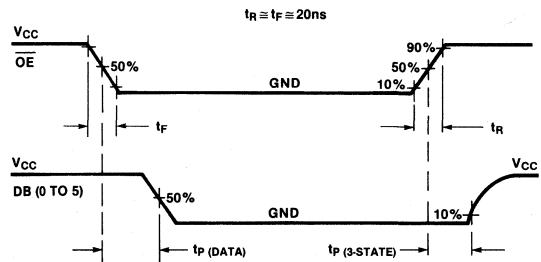
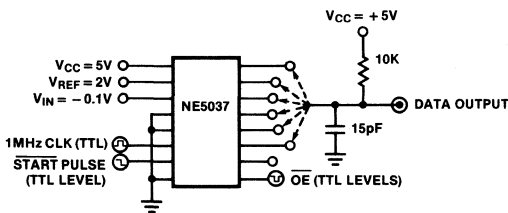
Preliminary

AC TEST CIRCUITS AND WAVEFORMS

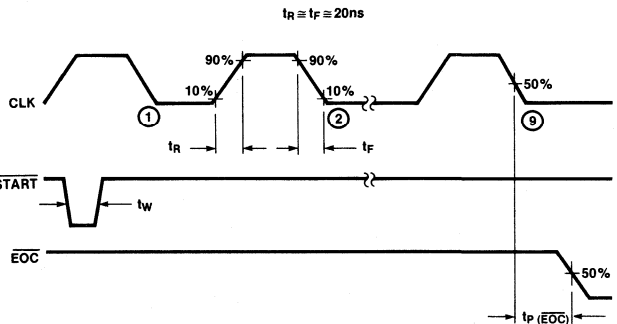
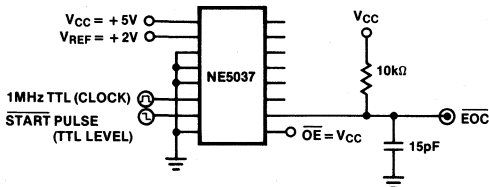
PROPAGATION DELAY TIME $t_{p(DATA)}$ AND $t_{p(3-STATE)}$



DATA OUTPUT HIGH



PROPAGATION DELAY TIME EOC $t_{p(EOC)}$



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8-BIT μ P-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT

NE/SE5118

DESCRIPTION

The NE5118 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the \overline{LE} input is in the low state. When \overline{LE} goes high, the input data present at the moment of transition is latched and retained until \overline{LE} again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

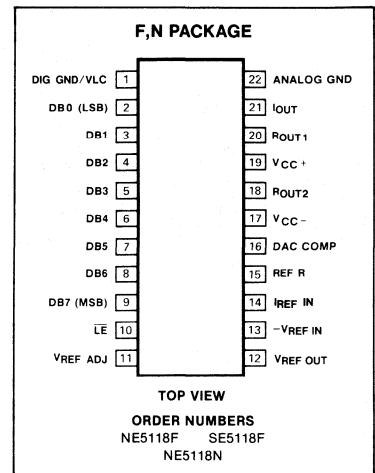
FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Fast settling output current—200ns
- Accurate to $\pm 1/2$ LSB (.19%)
- Monotonic to 8 bits
- Reference short-circuit protected
- Compatible with 8086, 6800 and many other μ P's

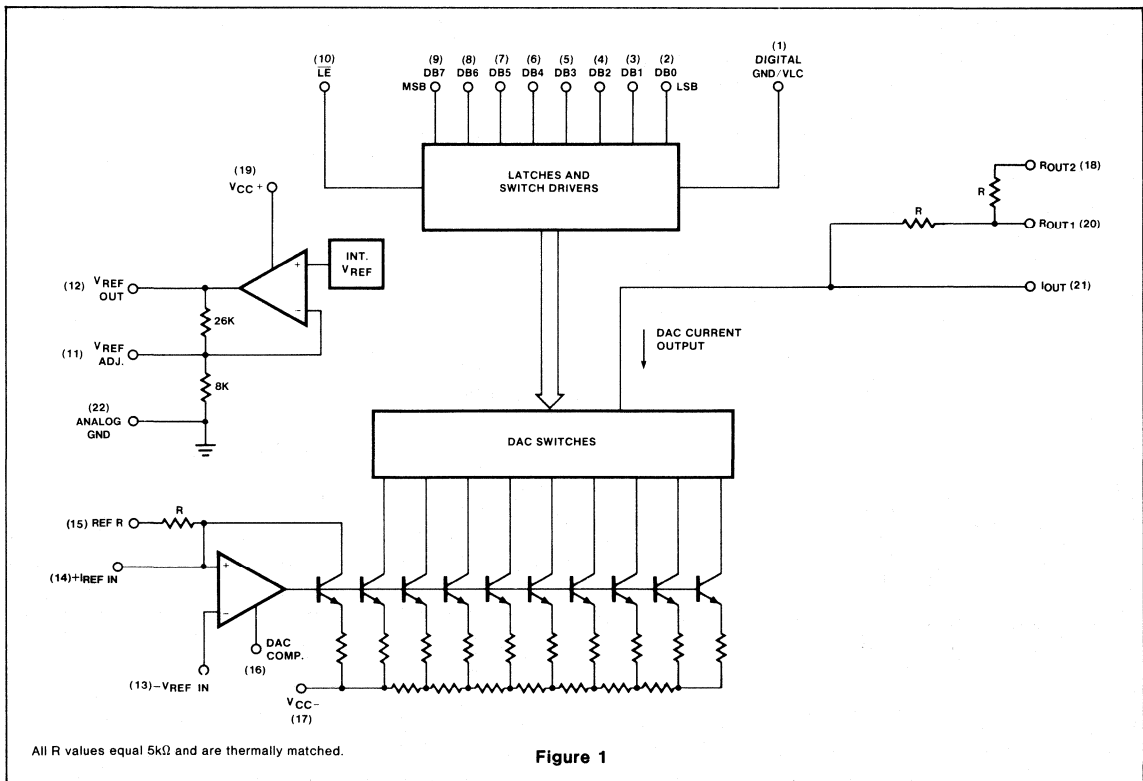
APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication
- CRT display drivers
- High-speed modems

PIN CONFIGURATION



BLOCK DIAGRAM



8-BIT μ P-COMPATIBLE D/A CONVERTER — CURRENT OUTPUT

NE/SE5118

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC+}	Positive supply voltage	18	V
V _{CC-}	Negative supply voltage	-18	V
V _{IN}	Logic input voltage	0 to 18	V
V _{REFIN}	Voltage at RREF input	12	V
V _{REFADJ}	Voltage at VREF adjust	0 to V _{REF}	V
V _{SUM}	Voltage at sum node	12	V
I _{REFSC}	Short-circuit current to ground at VREF OUT	Continuous	
I _{REFIN}	Reference input current (Pin 14)	3	mA
P _D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T _A	Operating temperature range		
	SE5118	-55 to +125	°C
	NE5118	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C
 For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS V_{CC+} = +15V, V_{CC-} = -15V, SE5118. -55°C ≤ T_A ≤ 125°C,
 NE5118. 0°C ≤ T_A ≤ 70°C unless otherwise specified.
 Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE5118			NE5118			UNIT
		Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Relative accuracy				±0.19			±0.19	%FS
V _{CC+}	Positive supply voltage	11.4	15		11.4	15		V
V _{CC-}	Negative supply voltage	-11.4	-15		-11.4	-15		V
V _{IN(1)}	Logic "1" input voltage	2.0			2.0			V
V _{IN(0)}	Logic "0" input voltage			0.8			0.8	V
I _{IN(1)}	Logic "1" input current		0.1	10		0.1	10	μA
I _{IN(0)}	Logic "0" input current		-2.0	-10		-2.0	-10	μA
I _{FS}	Full scale output current	1.90	1.992	2.10	1.90	1.992	2.10	mA
I _{ZS}	Zero scale current	-6	1	+6	-6	1	+6	μA
V _{REF}	Reference voltage	4.9	5.0	5.25	4.9	5.0	5.25	V
PSR ⁺ (out)	Output power supply rejection (+)	V ₋ = -15V, 13.5V ≤ V ₊ ≤ 16.5V, external V _{REF IN} = 5.000V				.001	.01	%FS/ %VS
PSR ⁻ (out)	Output power supply rejection (-)	V ₊ = 15V, -13.5V ≤ V ₋ ≤ -16.5V, external V _{REF IN} = 5.000V				.001	.01	%FS/ %VS
TC _{FS}	Full scale temperature coefficient	V _{REF IN} = 5.000V ¹				20		ppm/°C
TC _{ZS}	Zero scale temperature coefficient	I _{REF IN} = 1.00mA ²				5		ppm/°C

NOTES

1. This is for voltage out only. See Unipolar Voltage Output schematic.
2. This is for current output mode.

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8-BIT μ P-COMPATIBLE D/A CONVERTER — CURRENT OUTPUT

NE/SE5118

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC+} = +15V$, $V_{CC-} = -15V$, SE5118. $-55^{\circ}C \leq T_A \leq 125^{\circ}C$,
NE5118. $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified.
Typical values are specified at $25^{\circ}C$

PARAMETER	TEST CONDITIONS	SE5118			NE5118			UNIT		
		Min	Typ	Max	Min	Typ	Max			
I_{REF} I_{REFSC}	Reference output current Reference short circuit current	Note 1 $T_A = 25^{\circ}C$ $V_{REF OUT} = 0V$			15	3 30		15	3 30	mA mA
PSR+(REF)	Reference power supply rejection (+)	$V^- = -15V$, $13.5V \leq V^+ \leq 16.5V$, $I_{REF} = 1.0mA$.003	.01		.003	.01	%VR / %VS
PSR-(REF)	Reference power supply rejection (-)	$V^+ = 15V$, $-13.5V \leq V^- \leq 16.5V$, $I_{REF} = 1.0mA$.003	.01		.003	.01	%VR / %VS
TCREF	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$			60			60		ppm/ $^{\circ}C$
Z_{IN}	DAC R_{REFIN} input impedance				5.0			5.0		k Ω
I_{CC+}	Positive supply current	$V_{CC+} = 15V$			7	14		7	14	mA
I_{CC-}	Negative supply current	$V_{CC-} = -15V$			-10	-15		-10	-15	mA
P_D	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$			255	435		255	435	mW

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25^{\circ}C$

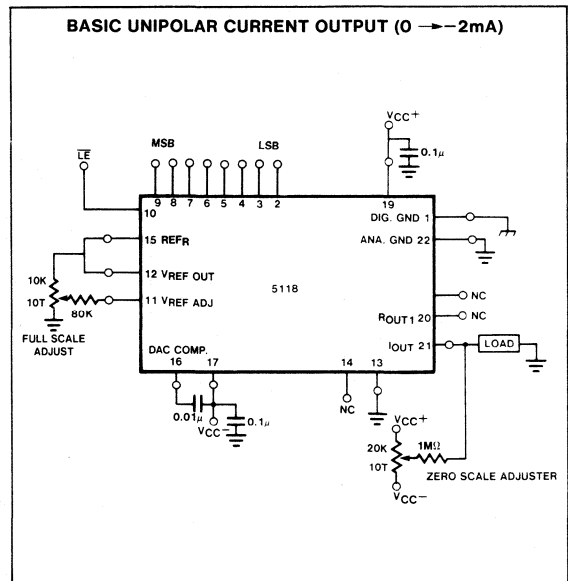
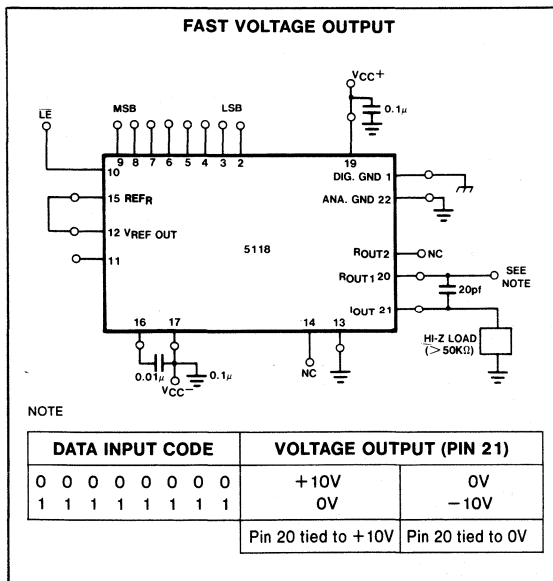
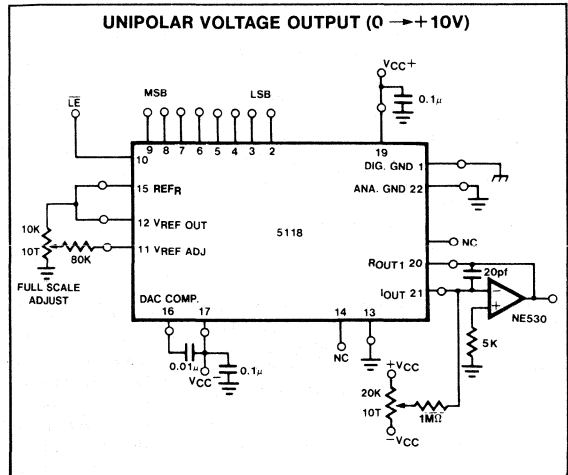
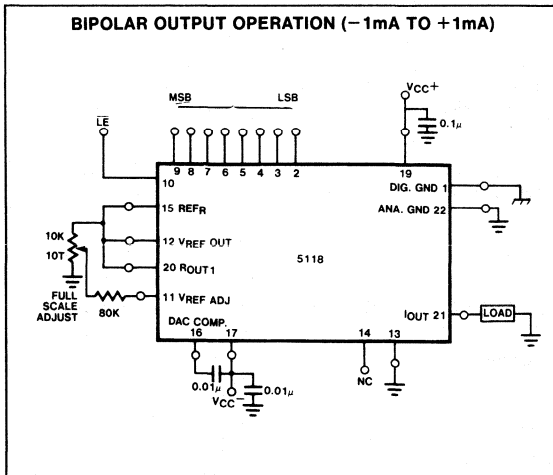
PARAMETER	TO	FROM	TEST CONDITIONS	SE/NE5118			UNIT
				Min	Typ	Max	
T_{SLH}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits Low-to-high			ns
T_{SHL}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits High-to-low			ns
t_{PLH}	Propagation delay	Output	Input	All bits switched Low-to-high			60
t_{PHL}	Propagation delay	Output	Input	All bits switched High-to-low			60
t_{PLSB}	Propagation delay	Output	Input	1 LSB change			60
t_{PLH}	Propagation delay	Output	\overline{LE}	Low-to-high transition			60
t_{PHL}	Propagation delay	Output	\overline{LE}	High-to-low transition			60
t_s	Set-up time	\overline{LE}	Input				100
t_h	Hold time	Input	\overline{LE}				50
t_{pw}	Latch enable pulse width						150

NOTES

1. For reference currents $> 3mA$, use of an external buffer is required.

8-BIT μ P-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT

NE/SE5118



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8-BIT μ P-COMPATIBLE D/A CONVERTER — CURRENT OUTPUT

NE/SE5119

DESCRIPTION

The NE5119 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the \overline{LE} input is in the low state. When \overline{LE} goes high, the input data present at the moment of transition is latched and retained until \overline{LE} again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

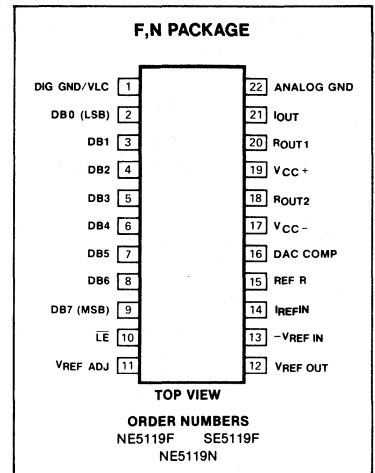
FEATURES

- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Fast settling output current — 200ns
- Accurate to $\pm 1/4$ LSB (.1%)
- Monotonic to 8 bits
- Reference short-circuit protected
- Compatible with 8086, 6800 and many other μ P's

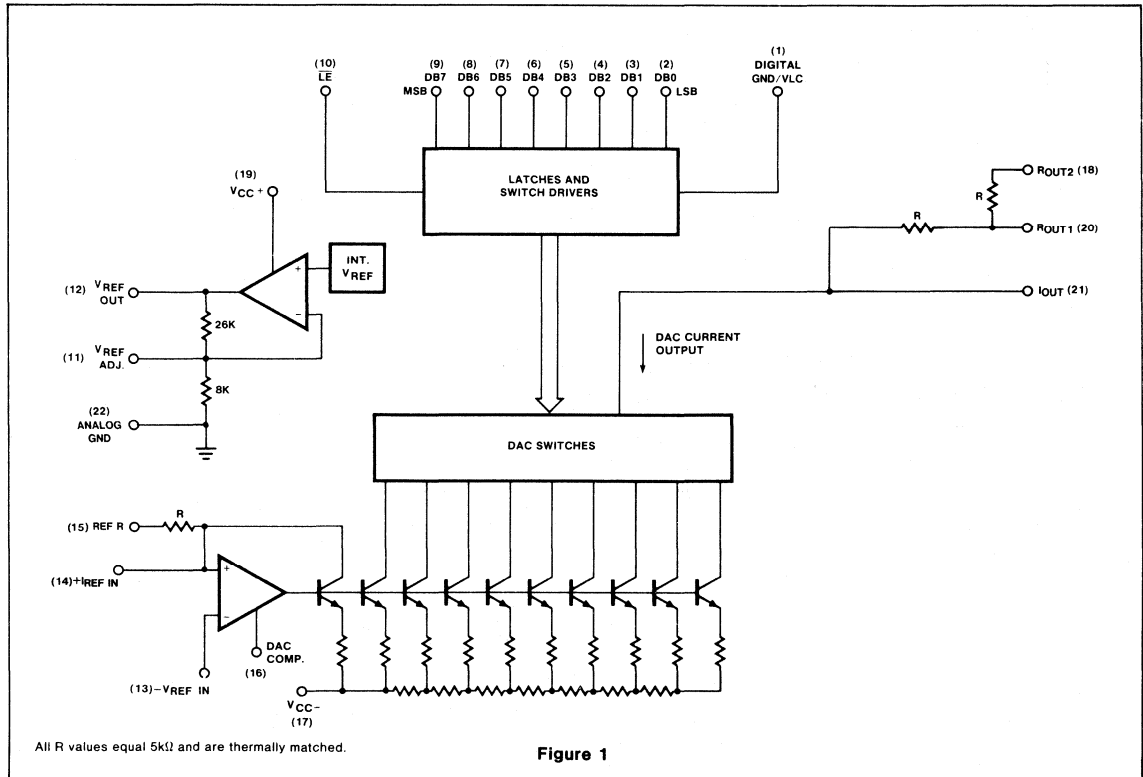
APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication
- CRT display drivers
- High-speed modems

PIN CONFIGURATION



BLOCK DIAGRAM



8-BIT μ P-COMPATIBLE D/A CONVERTER—CURRENT OUTPUT

NE/SE5119

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC+}	Positive supply voltage	18	V
V _{CC-}	Negative supply voltage	-18	V
V _{IN}	Logic input voltage	0 to 18	V
V _{REFIN}	Voltage at R _{REF} input	12	V
V _{REFADJ}	Voltage at V _{REF} adjust	0 to V _{REF}	V
V _{SUM}	Voltage at sum node	12	V
I _{REFSC}	Short-circuit current to ground at V _{REF} OUT	Continuous	
I _{REFIN}	Reference input current (Pin 14)	3	mA
P _D	Power dissipation*		
	-N package	800	mW
	-F package	1000	mW
T _A	Operating temperature range		
	SE5119	-55 to +125	°C
	NE5119	0 to +70	°C
T _{STG}	Storage temperature range	-65 to +150	°C
T _{SOLD}	Lead soldering temperature (10 seconds)	300	°C

*NOTES

For N package, derate at 120°C/W above 35°C

For F package, derate at 75°C/W above 75°C

DC ELECTRICAL CHARACTERISTICS V_{CC+} = +15V, V_{CC-} = -15V, SE5119. -55°C ≤ T_A ≤ 125°C, NE5119. 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C

PARAMETER	TEST CONDITIONS	SE5119			NE5119			UNIT
		Min	Typ	Max	Min	Typ	Max	
Resolution		8	8	8	8	8	8	Bits
Monotonicity		8	8	8	8	8	8	Bits
Relative accuracy				±0.1			±0.1	%FS
V _{CC+}	Positive supply voltage	11.4	15		11.4	15		V
V _{CC-}	Negative supply voltage	-11.4	-15		-11.4	-15		V
V _{IN(1)}	Logic "1" input voltage	2.0			2.0			V
V _{IN(0)}	Logic "0" input voltage			0.8			0.8	V
I _{IN(1)}	Logic "1" input current		0.1	10		0.1	10	μA
I _{IN(0)}	Logic "0" input current		-2.0	-10		-2.0	-10	μA
I _{FS}	Full scale output current	1.90	1.992	2.10	1.90	1.992	2.10	mA
I _{ZS}	Zero scale current		1			1		μA
V _{REF}	Reference voltage	4.9	5.0	5.25	4.9	5.0	5.25	V
PSR ⁺ (out)	Output power supply rejection (+)		.001	.01		.001	.01	%FS / %VS
PSR ⁻ (out)	Output power supply rejection (-)		.001	.01		.001	.01	%FS / %VS
TC _{FS}	Full scale temperature coefficient		20			20		ppm / °C
TC _{ZS}	Zero scale temperature coefficient		5			5		ppm / °C

NOTES

1. This is for voltage out only. See Unipolar Voltage Output schematic

2. This is for current output mode

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8-BIT μ P-COMPATIBLE D/A CONVERTER — CURRENT OUTPUT

NE/SE5119

DC ELECTRICAL CHARACTERISTICS (Cont'd) $V_{CC+} = +15V$, $V_{CC-} = -15V$, SE5119, $-55^{\circ}C \leq T_A \leq 125^{\circ}C$,
NE5119, $0^{\circ}C \leq T_A \leq 70^{\circ}C$ unless otherwise specified.
Typical values are specified at $25^{\circ}C$

PARAMETER	TEST CONDITIONS	SE5119			NE5119			UNIT		
		Min	Typ	Max	Min	Typ	Max			
I_{REF} I_{REFSC}	Reference output current Reference short circuit current	Note 1 $T_A = 25^{\circ}C$ $V_{REF OUT} = 0V$				15	3 30		mA mA	
PSR+(REF)	Reference power supply rejection (+)	$V_{-} = -15V$, $13.5V \leq V_{+} \leq 16.5V$, $I_{REF} = 1.0mA$.003	.01		%VR/ %VS	
PSR-(REF)	Reference power supply rejection (-)	$V_{+} = 15V$, $-13.5V \leq V_{-} \leq 16.5V$, $I_{REF} = 1.0mA$.003	.01		%VR/ %VS	
TCREF	Reference voltage temperature coefficient	$I_{REF} = 1.0mA$				60		60	ppm/ $^{\circ}C$	
Z_{IN}	DAC R_{REFIN} input impedance					5.0		5.0	k Ω	
I_{CC+}	Positive supply current	$V_{CC+} = 15V$				7	14	7	14	mA
I_{CC-}	Negative supply current	$V_{CC-} = -15V$				-10	-15	-10	-15	mA
PD	Power dissipation	$I_{REF} = 1.0mA$, $V_{CC} = \pm 15V$				255	435	255	435	mW

AC ELECTRICAL CHARACTERISTICS $V_{CC} = \pm 15V$, $T_A = 25^{\circ}C$

PARAMETER	TO	FROM	TEST CONDITIONS	SE/NE5119			UNIT
				Min	Typ	Max	
T_{SLH}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits Low-to-high			ns
T_{SHL}	Settling time	$\pm \frac{1}{2}$ LSB	Input	All bits High-to-low			ns
tPLH	Propagation delay	Output	Input	All bits switched Low-to-high			60
tPHL	Propagation delay	Output	Input	All bits switched High-to-low			60
tPLSB	Propagation delay	Output	Input	1 LSB change			60
tPLH	Propagation delay	Output	\overline{LE}	Low-to-high transition			60
tPHL	Propagation delay	Output	\overline{LE}	High-to-low transition			60
t_s	Set-up time	\overline{LE}	Input				100
t_h	Hold time	Input	\overline{LE}				50
t_{pw}	Latch enable pulse width						150

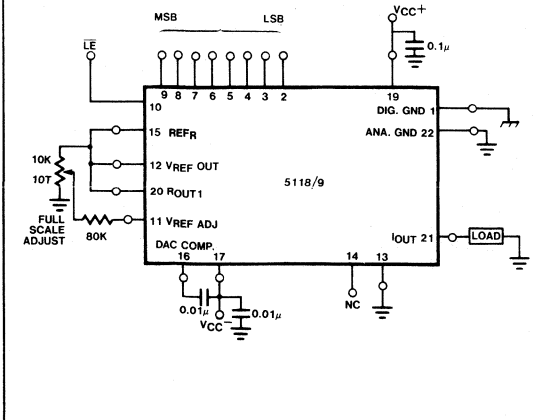
NOTES

1. For reference currents $> 3mA$, use of an external buffer is required.

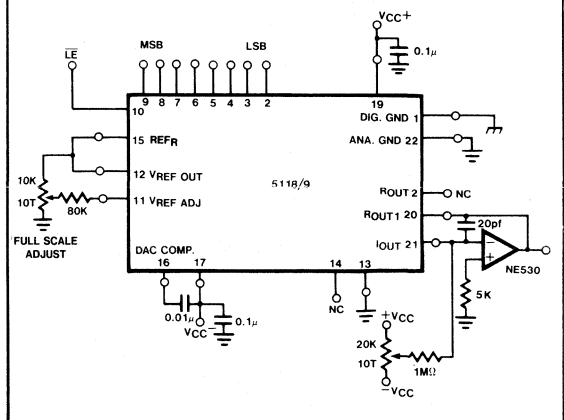
8-BIT μ P-COMPATIBLE D/A CONVERTER — CURRENT OUTPUT

NE/SE5119

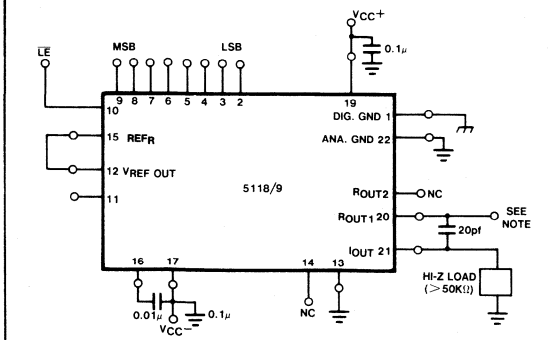
BIPOLAR OUTPUT OPERATION (-1mA TO +1mA)



UNIPOLAR VOLTAGE OUTPUT (0 → +10V)



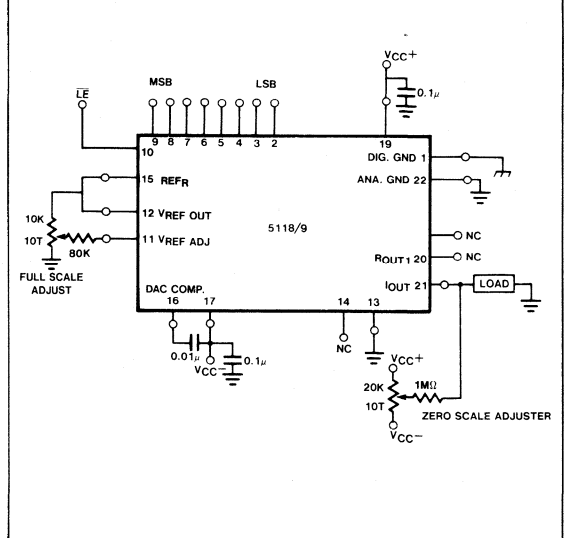
FAST VOLTAGE OUTPUT



NOTE

DATA INPUT CODE	VOLTAGE OUTPUT (PIN 21)	
0 0 0 0 0 0 0 0	+10V	0V
1 1 1 1 1 1 1 1	0V	-10V
	Pin 20 tied to +10V	Pin 20 tied to 0V

BASIC UNIPOLAR CURRENT OUTPUT (0 → -2mA)



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Section 12

Sample and Hold Circuits

INDEX

Section 12 — Sample and Hold Circuits

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LF398 Monolithic Sample and Hold Circuit	12-5
NE/SE5537 Sample and Hold Amplifier	12-9

SAMPLE AND HOLD CIRCUITS—SYMBOLS AND DEFINITIONS

Acquisition Time

The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

Aperture Delay Time

The time elapsed from the hold command to the opening of the switch.

Aperture Jitter

Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

Aperture Time

The delay required between "hold" command and an input analog transition, so that the transition does not affect the hold output.

Effective Aperture Delay

The time difference between the hold command and the time at which the input signal is at the held voltage.

Figure Of Merit

The ratio of the available charging current during sample mode to the leakage current during hold mode.

Hold-Mode Droop

The output voltage change per unit of time while in hold. Commonly specified in V/s, $\mu\text{V}/\mu\text{s}$ or other convenient units.

Hold-Mode Feed Through

The percentage of an input sinusoidal signal that is measured at the output of a sample-and-hold when it's in hold mode.

Hold Settling Time

The time required for the output to settle within 1mV of final value after the "hold" logic command.

Sample-To-Hold Offset Error

The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

Slew Rate

The fastest rate at which the sample & hold output can change (specified in V/ μs).

Hold Step

The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

Dynamic Sampling Error

The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

Gain Error

The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

Threshold

Level shall be defined as that level which causes the switch control to change state.

MONOLITHIC SAMPLE AND HOLD CIRCUIT

LF398

DESCRIPTION

The Signetics LF398 is a monolithic sample and hold circuit which utilizes high-voltage Ion-Implant JFET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.004% typical and acquisition time is as low as 6 μ s to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin and does not degrade input offset drift. The wide bandwidth allows the LF398 to be included inside the feedback loop of 1MHz op amps without having stability problems. Input impedance of 10¹⁰ Ω allows high source impedances to be used without degrading accuracy.

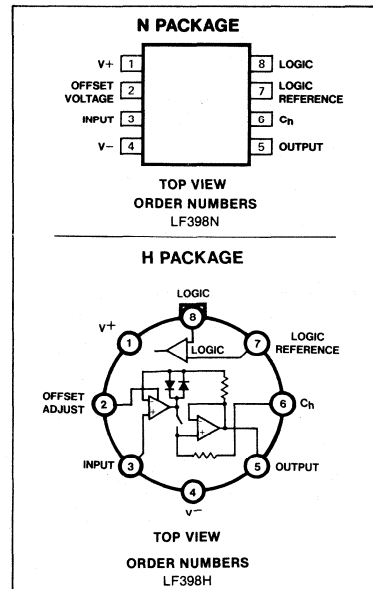
P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5mV/min with a 1 μ F hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode even for input signals equal to the supply voltages.

Logic inputs on the LF398 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF398 will operate from $\pm 5V$ to $\pm 18V$ supplies. It is available in an 8-lead TO-5 package or an 8-pin plastic DIP.

FEATURES

- Operates from $\pm 5V$ to $\pm 18V$ supplies
- Less than 10 μ s acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at $C_h = 0.01\mu F$
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change
 - during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth
- The LF398 is ideally suited for a wide variety of sample and hold applications including data acquisition, analog to digital conversion, synchronous demodulation, and automatic test setup.

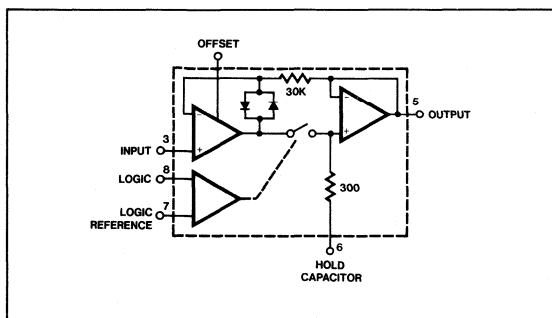
PIN CONFIGURATION



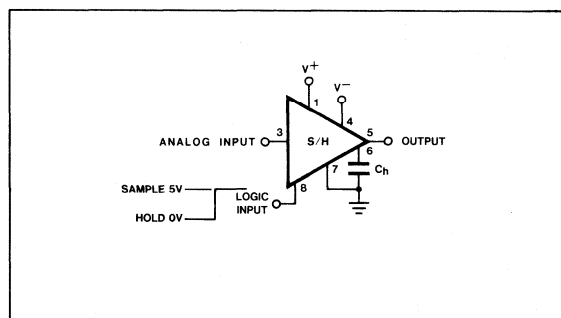
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	± 18	V
Power dissipation (package limitation) ¹	500	mW
Operating ambient temperature range LF398	0 to +70	$^{\circ}C$
Storage temperature range	-65 to +150	$^{\circ}C$
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage ²	+7, -30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	$^{\circ}C$

FUNCTIONAL DIAGRAM



TYPICAL APPLICATIONS



MONOLITHIC SAMPLE AND HOLD CIRCUIT

LF398

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25^\circ C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.

PARAMETER	TEST CONDITIONS	LF398			UNIT
		Min	Typ	Max	
Input offset voltage ⁶	$T_j = 25^\circ C$		2	7	mV
	Full temperature range			10	mV
Input bias current ⁶	$T_j = 25^\circ C$		10	50	nA
	Full temperature range			100	nA
Input impedance	$T_j = 25^\circ C$		10^{10}		Ω
Gain error	$T_j = 25^\circ C$, $R_L = 10K$		0.004	0.01	%
	Full temperature range			0.02	%
Feedthrough attenuation ratio at 1kHz	$T_j = 25^\circ C$, $C_h = 0.01\mu F$	80	90		dB
Output impedance	$T_j = 25^\circ C$, "HOLD" mode		0.5	4	Ω
	Full temperature range			6	Ω
"HOLD" step ⁴ Supply current ⁶	$T_j = 25^\circ C$, $C_h = 0.01\mu F$, $V_{OUT} = 0$		1.0	2.5	mV
	$T_j \geq 25^\circ C$		4.5	6.5	mA
Logic and logic reference input current	$T_j = 25^\circ C$		2	10	μA
Leakage current into hold capacitor ⁵	$T_j = 25^\circ C^5$		30	200	pA
	Hold mode				
Acquisition time to 0.1%	$\Delta V_{OUT} = 10V$, $C_h = 1000pF$		4		μs
	$C_h = 0.01\mu F$		20		μs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2V$		5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		dB
Differential logic threshold	$T_j = 25^\circ C$	0.8	1.4	2.4	V

NOTES

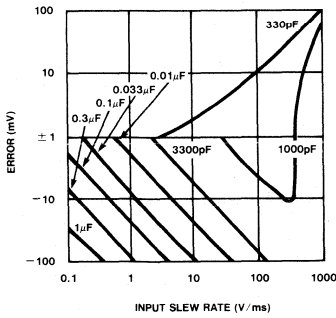
1. The maximum junction temperature of the LF398 is $150^\circ C$. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θ_{JA}) of $150^\circ C/W$.
2. Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.
3. Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15V$, $T_j = 25^\circ C$, $-11.5V \leq V_{IN} \leq +11.5V$, $C_h = 0.01\mu F$, and $R_L = 10k$. Logic reference voltage = 0V and logic voltage = 2.5V.
4. Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01 μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
5. Leakage current is measured at a junction temperature of $25^\circ C$. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the $25^\circ C$ value for each $11^\circ C$ increase in chip temperature. Leakage is guaranteed over full input signal range.
6. The parameters guaranteed over a supply voltage of ± 5 to $\pm 18V$.

MONOLITHIC SAMPLE AND HOLD CIRCUIT

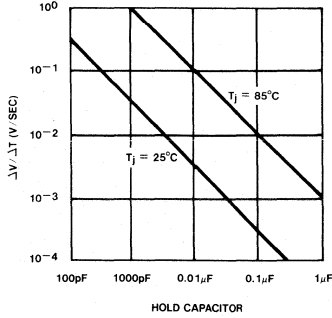
LF398

TYPICAL AC PERFORMANCE CHARACTERISTICS (cont'd)

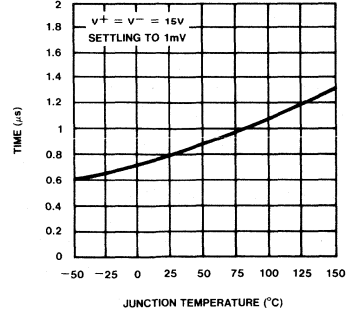
DYNAMIC SAMPLING ERROR



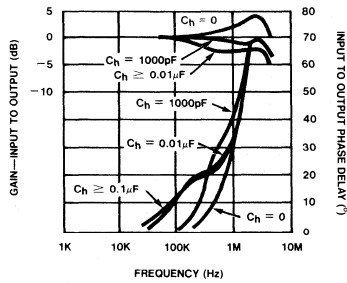
OUTPUT DROOP RATE



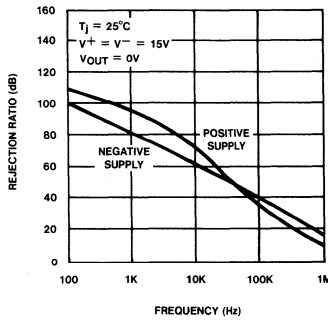
"HOLD" SETTLING TIME



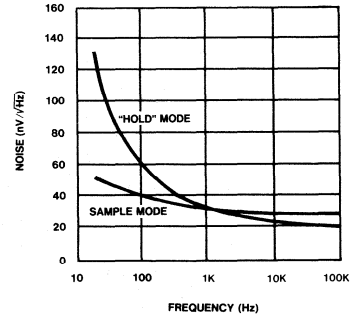
PHASE AND GAIN (INPUT TO OUTPUT, SMALL SIGNAL)



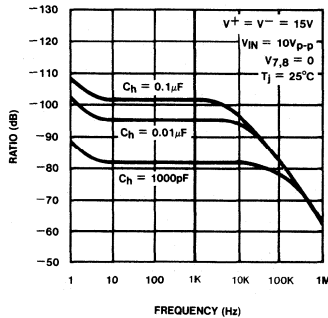
POWER SUPPLY REJECTION



OUTPUT NOISE



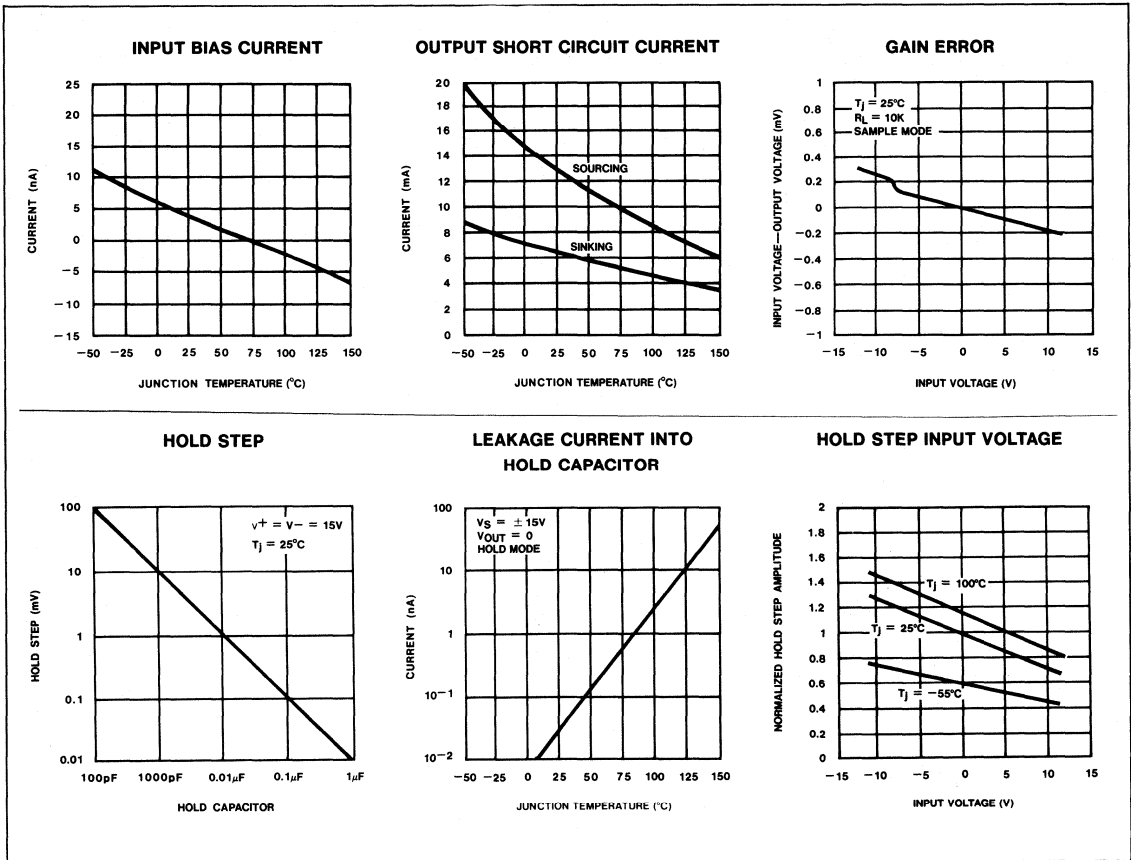
FEEDTHROUGH REJECTION RATIO (HOLD MODE)



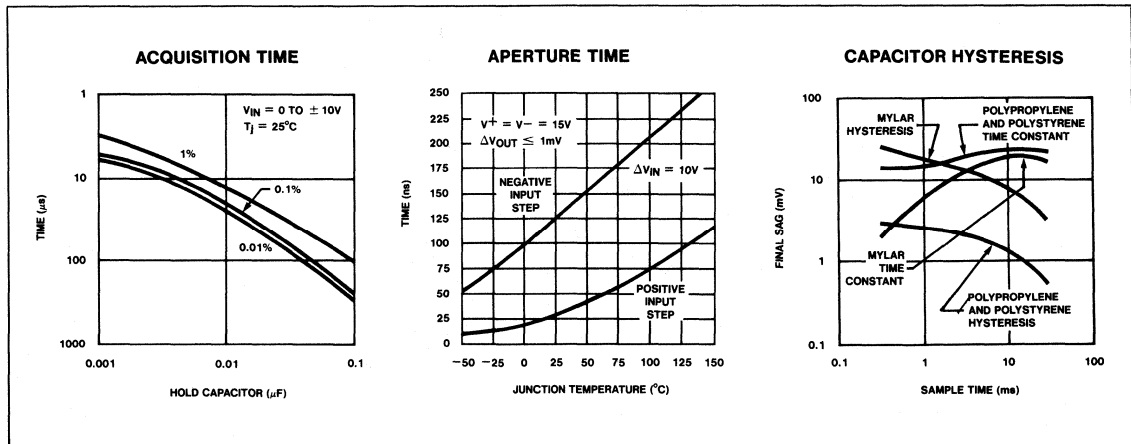
MONOLITHIC SAMPLE AND HOLD CIRCUIT

LF398

TYPICAL DC PERFORMANCE CHARACTERISTICS



TYPICAL AC PERFORMANCE CHARACTERISTICS



SAMPLE AND HOLD AMPLIFIER

NE/SE5537

DESCRIPTION

The NE5537 monolithic Sample and Hold amplifier combines the best features of an implanted JFET's with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin compatible with the LF198, and features superior performance in droop rate and output drive capability. The circuit shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the Sample mode. The first amplifier has bipolar input transistors which gives the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2KΩ load. The logic input is compati-

ble with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the Sample mode occurring when the logic input is high. It is available in 8-lead TO-5 and 8-pin plastic DIP packages.

FEATURES

- Operates from ±5V to ±18V supplies
- Hold leakage current 6pA @ T_j25°C
- Less than 10μs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5mV typical hold step at C_h = 0.01μF
- Low input offset: 1MV (typical)
- 0.002% gain accuracy with R_L = 2kΩ
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	± 18	V
Power dissipation (package limitation) ¹	500	mW
Operating ambient temperature range		
SE5537	-55 to +125	°C
NE5537	0 to +70	°C
Storage temperature range	-65 to +150	°C
Input voltage	Equal to supply voltage	
Logic to logic reference differential voltage ²	+7, -30	V
Output short circuit duration	Indefinite	
Hold capacitor short circuit duration	10	sec
Lead temperature (soldering, 10sec)	300	°C

NOTES

1. The maximum junction temperature of the SE5537 is 150°C and for the NE5537 is 100°C. When operating at elevated ambient temperature, the TO-5 and plastic DIP packages must be derated based on a thermal resistance (θ_{ja}) of 150°C/W.
2. Although the differential voltage may not exceed the limits given, the common mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

BLOCK DIAGRAM

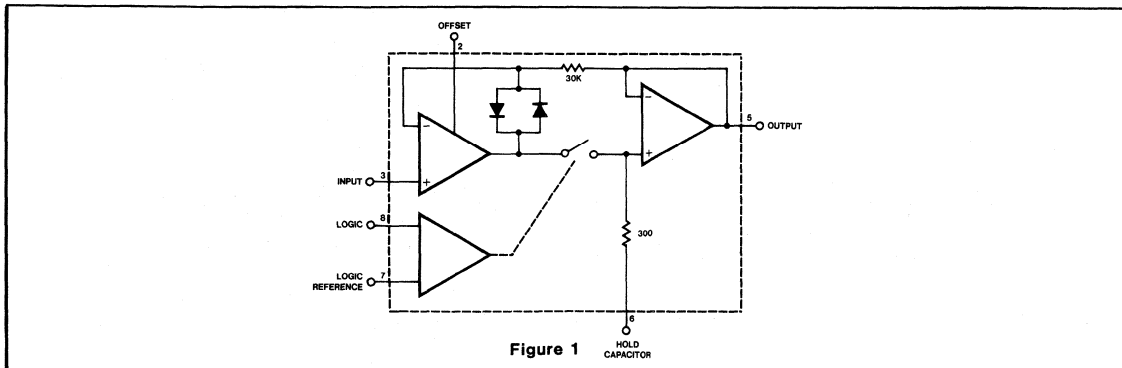
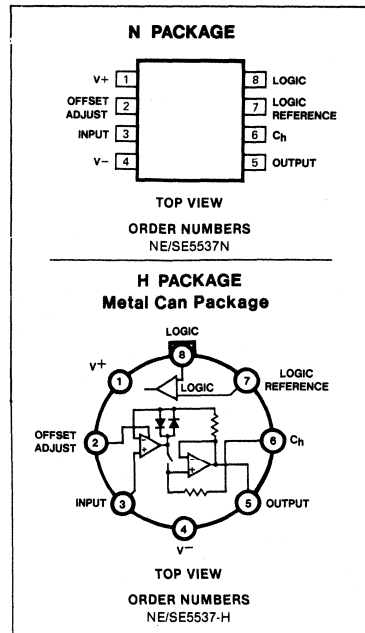


Figure 1

PIN CONFIGURATION



SAMPLE AND HOLD AMPLIFIER

NE/SE5537

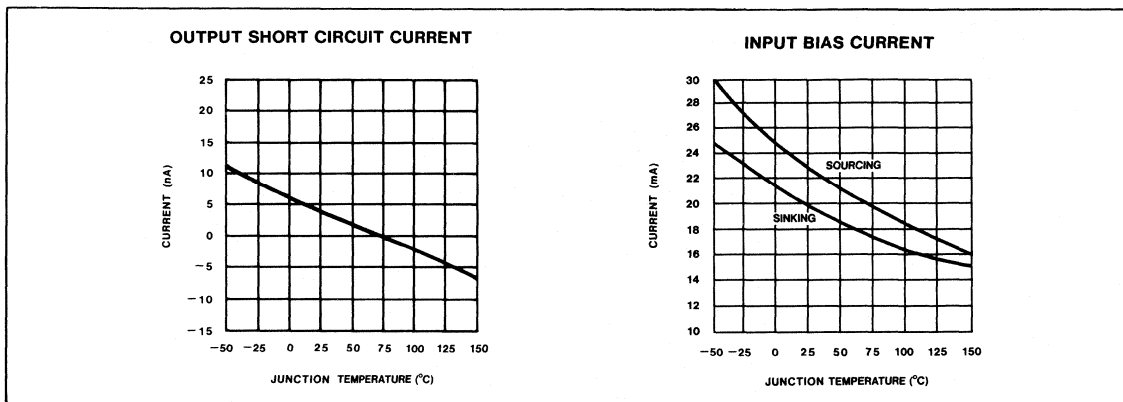
ELECTRICAL CHARACTERISTICS³

PARAMETER	TEST CONDITIONS	SE5537			NE5537			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage ⁶	$T_j = 25^\circ\text{C}$ Full temperature range		1	3 5		2	7 10	mV mV
Input bias current ⁶	$T_j = 25^\circ\text{C}$ Full temperature range		5	25 75		10	50 100	nA nA
Input impedance	$T_j = 25^\circ\text{C}$		10^{10}			10^{10}		Ω
Gain error	$T_j = 25^\circ\text{C}$, $-10\text{V} \leq V_{IN} \leq 10\text{V}$, $R_L = 2\text{K}$ $-11.5\text{V} \leq V_{IN} \leq 11.5\text{V}$, $R_L = 10\text{K}$ Full temperature range		0.002	0.007		0.004	0.01	%
				0.02			0.02	%
Feedthrough attenuation ratio at 1kHz	$T_j = 25^\circ\text{C}$, $C_h = 0.01\mu\text{F}$	86	96		80	90		dB
Output impedance	$T_j = 25^\circ\text{C}$, "HOLD" mode full temperature range		0.5	2 4		0.5	4 6	Ω
"HOLD" Step ⁴	$T_j = 25^\circ\text{C}$, $C_h = 0.01\mu\text{F}$, $V_{OUT} = 0$		0.5	2.0		1.0	2.5	mV
Supply current ⁶	$T_j = 25^\circ\text{C}$		4.5	6.5		4.5	7.5	mA
Logic and logic reference input current	$T_j = 25^\circ\text{C}$		2	10		2	10	μA
Leakage current into hold capacitor ⁶	$T_j = 25^\circ\text{C}$ hold mode ⁵		6	50		6	100	pA
Acquisition time to 0.1%	$V_{OUT} = 10\text{V}$, $C_h = 1000\text{pF}$ $C_h = 0.01\mu\text{f}$		4			4		μs
			20			20		μs
Hold capacitor charging current	$V_{IN} - V_{OUT} = 2\text{V}$		5			5		mA
Supply voltage rejection ratio	$V_{OUT} = 0$	80	110		80	110		dB
Differential logic threshold	$T_j = 25^\circ\text{C}$	0.8	1.4	2.4	0.8	1.4	2.4	V

NOTES

- Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, $V_S = \pm 15\text{V}$, $T_j = 25^\circ\text{C}$, $-11.5\text{V} \leq V_{IN} \leq 11.5\text{V}$, $C_h = 0.01\mu\text{F}$, and $R_L = 2\text{k}\Omega$. Logic reference voltage = 0V and logic voltage = 2.5V.
- Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1pF, for instance, will create an additional 0.5mV step with a 5V logic swing and a 0.01F hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.
- Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.
- These parameters guaranteed over a supply voltage range of ± 5 to $\pm 18\text{V}$.

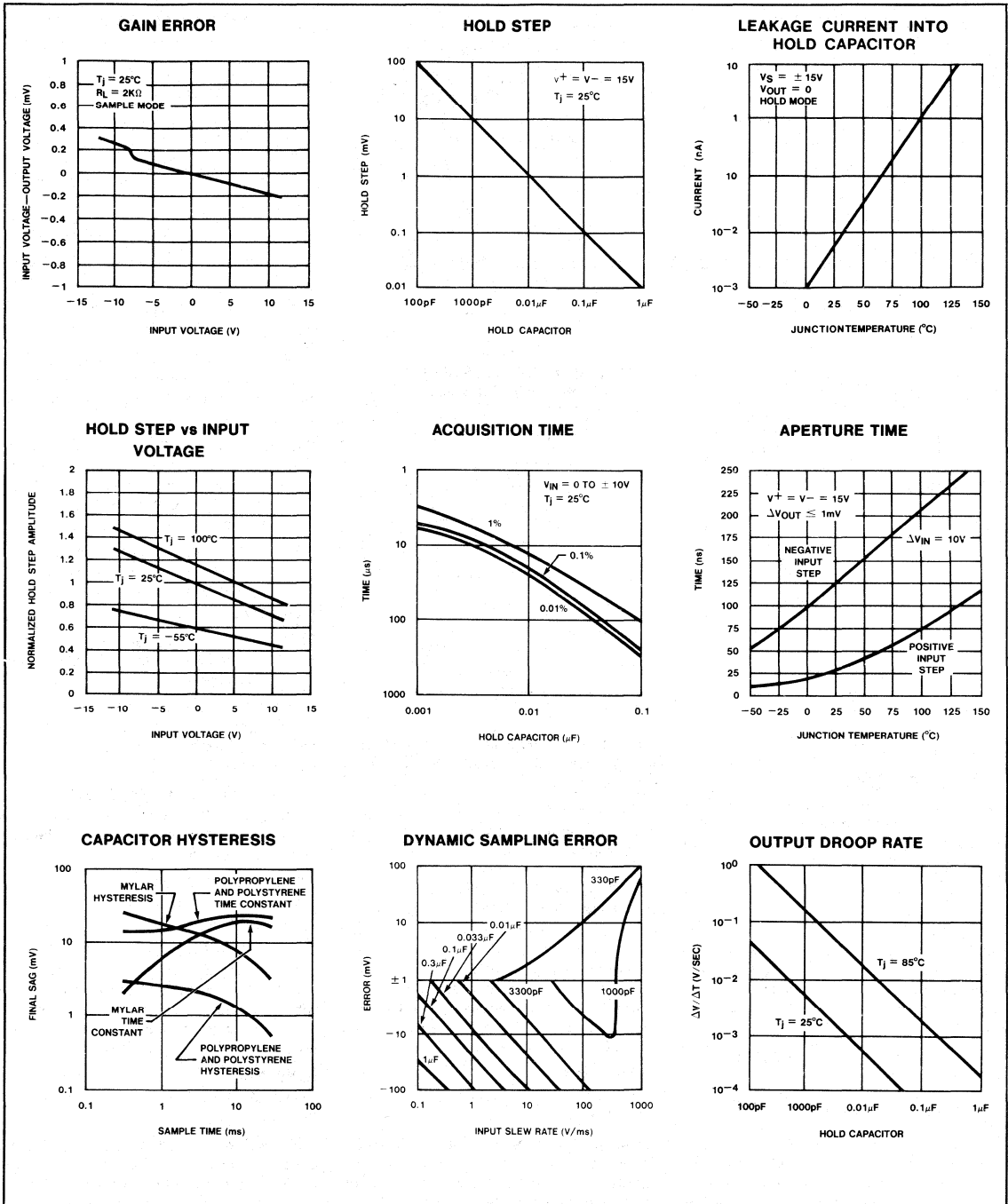
TYPICAL PERFORMANCE CHARACTERISTICS



SAMPLE AND HOLD AMPLIFIER

NE/SE5537

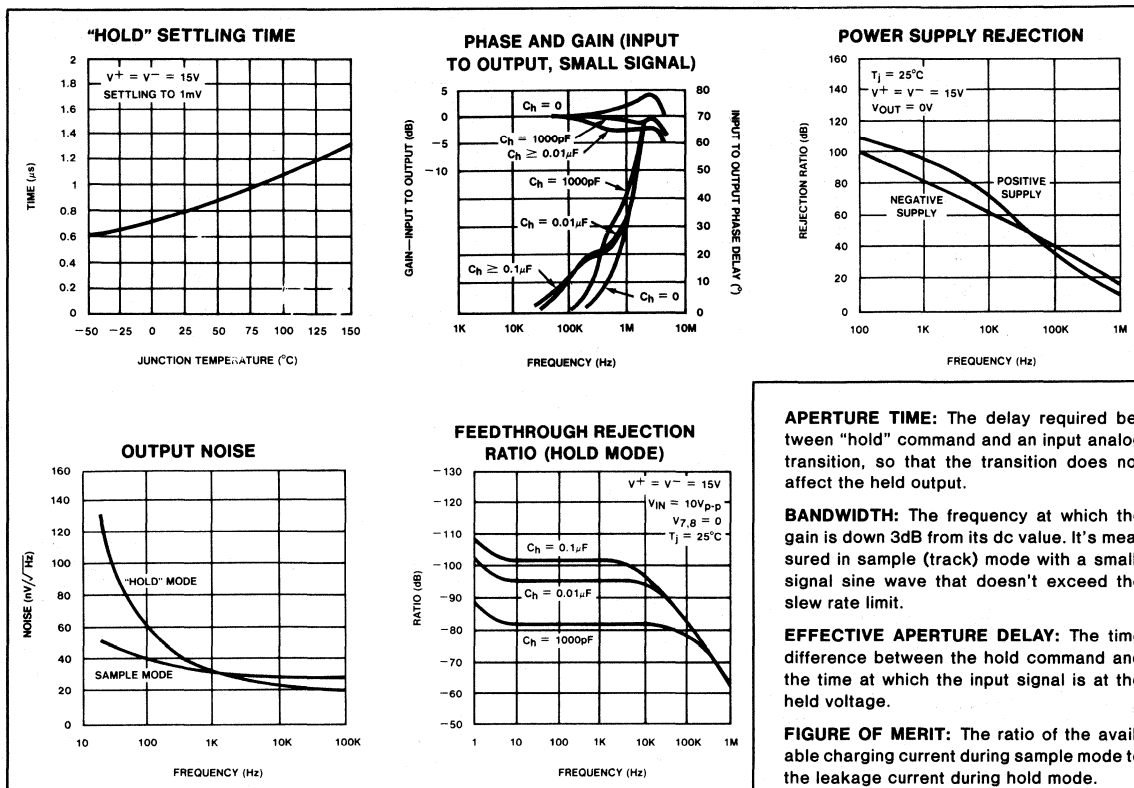
TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



SAMPLE AND HOLD AMPLIFIER

NE/SE5537

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



APERTURE TIME: The delay required between "hold" command and an input analog transition, so that the transition does not affect the held output.

BANDWIDTH: The frequency at which the gain is down 3dB from its dc value. It's measured in sample (track) mode with a small-signal sine wave that doesn't exceed the slew rate limit.

EFFECTIVE APERTURE DELAY: The time difference between the hold command and the time at which the input signal is at the held voltage.

FIGURE OF MERIT: The ratio of the available charging current during sample mode to the leakage current during hold mode.

HOLD-MODE DROOP: The output voltage change per unit of time while in hold. Commonly specified in V/s , $\mu V/\mu s$ or other convenient units.

HOLD-MODE FEEDTHROUGH: The percentage of an input sinusoidal signal that is measured at the output of a sample-and-hold when it's in hold mode.

HOLD SETTTLING TIME: The time required for the output to settle within 1mV of final value after the "hold" logic command.

SAMPLE-TO-HOLD OFFSET ERROR: The difference in output voltage between the time the switch starts to open, and the time when the output has settled completely. It is caused by charge being transferred to the hold capacitor switch as it opens.

SLEW RATE: The fastest rate at which the sample & hold output can change (specified in $V/\mu s$).

HOLD STEP: The voltage step at the output of the sample and hold when switching from sample mode to hold mode with a steady (dc) analog input voltage. Logic swing is 5V.

SAMPLE AND HOLD

INTRODUCTION

For many years designers have used the sample and hold (or track and hold) to operate on analog information in a time frame which is expedient.

By sampling a segment of the information and holding it until the proper timing for converting to some form of control signal or readout allows the designer certain freedom in performing predetermined manipulative functions. Therefore, the sample and hold can be defined as a "selective analog memory cell".

The memory is volatile and will also decay with time.

When using the sample and hold method for evaluating signal information, the designer is given the added feature of eliminating outside noise elements. With the analog to digital converter products available today the "dc memory" of the sample and hold can be

easily converted to digital format and further incorporated into microprocessor based systems.

Parametric evaluation of the sample and hold will be discussed in the following paragraphs.

DEFINITION OF TERMS

ACQUISITION TIME: The time required to acquire a new analog input voltage with an output step of 10V. Note that acquisition time is not just the time required for the output to settle, but also includes the time required for all internal nodes to settle so that the output assumes the proper value when switched to the hold mode.

APERTURE DELAY TIME: The time elapsed from the hold command to the opening of the switch.

APERTURE JITTER: Also called "aperture uncertainty time", it's the time variation or uncertainty with which the switch opens, or the time variation in aperture delay.

SAMPLE AND HOLD AMPLIFIER

NE/SE5537

DYNAMIC SAMPLING ERROR: The error introduced into the held output due to a changing analog input at the time the hold command is given. Error is expressed in mV with a given hold capacitor value and input slew rate. Note that this error term occurs even for long sample times.

GAIN ERROR: The ratio of output voltage swing to input voltage swing in the sample mode expressed as a percent difference.

THRESHOLD: Level shall be defined as that level which causes the switch control to change state.

BASIC BLOCK DIAGRAM

The basic circuit concept of the sample and hold circuit incorporates the use of two (2) operational amplifiers and a switch control mechanism (which determines sample, hold or track conditions). Reference figure 1.

The block diagram of the NE5537 is a closed loop non-inverting unity gain sample and hold system. The input buffer amplifier supplies the current necessary to charge the hold capacitor, while the output buffer amplifier closes the loop such that the output voltage is identical to the input voltage (with consideration for input offset voltage, offset current, and temperature variations which are common to all sample and hold circuits, be they monolithic, hybrid or modular).

When the sampling switch is open (in the hold mode) the clamping diodes close the loop around the input amplifier to keep it from being overdriven into saturation.

The switch control is driven by external logic levels via a timing sequence remote from the sample and hold device. Reference figure 2. The switch control has a floating reference (pin 7), referred to as the logic reference which makes the sample and hold device compatible to several types of external logic signals (TTL, PMOS, & CMOS). The switching device operates at a threshold level of 1.4V.

The switch mechanism is on (sampling an information stream) when the logic level is high (pin 8 is 1.4 volts higher than pin 7) and presents a load of 5 microamperes to the input logic signal. The analog sampled signal is amplified, stored (in the external holding capacitor), and buffered. At the end of the sampling period the internal switch mechanism turns off (switch opens) and the "stored analog memory" information on the external capacitor (pin 6) is loaded down by an operational amplifier connected in the unity gain non-inverting configuration. This

amplifier, whose input impedance is effectively:

$$R = R_{IN}(A_{OL}) / (1 + 1/A)$$

where

- R = Effective input impedance
- R_{IN} = Open loop input impedance
- A_{OL} = Open loop gain
- A = AC loop gain

Therefore, the higher the open loop gain of the second operational amplifier, the larger the effective loading on the capacitor. The larger the load, the lower the "leakage" current and the better the droop characteristics.

In actuality the amplifiers are designed with special leakage current cancellation circuits along with FET input devices. The leakage current cancellation circuits give better high temperature operation (remember that the FET amplifiers double in required bias current for every 10 degree increase in junction temperature).

Sampling time for the NE5537 is less than 10μsec, (measured to 0.1% of input signal). Leakage current is 6pA at a rate output load of 2kΩ.

BASIC APPLICATIONS

Multiplying DAC

As depicted in the block diagram of figure 3, the sample and hold circuit is used to supply a "variable" reference to the digital to analog converter. As the input reference varies, the output will change in accordance with equation 1, shown in figure 3.

Varying the input signal reference level can aid the system in performing both compression and expansion operations. The multiplying DAC's used are the Signetics SE/NE 5008; however, if the rate of change of the reference variation is kept slow enough a microprocessor compatible DAC can be incorporated, such as the NE5018 or the NE5020.

DATA ACQUISITION SYSTEMS

As mentioned earlier, the designer may wish to operate on several different segments of an "analog" signal; however he is limited by the fact that only one analog to digital converter channel is available to him. Figure 4 shows the means by which a multiplexing system may be accomplished.

APPLICATION HINTS

Hold Capacitor

A significant source of error in an accurate sample and hold circuit is dielectric absorption in the hold capacitor. A mylar cap, for

instance, may "sag back" up to 0.2% after a quick change in voltage. A long "soak" time is required before the circuit can be put back into the hold mode with this type of capacitor. Dielectrics with very low hysteresis are polystyrene, polypropylene, and Teflon. Other types such as mica and polycarbonate are not nearly as good. Ceramic is unusable with > 1% hysteresis. The advantage of polypropylene over polystyrene is that it extends the maximum ambient temperature from 85°C to 100°C. The hysteresis relaxation time constant in polystyrene, for instance, is 10-50ms. If A-to-D conversion can be made within 1ms, hysteresis error will be reduced by a factor of ten.

DC Zeroing

DC Zeroing is accomplished by connecting the offset adjust pin to the wiper of a 1kΩ potentiometer which has one end tied to V⁺ and the other end tied through a resistor to ground. The resistor should be selected to give ≈ 0.6mA through the 1kΩ potentiometer.

Sampling Dynamic Signals

Sampling errors due to moving (changing) input signals are of significant concern to designers employing sample and hold circuits. There exist finite phase delays through the sample and hold circuit causing an input-output phase differential for moving signals. In addition, the series protection resistor (300Ω to pin 6 of the NE5537) will add an RC time constant, over and above the slew rate limitation of the input buffer/current drive amplifier. This means that at the moment the "hold" command arrives, the hold capacitor voltage may be somewhat different than the actual analog input. The effect of these delays is opposite to the effect created by delays in the logic which switches the circuit from sample to hold. For example, consider an analog input of 20 Vp-p at 10kHz. Maximum dV/dt is 0.6V/μs. With no analog phase delay and 100ns logic delay, one could expect up to (0.1μs) (0.6V/μs) = 60mV error if the "hold" signal arrived near maximum dV/dt of the input. A positive going input would give a ±60mV error. Now assume a 1MHz (3dB) bandwidth for the overall analog loop. This generates a phase delay of 160ns. If the hold capacitor sees this exact delay, then error due to analog delay will be (0.16μs) (0.6V/μs) = -96mV (analog) for a total of -36mV. To add to the confusion, analog delay is proportional to hold capacitor value while digital delay remains constant. A family of curves (dynamic sampling error) is included to help estimate errors.

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SAMPLE AND HOLD AMPLIFIER

NE/SE5537

A curve labeled *Aperture Time* has been included for sampling conditions where the input is steady during the sampling period, but may experience a sudden change nearly coincident with the "hold" command. This curve is based on a 1mV error fed into the output.

A second curve, *Hold Settling Time* indicates the time required for the output to settle to 1mV after the "hold" command.

Digital Feedthrough

Fast rise time logic signals can cause hold errors by feeding externally into the analog input at the same time the amplifier is put into the hold mode. To minimize this prob-

lem, board layout should keep logic lines as far as possible from the analog input. Grounded guarding traces may also be used around the input line, especially if it is driven from a high impedance source. Reducing high amplitude logic signals to 2.5V will also help.

Logic signals also couple to the hold capacitor. This hold capacitor should be guarded by a P.C. card trace connected to the sample-and-hold output. This will also minimize board leakage.

SPECIAL NOTES

1. Not all definitions herein defined are measured parametrically for the NE5537, but are legitimate terms used in sample and hold systems.
2. Reference should be made to Design Engineering, volumes 23 (Nov. 8, 1978), 25 (Dec. 6, 1978) and 26 (Dec. 20, 1978) for articles written by Eugene Zuch of Datel Systems, Inc. for a further discussion of sample and hold circuits.
3. Reference also made to National Semiconductor Corporation's Special Functions Data Book (1976).

TYPICAL APPLICATIONS

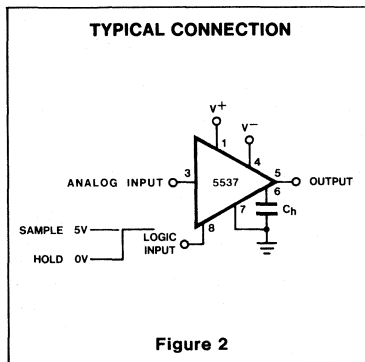


Figure 2

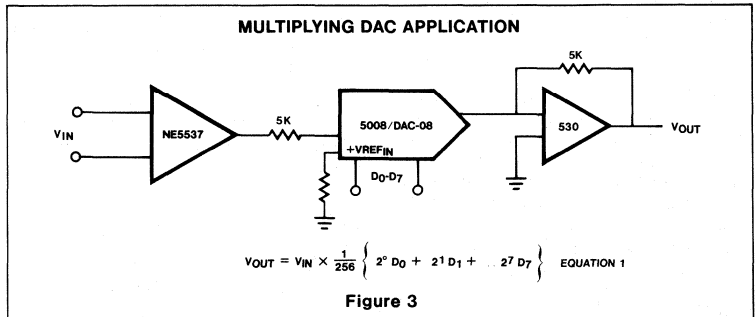


Figure 3

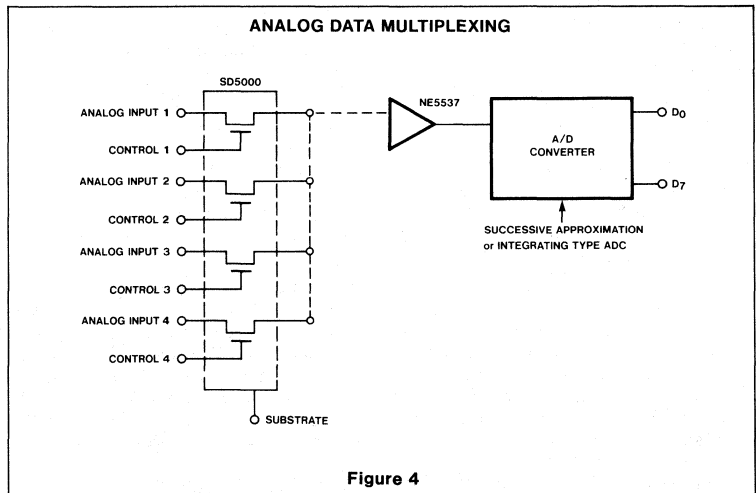


Figure 4

Section 13 Transistor Arrays

INDEX

Section 13 — Transistor Arrays

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SEVEN TRANSISTOR ARRAY

CA3081/CA3082

DESCRIPTION

The CA3081 and CA3082 are monolithic integrated circuits, each consisting of seven separate npn transistors on a common substrate. The transistors are capable of driving loads of up to 100mA. At the same time, the transistor geometry used gives maximum current gain at quite low currents, making the devices also suitable for small-signal applications. In the CA3081, the transistors are connected in a common emitter configuration, while in the CA3082, the collectors are common. The transistor arrays are particularly suitable for driving light-emitting diodes and seven-segment displays, as well as for general purpose applications. The CA3081 and CA3082 are available in both 16-lead dual-in-line plastic and cerdip packages.

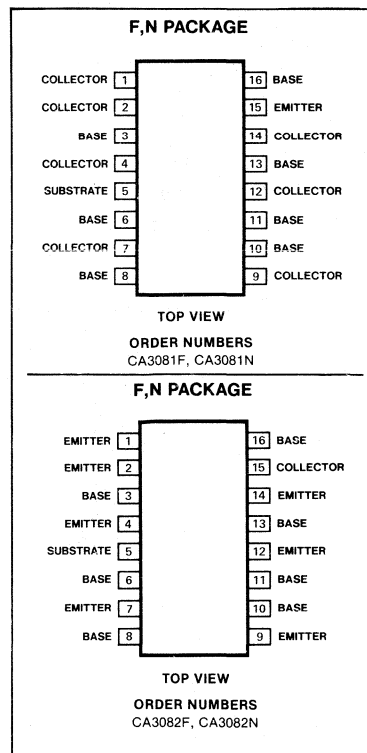
FEATURES

- Seven transistors permit a wide range of applications in either a common emitter (CA3081) or common-collector (CA3082) configuration.
- High I_C : 100mA maximum
- Low $V_{CE\ sat}$ (at 50mA): 0.4V typical

APPLICATIONS

- Drivers for:
Incandescent display devices
LED
Relay control
Thyristor firing

PIN CONFIGURATIONS



PIN DESIGNATION (CA3081)

PIN NO.	SYMBOL	NAME AND FUNCTION
1	C1	Collector, Transistor 1
2	C2	Collector, Transistor 2
3	B2	Base, Transistor 2
4	C5	Collector, Transistor 5
5	SUB	Substrate
6	B5	Base, Transistor 5
7	C7	Collector, Transistor 7
8	B7	Base, Transistor 7
9	C6	Collector, Transistor 6
10	B6	Base, Transistor 6
11	B4	Base, Transistor 4
12	C4	Collector, Transistor 4
13	B3	Base, Transistor 3
14	C3	Collector, Transistor 3
15	E	Common emitter
16	B1	Base, Transistor 1

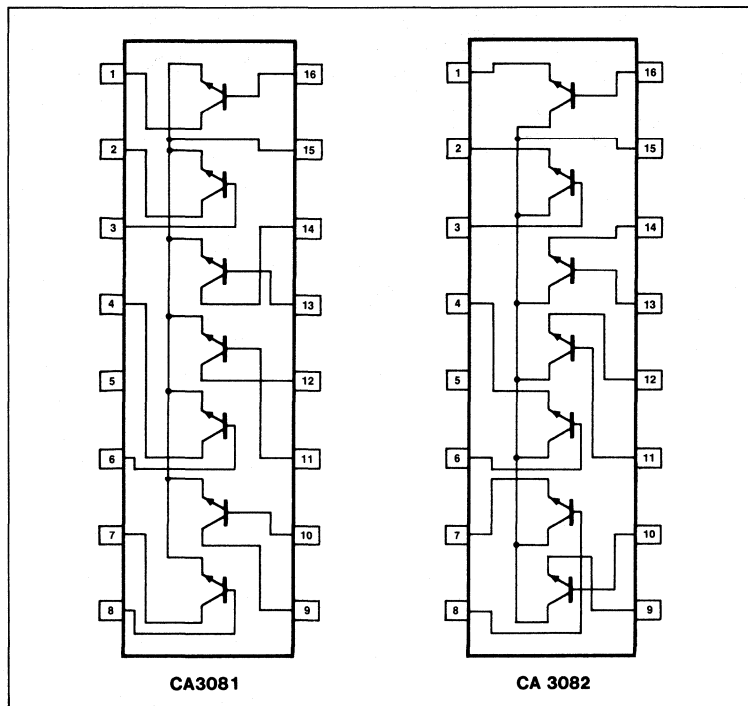
PIN DESIGNATION (CA3082)

PIN	SYMBOL	NAME AND FUNCTION
1	E1	Emitter, Transistor 1
2	E2	Emitter, Transistor 2
3	B2	Base, Transistor 2
4	E5	Emitter, Transistor 5
5	SUB	Substrate
6	B5	Base, Transistor 5
7	E6	Emitter, Transistor 6
8	B6	Base, Transistor 6
9	E7	Emitter, Transistor 7
10	B7	Base, Transistor 7
11	B4	Base, Transistor 4
12	E4	Emitter, Transistor 4
13	B3	Base, Transistor 3
14	E3	Emitter, Transistor 3
15	C	Common collector
16	B1	Base, Transistor 1

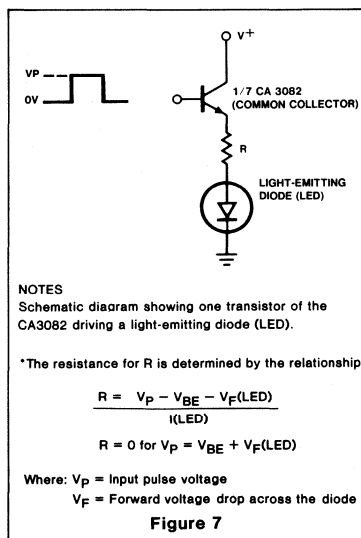
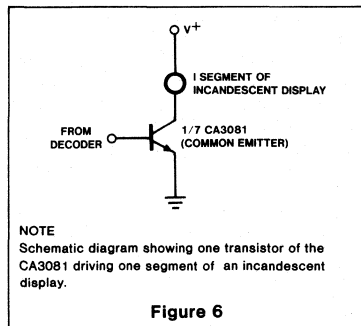
SEVEN TRANSISTOR ARRAY

CA3081/CA3082

BLOCK DIAGRAM



TYPICAL READ-OUT DRIVER APPLICATIONS



ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ C$

PARAMETER	RATING	UNIT	
P	Power dissipation: Any one transistor	500	mW
P _{TOT}	Total package	750	mW
	Above 55°C	Derate Linearly 6.67	mW / °C
T _A	Ambient temperature range: Operating	-55 to +125	°C
	Storage	-65 to +150	°C
	Lead temperature (10 seconds)	265	°C
V _{CEO}	Collector to emitter voltage ¹	16	V
V _{CBO}	Collector to base voltage ¹	20	V
V _{CIO}	Collector to substrate voltage ^{1,2}	20	V
V _{EBO}	Emitter to base voltage ¹	5	V
I _C	Collector current ¹	100	mA
I _B	Base current ¹	20	mA

NOTES

1. Ratings apply for each transistor in the device.
2. The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

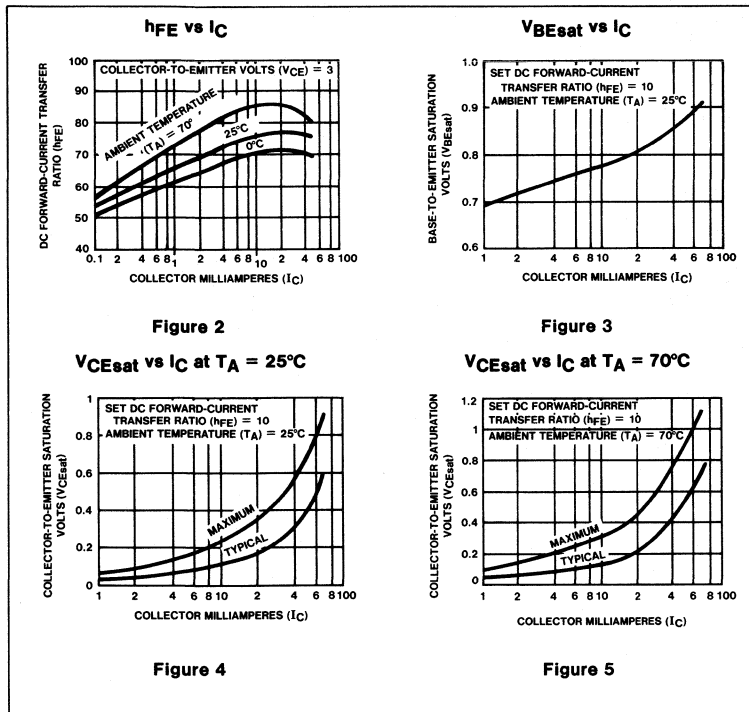
SEVEN TRANSISTOR ARRAY

CA3081/CA3082

STATIC ELECTRICAL CHARACTERISTICS FOR EACH TRANSISTOR $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
		Min	Typ	Max		
V_{CBO} (BR)	Collector to base breakdown voltage				V	
V_{CIO} (BR)	Collector to substrate breakdown voltage				V	
V_{CEO} (BR)	Collector to emitter breakdown voltage				V	
V_{EBO} (BR)	Emitter to base breakdown voltage				V	
h_{FE}	DC forward current Transfer Ratio	$V_{CE} = 0.5\text{V}, I_C = 30\text{mA}$ $V_{CE} = 0.8\text{V}, I_C = 50\text{mA}$	30 40	68 70		
$V_{BE\text{ sat}}$	Base to emitter saturation voltage	$I_C = 30\text{mA}, I_B = 1\text{mA}$		0.87	1.0	V
$V_{CE\text{ sat}}$	Collector to emitter saturation voltage	CA3081 / CA3082 $I_C = 30\text{mA}, I_B = 1\text{mA}$ CA3081 $I_C = 50\text{mA}, I_B = 5\text{mA}$ CA3082 $I_C = 50\text{mA}, I_B = 5\text{mA}$		0.27 0.4 0.4	0.5 0.7 0.8	V
I_{CEO}	Collector cutoff current	$V_{CE} = 10\text{V}, I_B = 0$			10	μA
I_{CBO}	Collector cutoff current	$V_{CB} = 10\text{V}, I_E = 0$			1	μA

TYPICAL PERFORMANCE CHARACTERISTICS



HIGH VOLTAGE TRANSISTOR ARRAY

CA3183

DESCRIPTION

The CA3183 is a general purpose high-voltage silicon n-p-n transistor array on a common monolithic substrate. This integrated circuit features a tighter control of breakdown voltage, providing for applications requiring higher voltages. The array consists of five high-current transistors with independent connections for each transistor. Additionally, two of the transistors (Q_1 and Q_2) are matched at low-current for applications where offset parameters are of special importance. A special substrate terminal has also been included for greater flexibility in circuit design. The CA3183 is available in both 16-lead dual-in-line plastic and cerdip packages and operates over the ambient temperature range of -40°C to $+85^{\circ}\text{C}$.

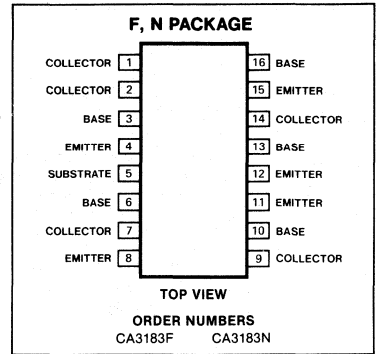
FEATURES

- Matched general purpose transistors
- V_{BE} matched $\pm 5\text{mV}$ maximum
- High I_C : 75mA maximum

APPLICATIONS

- General use in signal processing systems in dc through VHF range
- Custom designed differential amplifiers
- Temperature compensated amplifiers
- Lamp and relay drivers
- Thyristor firing

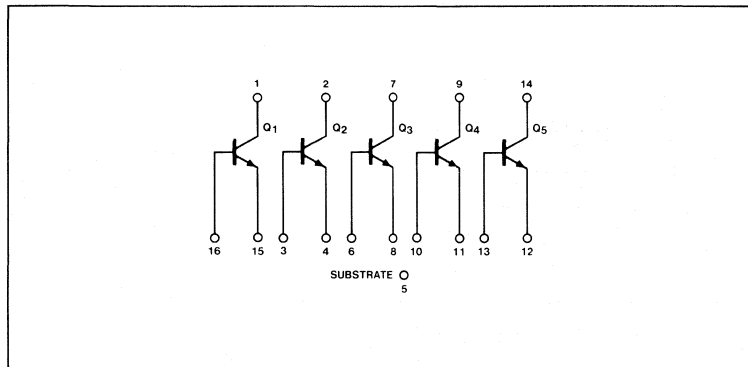
PIN CONFIGURATION



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	C1	Collector, transistor 1
2	C2	Collector, transistor 2
3	B2	Base, transistor 2
4	E2	Emitter, transistor 2
5	SUB	Substrate
6	B3	Base, transistor 3
7	C3	Collector, transistor 3
8	E3	Emitter, transistor 3
9	C4	Collector, transistor 4
10	B4	Base, transistor 4
11	E4	Emitter, transistor 4
12	E5	Emitter, transistor 5
13	B5	Base, transistor 5
14	C5	Collector, transistor 5
15	E1	Emitter, transistor 1
16	B1	Base, transistor 1

BLOCK DIAGRAM



HIGH VOLTAGE TRANSISTOR ARRAY

CA3183

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _{CEO}	Collector-emitter voltage ¹	40	V
V _{CBO}	Collector-base voltage ¹	50	V
V _{CIO}	Collector-substrate voltage ^{1,2}	50	V
V _{EBO}	Emitter-base voltage ¹	5	V
I _C	Collector current ¹	75	mA
I _B	Base current ¹	20	mA
P	Power dissipation: any one transistor	500	mW
P _{TOT}	total package up to 55°C	750	mW
T _A	Operating ambient temperature	-40 to +85	°C
T _{stg}	Storage temperature	-65 to +150	°C

NOTES

- For each transistor.
- The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

STATIC ELECTRICAL CHARACTERISTICS FOR EACH TRANSISTOR $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	CA3183			UNIT
		Min	Typ	Max	
V _{CEO} (BR)	Collector-emitter breakdown voltage $I_C = 1\text{mA}, I_B = 0$	40			V
V _{CBO} (BR)	Collector-base breakdown voltage $I_C = 100\mu\text{A}, I_E = 0$	50			V
V _{CIO} (BR)	Collector-substrate breakdown voltage $I_{CI} = 100\mu\text{A}, I_B = 0, I_E = 0$	50			V
V _{EBO} (BR)	Emitter-base breakdown voltage $I_E = 500\mu\text{A}, I_C = 0$	5			V
I _{CEO}	Collector cutoff current $V_{CE} = 10\text{V}, I_B = 0$			10	μA
I _{CBO}	Collector cutoff current $V_{CB} = 10\text{V}, I_E = 0$			1	μA
h _{FE}	DC forward current transfer ratio $V_{CE} = 3\text{V}, I_C = 10\text{mA}$ $V_{CE} = 5\text{V}, I_C = 50\text{mA}$	40 40			
V _{BE}	Base-emitter voltage $V_{CE} = 3\text{V}, I_C = 10\text{mA}$	0.65	0.75	0.85	V
V _{CE} (SAT)	Collector-emitter saturation voltage $I_C = 50\text{mA}, I_B = 5\text{mA}$		1.7	3.0	V

STATIC ELECTRICAL CHARACTERISTICS FOR TRANSISTORS Q1 AND Q2 (AS A DIFFERENTIAL AMPLIFIER) $T_A = 25^\circ\text{C}$ unless otherwise specified.

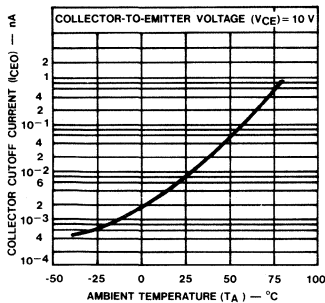
PARAMETER	TEST CONDITIONS	CA3183			UNIT
		Min	Typ	Max	
V _{I0}	Absolute input offset voltage $V_{CE} = 3\text{V}, I_C = 1\text{mA}$		0.47	5	mV
I _{I0}	Absolute input offset current $V_{CE} = 3\text{V}, I_C = 1\text{mA}$		0.78	2.5	μA

HIGH VOLTAGE TRANSISTOR ARRAY

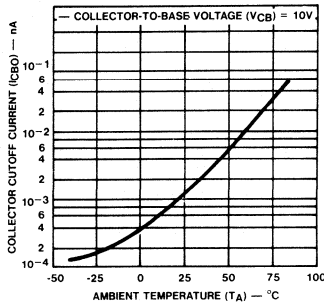
CA3183

TYPICAL PERFORMANCE CHARACTERISTICS

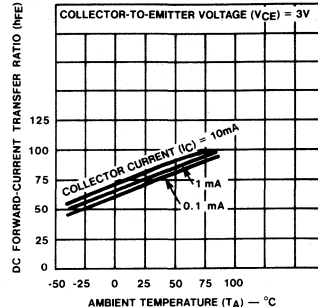
$I_{CEO} \ v \ T_A$ FOR ANY TRANSISTOR



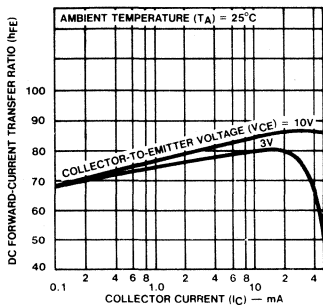
$I_{CBO} \ v \ T_A$ FOR ANY TRANSISTOR



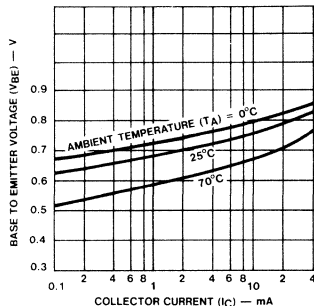
$h_{FE} \ v \ T_A$ FOR ANY TRANSISTOR



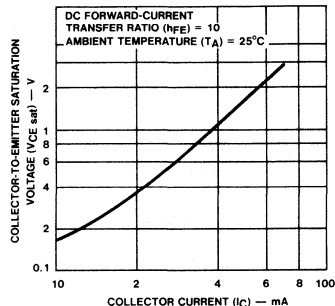
$h_{FE} \ v \ I_C$ FOR ANY TRANSISTOR



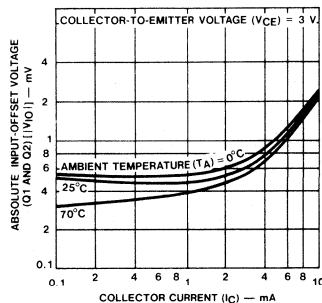
$V_{BE} \ v \ I_C$ FOR ANY TRANSISTOR



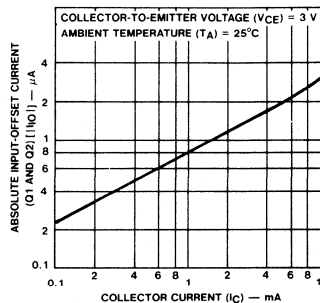
$V_{CE \ sat} \ v \ I_C$ FOR ANY TRANSISTOR



$|V_{IO}| \ v \ I_C$ FOR DIFFERENTIAL AMPLIFIER (Q1 AND Q2)



$|I_{IO}| \ v \ I_C$ FOR DIFFERENTIAL AMPLIFIER (Q1 AND Q2)



HIGH VOLTAGE/HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

ULN2001/03/04

DESCRIPTION

These high-voltage, high-current Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak inrush currents to 600mA are allowable, making them ideal for driving tungsten filament lamps also.

The Type ULN-2001 is a general-purpose array which may be used with DTL, TTL, PMOS, CMOS, etc. It is pinned with inputs opposite outputs to facilitate ease of circuit board layout and is priced to compete directly with discrete transistor alternatives.

The Type ULN-2003 has a series base resistor to each Darlington pair, and thus allows operation directly with TTL or CMOS operating at a supply voltage of 5V.

The Type ULN-2004 has an appropriate series input resistor to allow its operation directly from CMOS or PMOS outputs utilizing supply voltages of 6 to 15V. The required input current is below that of the Type ULN-2003.

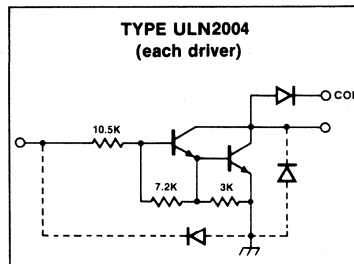
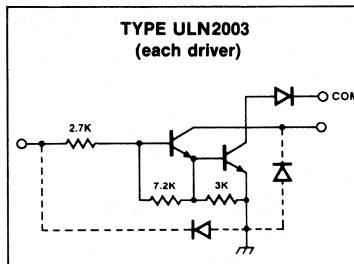
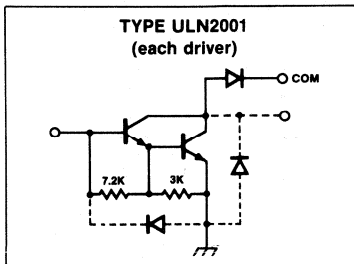
In all cases, the individual Darlington pair collector current rating is 500mA. However, outputs may be paralleled for higher load current capability. All devices are supplied in a 16-pin dual in-line plastic package.

FEATURES

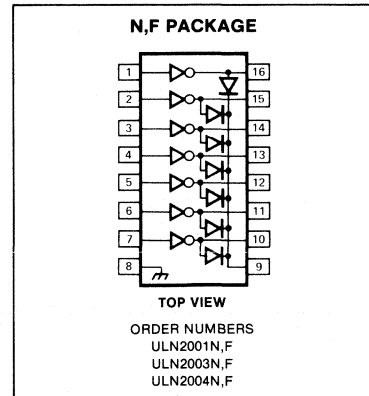
- Peak inrush current 600mA
- Protected internally against inductive loads
- Open collector topology
- Compatible with most logic technologies

ABSOLUTE MAXIMUM RATINGS

EQUIVALENT SCHEMATICS



PIN CONFIGURATION



at 25°C Free-Air temperature for any one Darlington pair unless otherwise specified.

PARAMETER	RATING	UNIT
V _{CE}	Output voltage	50 V
V _{IN}	Input voltage	30 V
V _{EBO}	Emitter base voltage	6 V
I _C	Continuous collector current	500 mA
I _B	Continuous base current	25 mA
P _D	Power dissipation	1.3 W
	Derating factor above 25°C	95 °C/W
T _A	Ambient temperature range (operating)	0 to +85 °C
T _S	Storage temperature range	-65 to +150 °C

*NOTE
Under normal operating conditions, these units will sustain 350mA per output with V_{CE(SAT)} = 1.6V at 70°C with a pulse width of 20 ms and a duty cycle of 30%.

HIGH VOLTAGE/HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

ULN2001/03/04

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.1,2,3

PARAMETER	TEST CONDITIONS	Test Fig.	LIMITS			UNIT
			Min	Typ	Max	
I _{CEX} Output leakage current Type ULN-2004	V _{CE} = 50V, T _A = 70°C V _{CE} = 50V, T _A = 70°C, V _{IN} = 1V	1A	—	—	100	μA
		1B	—	—	500	μA
V _{CE(SAT)} Collector-emitter Saturation voltage	I _C = 350mA, I _B = 500μA I _C = 200mA, I _B = 350μA I _C = 100mA, I _B = 250μA	2	—	1.25	1.6	V
		2	—	1.1	1.3	V
		2	—	0.9	1.1	V
I _{IN(ON)} Input current Type ULN-2003 Type ULN-2004	V _{IN} = 3.85V V _{IN} = 5V V _{IN} = 12V	3	—	0.93	1.35	mA
		3	—	0.35	0.5	mA
		3	—	1.0	1.45	mA
I _{IN(OFF)} Input current	I _C = 500μA, T _A = 70°C	4	50	65	—	μA
V _{IN(ON)} Input voltage Type ULN-2003 Type ULN-2004	V _{CE} = 2V, I _C = 200mA V _{CE} = 2V, I _C = 250mA V _{CE} = 2V, I _C = 300mA	5	—	—	2.4	V
		5	—	—	2.7	V
		5	—	—	3.0	V
	V _{CE} = 2V, I _C = 125mA V _{CE} = 2V, I _C = 200mA V _{CE} = 2V, I _C = 275mA V _{CE} = 2V, I _C = 350mA	5	—	—	5.0	V
		5	—	—	6.0	V
		5	—	—	7.0	V
		5	—	—	8.0	V
h _{FE} D-C forward current transfer ratio Type ULN-2001	V _{CE} = 2V, I _C = 350mA	2	1000	—	—	—
C _{IN} Input capacitance		—	—	15	30	pF
I _R Clamp diode leakage current	V _R = 50V	6	—	—	50	μA
V _F Clamp diode forward voltage	I _F = 350mA	7	—	1.7	2	V

NOTES

- All limits stated apply to the complete Darlington series except as specified for a single device type.
- The I_{IN(OFF)} current limit guarantees against partial turn-on of the output.
- The V_{IN(ON)} voltage limit guarantees a minimum output sink current per the specified test conditions.

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise specified.1,2,3

PARAMETER	TEST CONDITIONS	Test Fig.	LIMITS			UNIT
			Min	Typ	Max	
t _{PLH} Turn-on delay	0.5 E _{IN} to 0.5 E _{OUT}	—	—	1.0	5	μs
t _{PHL} Turn-off delay	0.5 E _{IN} to 0.5 E _{OUT}	—	—	1.0	5	μs

NOTES

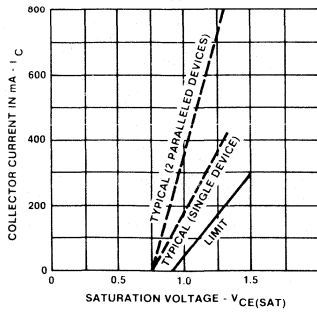
- All limits stated apply to the complete Darlington series except as specified for a single device type.
- The I_{IN(OFF)} current limit guarantees against partial turn-on of the output.
- The V_{IN(ON)} voltage limit guarantees a minimum output sink current per the specified test conditions.

HIGH VOLTAGE/HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

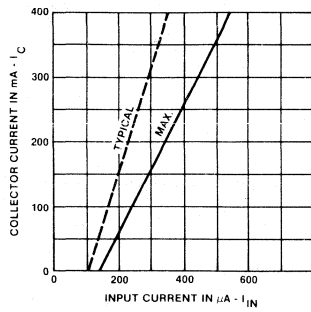
ULN2001/03/04

TYPICAL PERFORMANCE CHARACTERISTICS

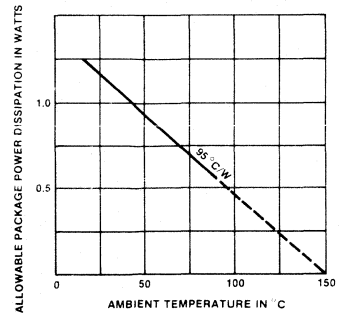
COLLECTOR CURRENT AS A FUNCTION OF SATURATION VOLTAGE



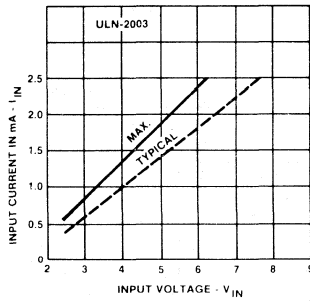
COLLECTOR CURRENT AS A FUNCTION OF INPUT CURRENT



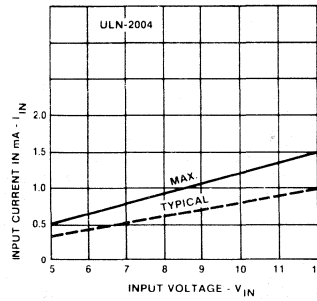
ALLOWABLE AVERAGE PACKAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



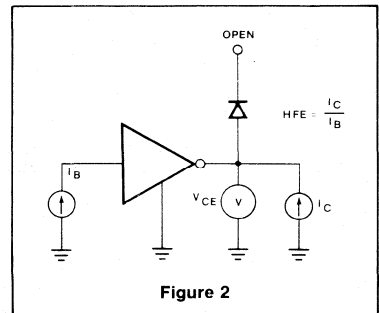
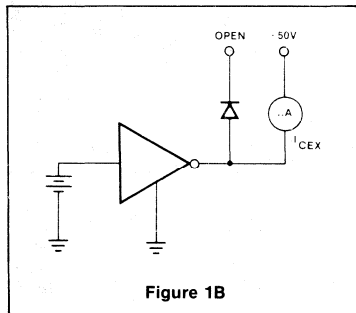
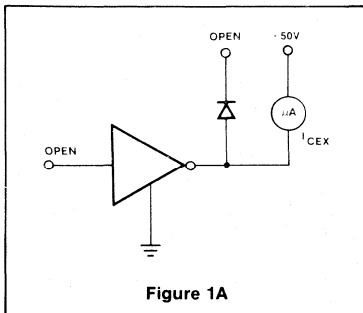
INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2003



INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE FOR TYPE ULN-2004



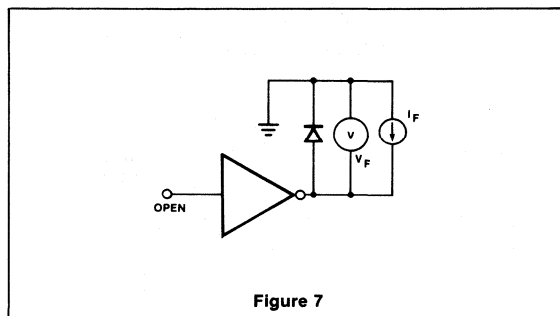
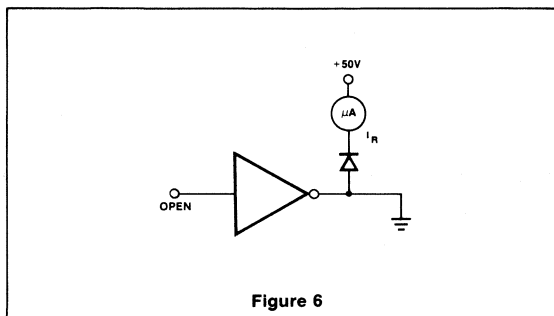
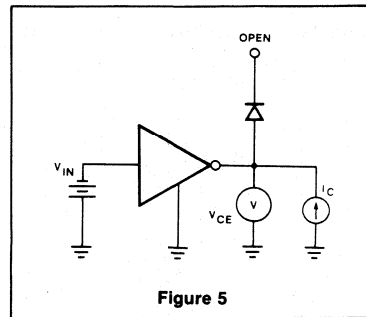
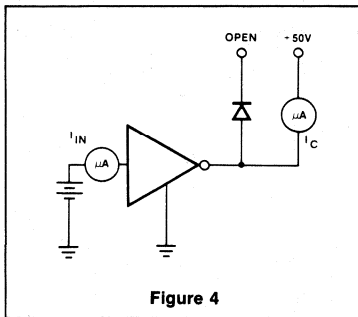
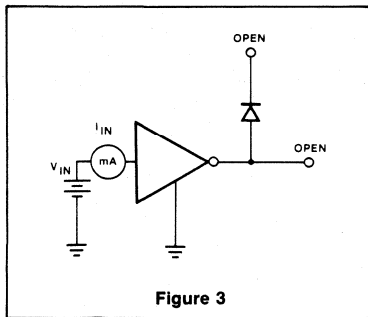
TEST FIGURES



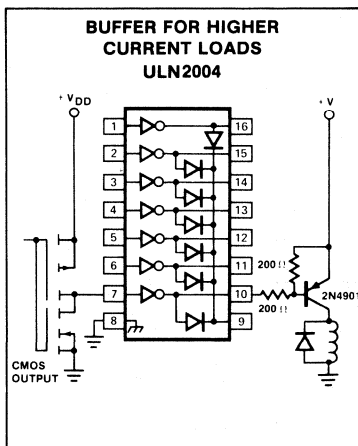
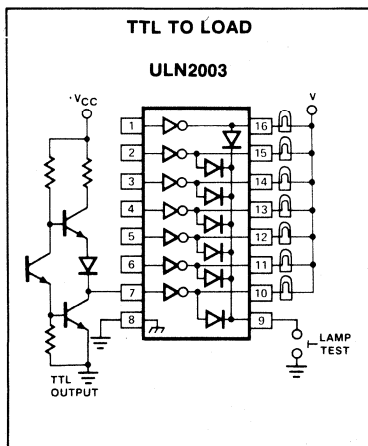
HIGH VOLTAGE/HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

ULN2001/03/04

TEST FIGURES (Cont'd)



TYPICAL APPLICATIONS



Section 14 Radio Circuits

INDEX

Section 14 — Radio Circuits

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FM IF SYSTEM

CA3089

DESCRIPTION

CA3089 is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Figure 6 is a block diagram showing the CA3089 features, which include a three-state FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable features such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8 to +18 volts.

The CA3089 is ideal for high-fidelity operation. Distortion in a CA3089 FM-IF system is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089 utilizes a 16-lead dual-in-line plastic package and can operate over the ambient temperature range of -40°C to +85°C.

FEATURES

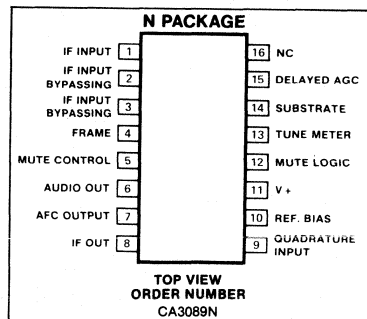
- **Exceptional limiting sensitivity: 10μV typ. at -3dB point**
- **Low distortion: 0.1% typ. (with double-tuned coil)**

- **Single-coil tuning capability**
- **High recovered audio: 400mV typ.**
- **Provides specific signal for control of interchannel muting (squelch)**
- **Provides specific signal for direct drive of a tuning meter**
- **Provides delayed AGC voltage for RF amplifier**
- **Provides a specific circuit for flexible AFC**
- **Internal supply/voltage regulators**

APPLICATIONS

- **High-fidelity FM receivers**
- **Automotive FM receivers**
- **Communications FM receivers**

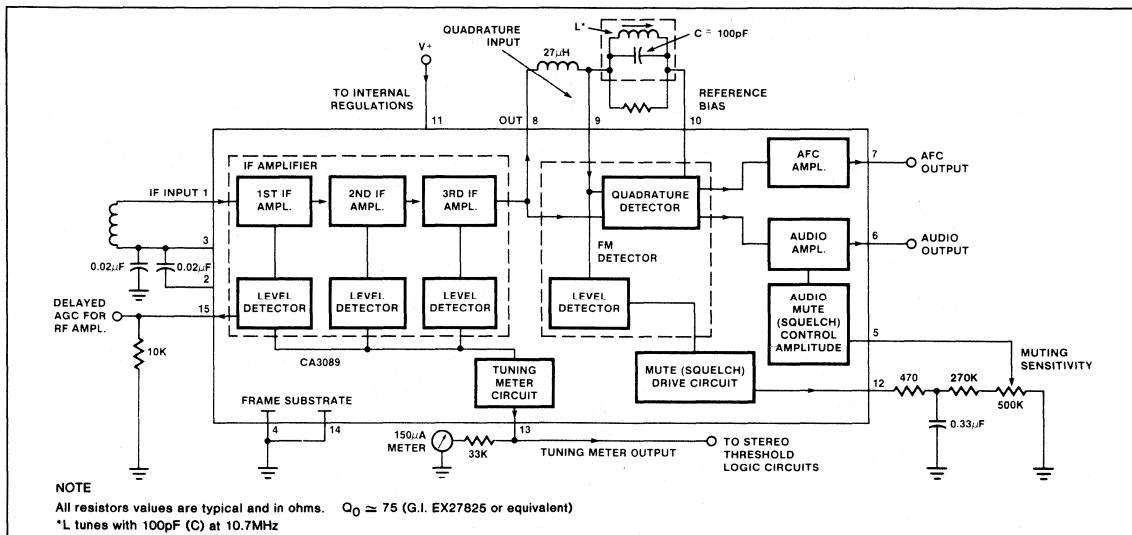
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
DC supply voltage:		
Between terminals 11 and 4	18	V
Between terminals 11 and 14	18	V
DC Current (out of terminal 15)	2	mA
Device dissipation:		
Up to $T_A = 60^\circ\text{C}$	600	mW
Above $T_A = 60^\circ\text{C}$	derate linearly	
	6.7	mW/°C
Ambient temperature range:		
Operating	-40 to +85	°C
Storage	-65 to +150	°C
Lead temperature (during soldering):		
At distance not less than 1/32" (0.79mm) from case for 10 seconds-max	+265	°C

BLOCK DIAGRAM

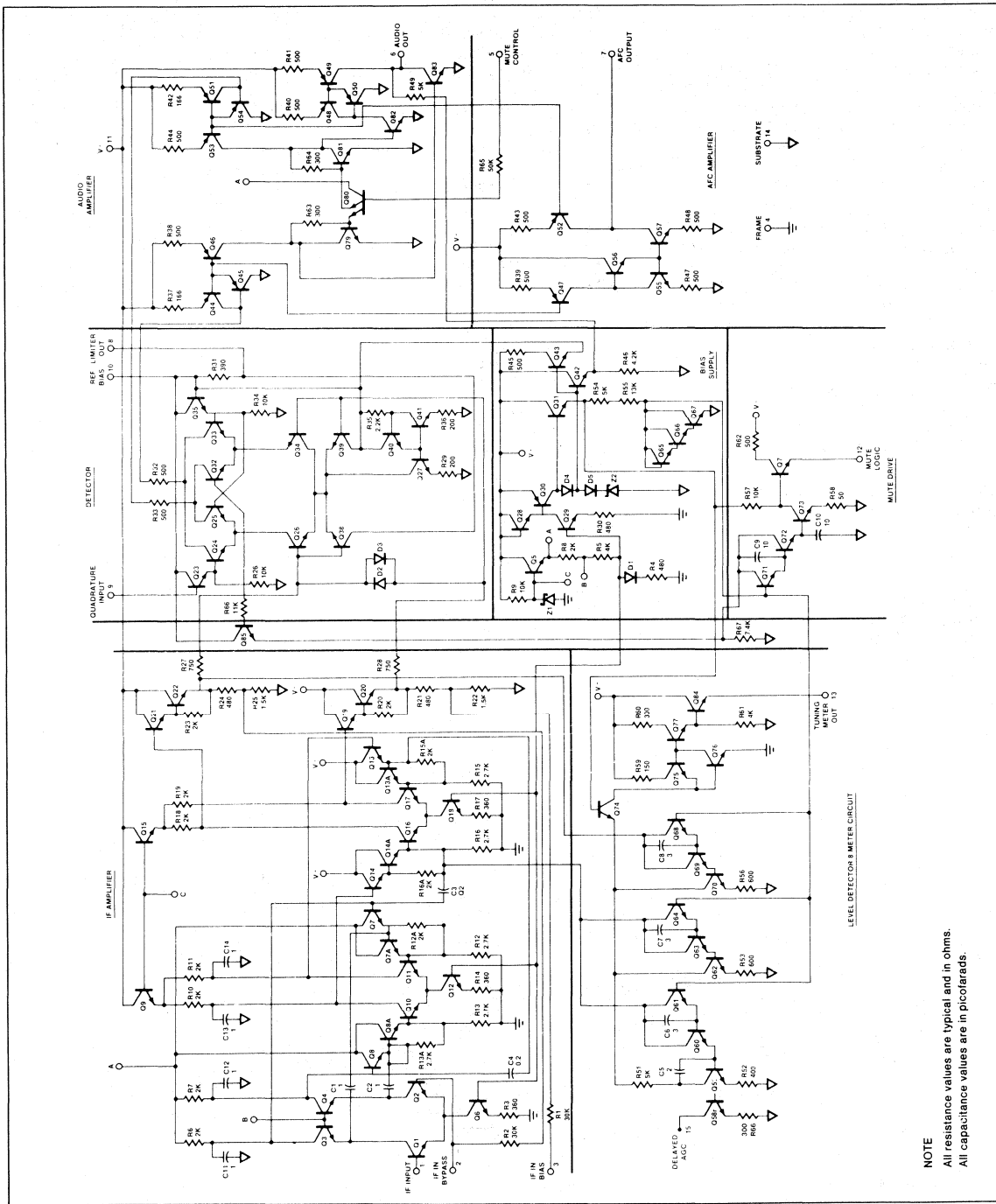


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FM IF SYSTEM

CA3089

EQUIVALENT SCHEMATIC



NOTE
 All resistance values are typical and in ohms.
 All capacitance values are in picofarads.

FM IF SYSTEM

CA3089

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V^+ = 12\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	CA3089D2			UNIT
		Min	Typ	Max	
STATIC (DC) CHARACTERISTICS					
I_{11} Quiescent circuit current	No signal input, non-muted	16	23	30	mA
DC Voltages: ⁴					
V_1 Terminal 1 (IF input)	No signal input, non-muted	1.2	1.9	2.4	V
V_2 Terminal 2 (ac return to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_3 Terminal 3 (dc bias to input)	No signal input, non-muted	1.2	1.9	2.4	V
V_6 Terminal 6 (audio output)	No signal input, non-muted	5.0	5.6	6.0	V
V_7 Terminal 7 (A.F.C.)	No signal input, non-muted	5.0	5.6	6.0	V
V_{10} Terminal 10 (dc reference)	No signal input, non-muted	5.0	5.6	6.0	V
DYNAMIC CHARACTERISTICS					
$V_{I(\text{lim})}$ Input limiting voltage (-3dB point) ³			10	25	μV
AMR AM Rejection (terminal 6) ⁴					
V_O Recovered audio voltage (terminal 6) ³	$V_{IN} = 0.1\text{V}$, $F_O = 10.7\text{MHz}$, $f_{\text{mod}} = 400\text{Hz}$, AM Mod = 30%	45 400	55 500	600	dB mV
Total harmonic distortion: ¹					
THD Single tuned (terminal 6) ³			0.5	1.0	%
THD Double tuned (terminal 6) ⁴	$f_{\text{mod}} = 400\text{Hz}$, $V_{IN} = 0.1$		0.1		%
S+N/N Signal plus noise to noise ratio (terminal 6) ³	Deviation = $\pm 75\text{kHz}$ $V_{IN} = 0.1\text{V}$	60	70		dB
MU_{IN} Mute input (terminal 5)	$V_5 = 2.5\text{V}$	50	70		dB
MU_{OUT} Mute output (terminal 12)	$V_{IN} = 50\mu\text{V}$ $V_{IN} = 0\text{V}$	4.0		.5	V V
MTR Meter output (terminal 13)	$V_{IN} = 0.1\text{V}$ $V_{IN} = 500\mu\text{V}$ $V_{IN} = 0\text{V}$	2.5 1.0	3.5 1.5	.7	V V V
AGC Delayed AGC (terminal 15)	$V_{IN} = .01\text{V}$ $V_{IN} = 10\mu\text{V}$	4.0	5.0	.5	V V
THD Double tuned (terminal 6) ⁴	$f_{\text{mod}} = 400\text{Hz}$ $V_{IN} = 0.1$		0.1		%

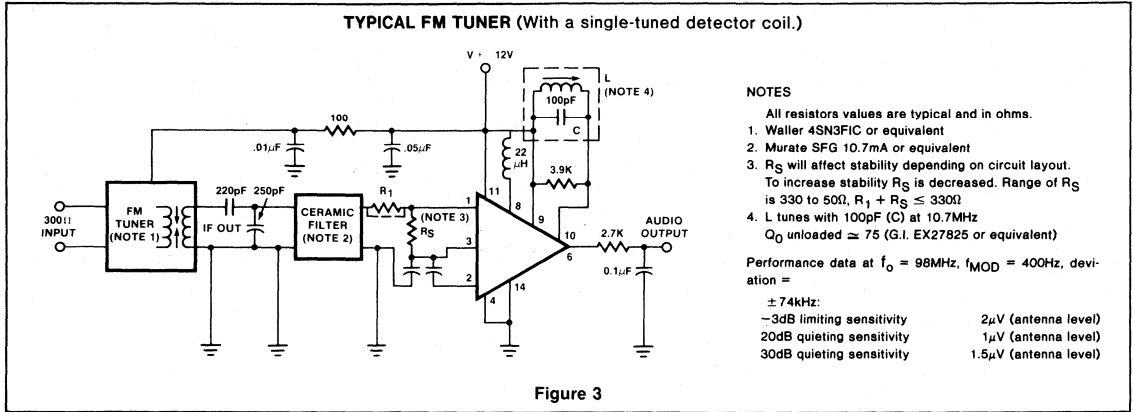
NOTES

1. THD characteristics and Audio Level are essentially a function of the phase and Q characteristics of the network connected between terminals 8,9, and 10.
2. Test circuit Figure 1.
3. Test circuit Figure 2.
4. Test circuit Figures 1 and 2.

FM IF SYSTEM

CA3089

TEST CIRCUITS



SYSTEM DESIGN CONSIDERATIONS

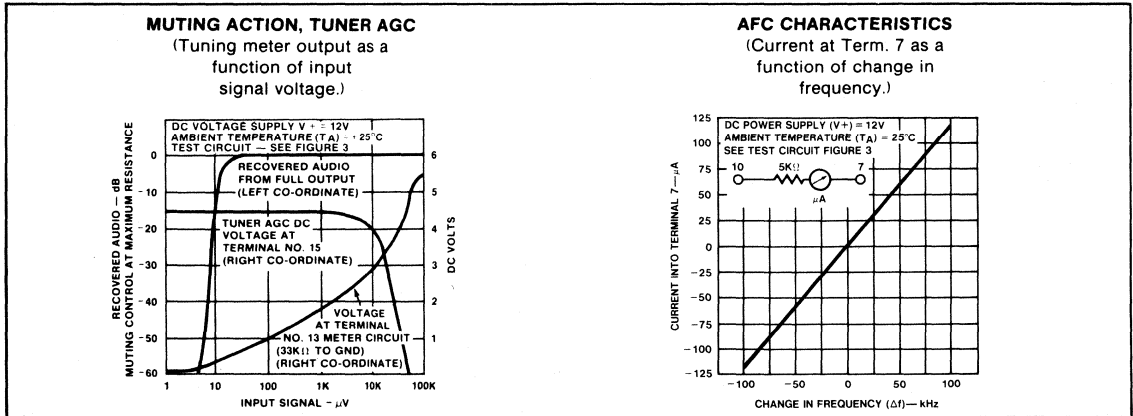
The CA3089 is a very high gain device and therefore careful consideration must be given to the layout of external components to minimize feedback. The input by-pass capacitors should be located close to the input terminals and the values

should not be large nor should the capacitors be of the type which might introduce inductive reactance to the circuit. An example of good by-pass capacitors would be ceramic disc with values in the range of .01 to .05 microfarad.

The input impedance of the CA3089 is approximately 10,000 ohms. It is *not*

recommended to match this impedance. The value of the input termination resistor should be as low as possible without degrading system operation. The lower the value of this resistor the greater the system stability. An input terminating resistor between 50 and 100 ohms is recommended.

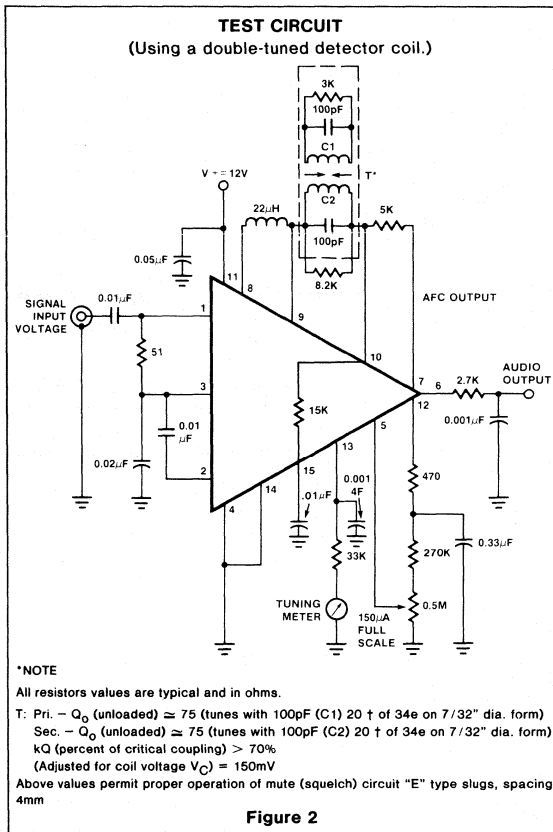
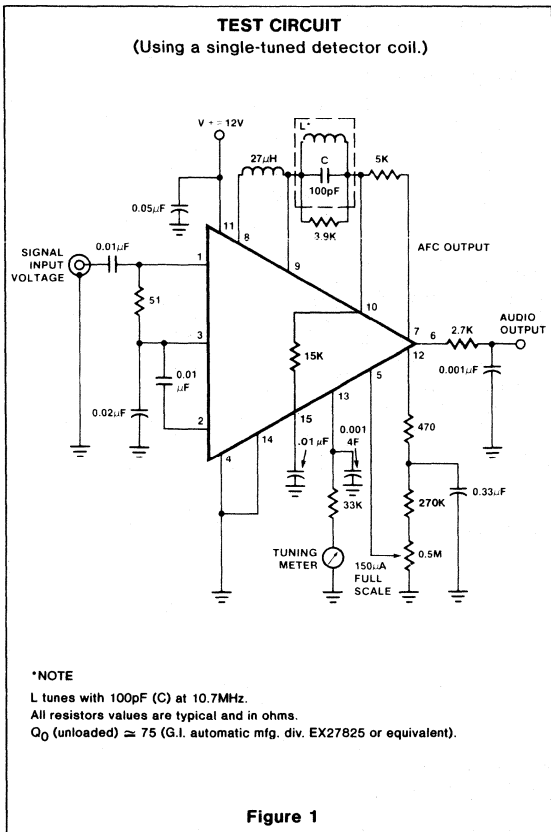
TYPICAL PERFORMANCE CHARACTERISTICS



FM IF SYSTEM

CA3089

TEST CIRCUITS



FM/IF SYSTEM

CA3189

DESCRIPTION

The CA3189 is a monolithic integrated circuit that provides all the functions of a comprehensive FM/IF system. The CA3189 features a three stage FM/IF amplifier/limiter configuration with level detectors for each stage. A doubly balanced quadrature FM detector and an audio amplifier features the optional use of a muting (squelch) circuit. Mute is enabled when either the input signal level is low or when the input frequency changes, through an external mute logic circuit between pins 5 and 12. Center channel detect can also be derived via this mute logic circuit.

The CA3189 includes features found in the CA3089, such as delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. Internal power supply regulators maintain a nearly constant current drain over the voltage range of +8V to +16V. The CA3189 FM/IF system distortion is primarily a function of the phase linearity of the outboard detector coil.

FEATURES

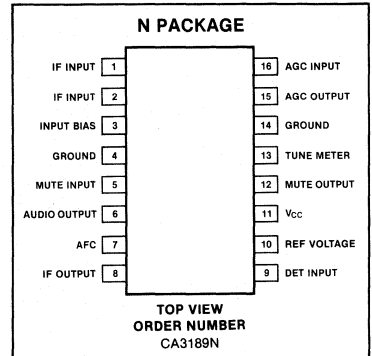
- AGC threshold controlled externally
- Low signal or fre. muting option
- Single coil tuning capability

- Exceptional limiting sensitivity: 10 μ V typical at -3dB point
- Low distortion: 0.1% with double tuned coil
- High recovered audio: 500mV typical
- Internal supply/voltage regulators
- Mute—center channel detect

APPLICATIONS

- Automotive FM receivers
- High fidelity FM receivers
- Communications FM receivers

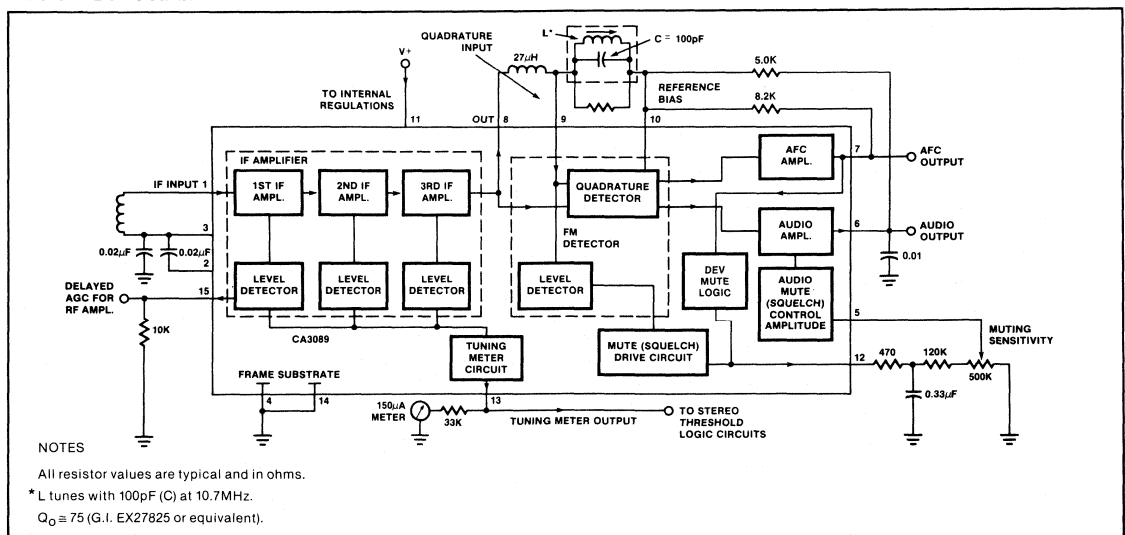
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
DC supply voltage: Between terminals 11 and 4	18	V
Between terminals 11 and 14	18	V
DC current (out of terminal 15)	2	mA
Device dissipation: Up to T _A = 60 °C	600	mW
Above T _A = 60 °C	derate linearly 6.7	mW/°C
Ambient temperature range: Operating	-40 to +85	°C
Storage	-65 to +150	°C
Lead temperature (during soldering): At distance not less than 1/32" (0.79mm) from case for 10 seconds max	+265	°C

BLOCK DIAGRAM



FM/IF SYSTEM

CA3189

STATIC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V^+ = 12\text{V}$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	Min	Typ	Max	UNIT
I_{11}	Quiescent circuit current	No signal input, non-muted	16	28	40	mA
DC Voltages: ⁴						
V1	Terminal 1 (IF input)	No signal input, non-muted	1.2	1.9	2.4	V
V2	Terminal 2 (AC return to input)	No signal input, non-muted	1.2	1.9	2.4	V
V3	Terminal 3 (DC bias to input)	No signal input, non-muted	1.2	1.9	2.4	V
V7	Terminal 7 (AFC)	No signal input, non-muted	5.0	5.6	6.0	V
V10	Terminal 10 (DC reference)	No signal input, non-muted	5.0	5.6	6.0	V

DYNAMIC CHARACTERISTICS

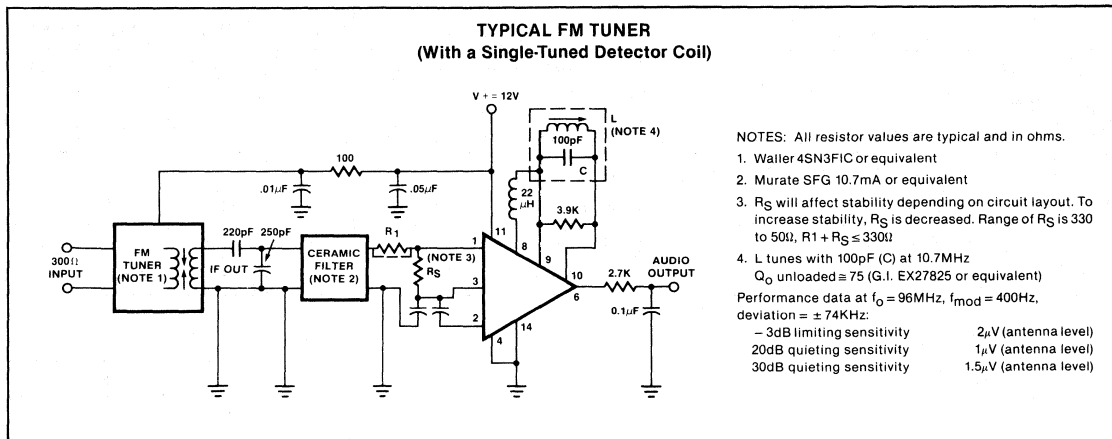
$V_{(lim)}$	Input limiting voltage (-3dB point) ³			10	25	μV	
AMR	AM rejection (terminal 6) ³	$V_{IN} = 0.1\text{V}$, $F_o = 10.7\text{MHz}$, $f_{mod} = 400\text{Hz}$, AM Mod = 30%	45	55		dB	
V_O	Recovered audio voltage (terminal 6) ³		325	500	650	mV	
Total harmonic distortion: ¹							
THD	Single tuned (terminal 6) ³			0.5	1.0	%	
THD	Double tuned (terminal 6) ⁴	$f_{mod} = 400\text{Hz}$, $V_{IN} = 0.1\text{V}$		0.1		%	
S+N/N	Signal plus noise to noise ratio (terminal 6) ³	Deviation— $\pm 75\text{KHz}$	65	72		dB	
MU	Mute (terminal 6)	$V_5 = 2.5\text{V}$	50	70		dB	
MU_{OUT}	Mute output (terminal 12)	$V_{IN} = 100\mu\text{V}$ $V_{IN} = 0\text{V}$	4.0	0.1	0.7	V	
MUF	Deviation mute frequency	$V_{IN} = 0.1\text{V}$, $f = 10.7\text{KHz}$		± 40		KHz	
MTR	Meteroutput (terminal 13)	$V_{IN} = 0.1\text{V}$ $V_{IN} = 500\mu\text{V}$ $V_{IN} = 0\text{V}$	3.0 1.0	4.0 1.5 0.3	0.7	V	
AGC	Delayed AGC (terminal 15)	$V_{16} > 2.5\text{V}$ $V_{16} < 0.7\text{V}$	8.0	0.2 10.0	0.7	V	
AGC	Threshold (terminal 16)	$V_{15} = \text{low to high}$		1.25	2.5	V	
CS	On-channel step (terminal 12)	$V_{IN} = 0.1\text{V}$ $f = 10.7\text{MHz}$	$f_{DEV} < \pm 15\text{KHz}$		0	0.7	V
			$f_{DEV} > \pm 80\text{KHz}$	4.5	5.6		

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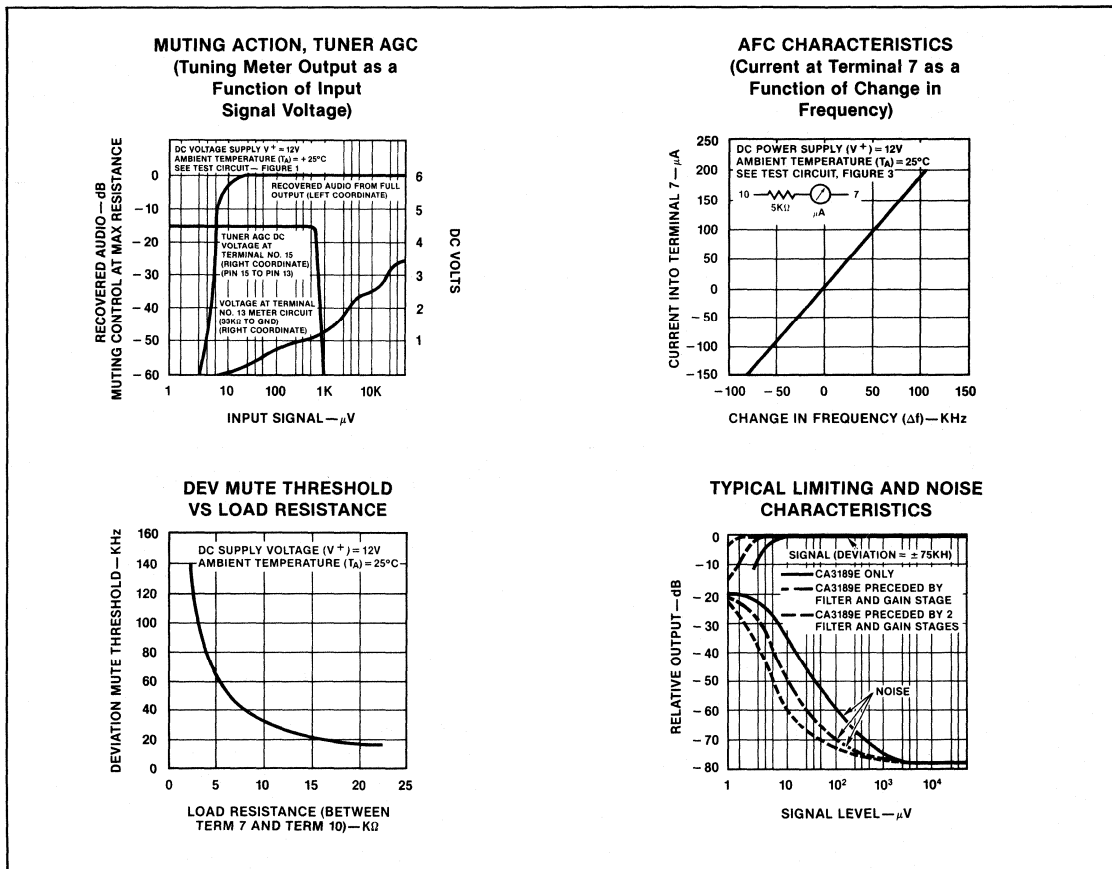
FM/IF SYSTEM

CA3189

TEST CIRCUITS



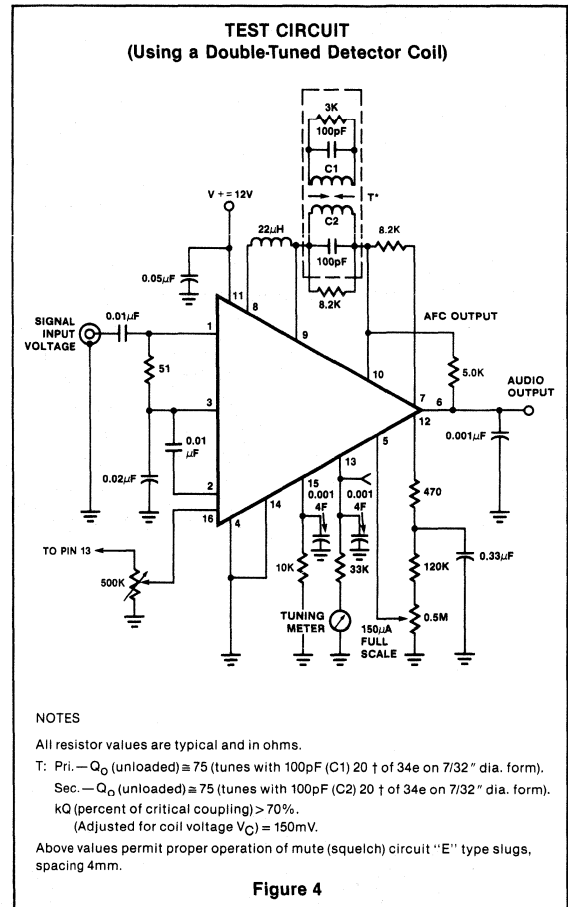
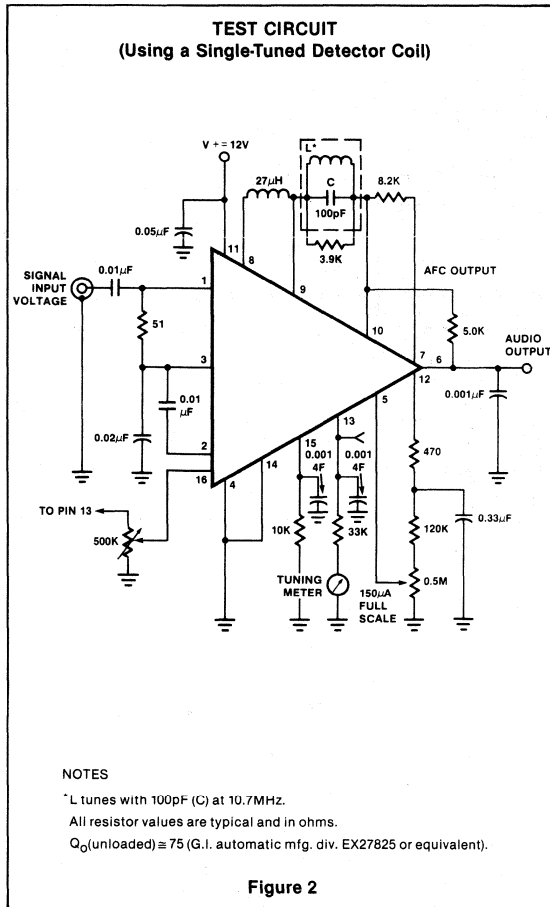
TYPICAL PERFORMANCE CHARACTERISTICS



FM/IF SYSTEM

CA3189

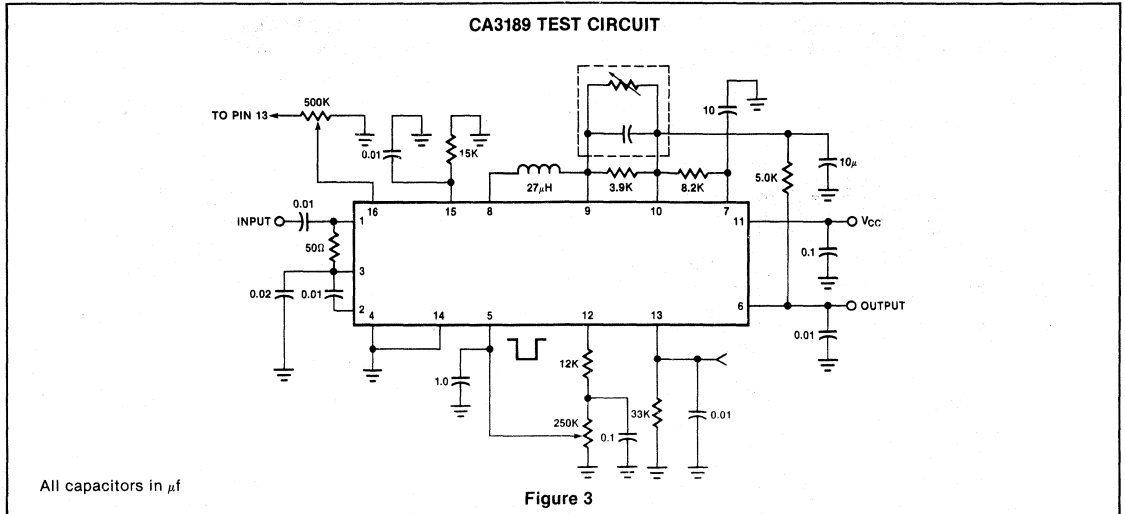
TEST CIRCUITS



FM/IF SYSTEM

CA3189

TEST CIRCUITS



STEREO DEMODULATOR WITH BLEND

LM1870

DESCRIPTION

The LM1870 combination FM Stereo Demodulator and Blend Circuit is a PLL circuit with a D.C. control pin whose purpose is to reduce switching noise by decreasing separation under low signal amplitude conditions. The part is designed specifically for automobile applications where fluctuating signal strength can cause demodulation noise.

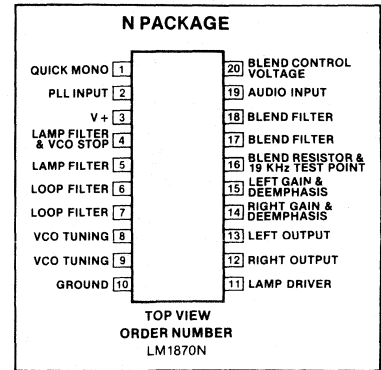
FEATURES

- Stereo blend control
- Wide input dynamic range
- Low total harmonic distortion
- VCO disable function
- Monophonic override pin
- Supply range 7V-15V

APPLICATIONS

- Auto radios
- High fidelity tuners
- High performance portable radios
- Electronic tuned radios

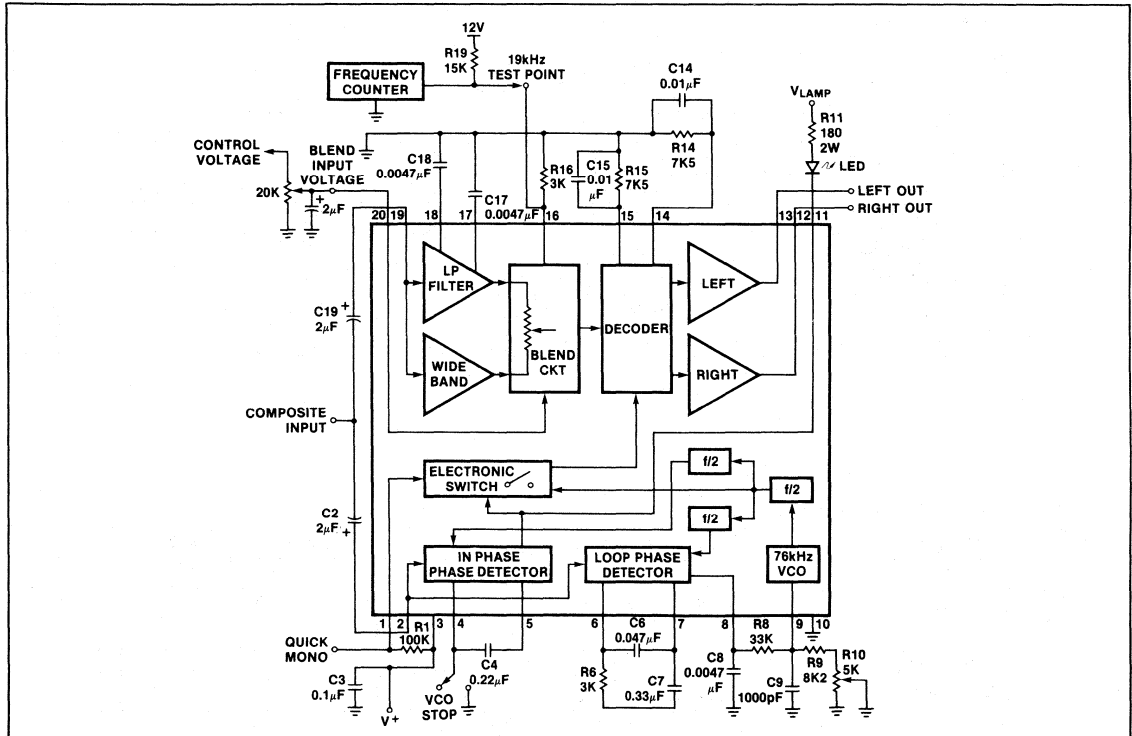
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, pin 3	15	V
Lamp driver voltage, pin 11	18	V
Output voltage, pin 12, 13 supply off	7	V
Quick mono input (pin 20)	V+ (pin 3)	V
Blend input (pin 20)	15	V
Operating temperature range	0°C to +70°C	
Power dissipation (note 1)	1	W
Storage temperature	-65°C to +125°C	
Lead temperature (soldering, 10 seconds)	300°C	

TYPICAL APPLICATION AND TEST CIRCUIT



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STEREO DEMODULATOR WITH BLEND**LM1870****DC ELECTRICAL CHARACTERISTICS** $T_A = 25^\circ\text{C}$, $V^+ = 8\text{V}$ unless otherwise noted (Figure 1)

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating supply voltage		7	8	15	V
Supply current			26	45	mA
Input DC voltage	Pin 19		4		V
Input DC voltage	Pin 2		1.8		V
Supply rejection		15	30		dB
Lamp leakage current	Lamp off, pin 11 = 16V		0.1	100	μA
Lamp saturation voltage	Lamp on, pin 11 @ 75mA		1.4	2.0	V
VCO stop voltage	Voltage @ pin 4 to stop VCO	0.2	0.4		V
VCO stop current	Pin 4 = 0.2V		-30	-100	μA
Blend input bias current			-2	-20	μA
Quick mono switch voltage			4		V
Quick mono bias current	Pin 1 = 8V		2		μA
Output leakage	Pin 12 or 13 = 6.5V, pin 3 = 0V		0.1	20	μA

AUDIO ELECTRICAL CHARACTERISTICS

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Mono gain	1kHz	-4	-1	+2	dB
Mono THD	1kHz @ 200mVrms		0.05	0.25	%
Channel balance			± 0.4	± 1.5	dB
Gain shift	Mono to stereo		± 0.1	± 1.0	dB
Channel separation	Pin 20 $\geq 1.1\text{V}$	30	45		dB
Output DC shift	Mono to stereo		± 15	± 100	mV
Input resistance	Pin 19	20	40		k Ω
Output resistance	Pin 12, 13		65	200	Ω
Ultrasonic rejection	19kHz + 38kHz		30		dB
SCA rejection	(Note 2)		70		dB
Signal to noise	1kHz @ 200mVrms MONO		68		dB

PLL ELECTRICAL CHARACTERISTICS

SYMBOL AND PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Lamp ON voltage	19kHz on pin 2		15	20	mV
Lamp OFF voltage	19kHz on pin 2	2.5	5		mV
Lamp hysteresis			10		dB
Capture range	25mVrms on pin 2	± 2	± 4	± 6	%
Hold in range	25mVrms on pin 2		± 12		%
Input resistance	Pin 2	8	14		k Ω

STEREO DEMODULATOR WITH BLEND

LM1870

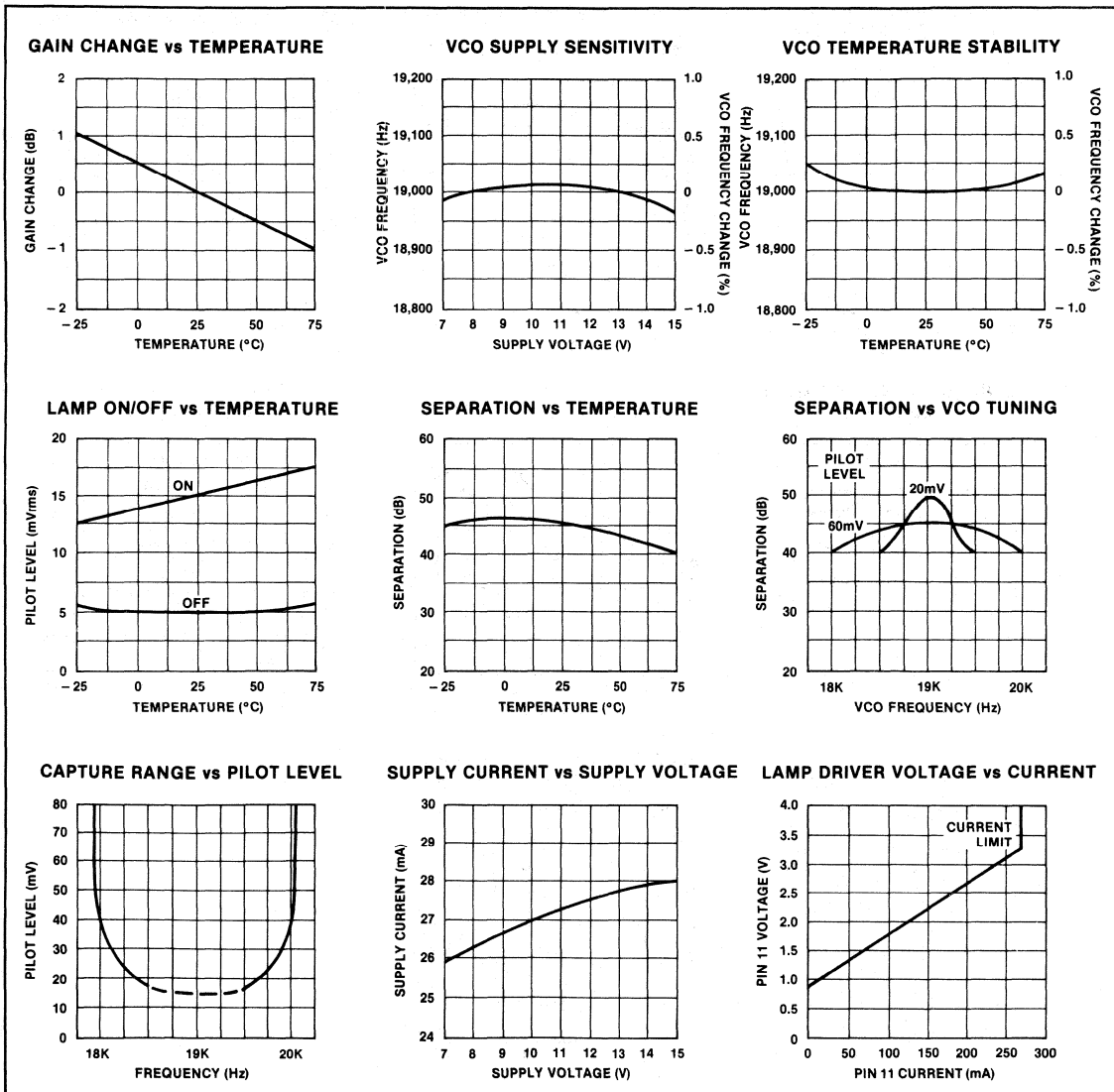
BLEND ELECTRICAL CHARACTERISTICS

SYMBOL AND PARAMETER	TEST CONDITIONS (Pin 20 from 1.1V to 0.2V)	MIN	TYP	MAX	UNIT
Stereo gain change	1kHz L = - R input	- 25	- 35		dB
Mono gain change	1kHz L = R input	- 1.5	- 0.5	0.5	dB
	10kHz L = R input	- 8	- 14	- 20	dB
Output DC shift			± 40	± 100	mV

NOTES

- For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 125°C/W junction to ambient.
- Input is 10% SCA (74.5kHz), 9% pilot and 1kHz left or right. Rejection is ratio of 1kHz output to 1.5kHz output.

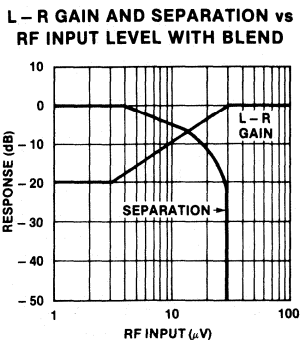
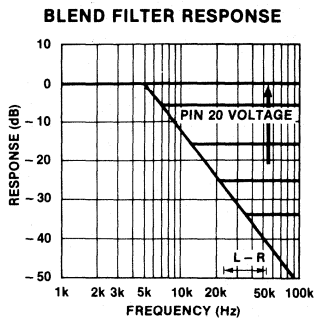
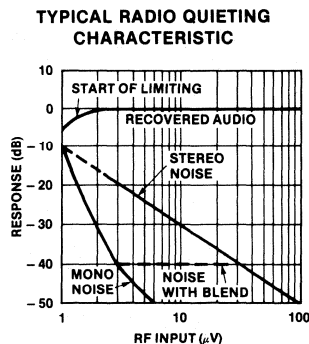
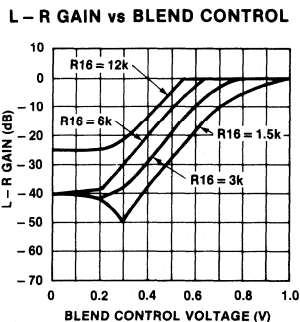
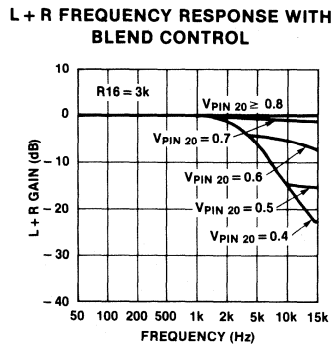
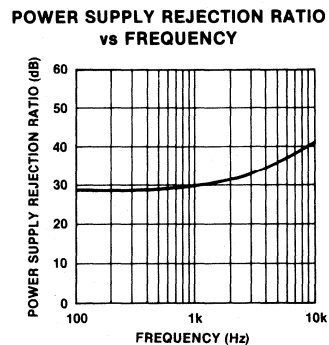
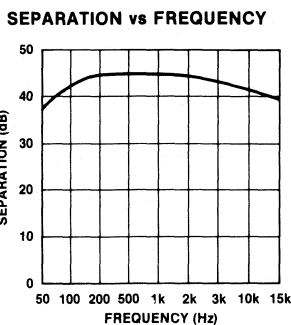
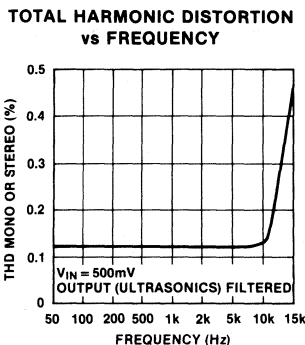
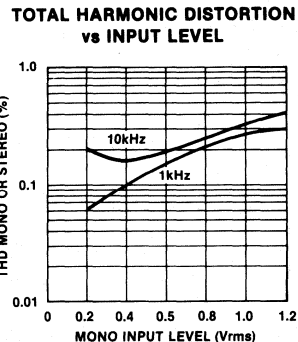
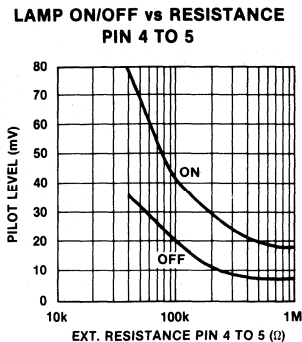
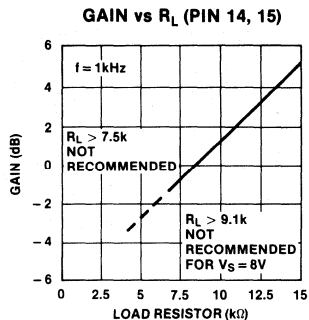
TYPICAL CHARACTERISTICS



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STEREO DEMODULATOR WITH BLEND

LM1870



BALANCED MODULATOR-DEMODULATOR

MC1496/MC1596

DESCRIPTION

The MC1496 is a monolithic Double-Balanced Modulator/Demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The MC1596 will operate over the full military temperature range of -55°C to +125°C. The MC 1496 is intended for applications within the range of 0°C to +70°C.

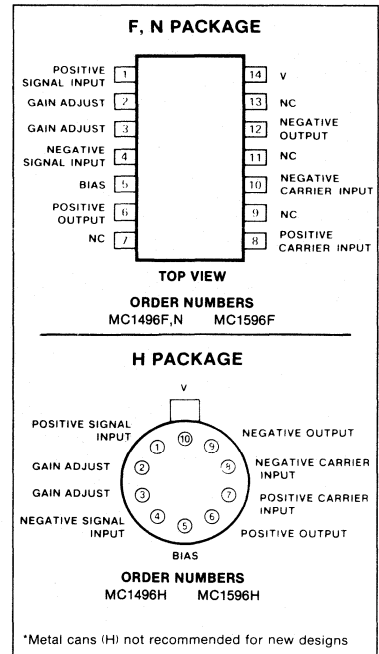
FEATURES

- Excellent carrier suppression
65dB typ @ 0.5MHz
50dB typ @ 10MHz
- Adjustable gain and signal handling
- Balanced inputs and outputs
- High common-mode rejection—85dB typ

APPLICATIONS

- Suppressed carrier and amplitude modulation
- Synchronous detection
- FM detection
- Phase detection
- Sampling
- Single sideband
- Frequency doubling

PIN CONFIGURATIONS



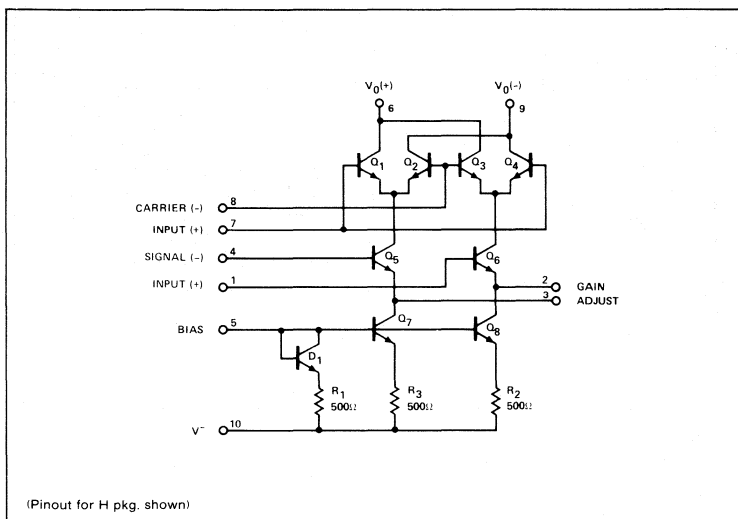
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Applied voltage ^{1,2}	30	V
Differential input signal (V ₇ -V ₈)	±5.0	V
Differential input signal (V ₄ -V ₁)	(5 ± 1 ₅ R _e)	V
Input signal (V ₂ -V ₁ , V ₃ -V ₄)	5.0	V
Bias current (I ₅)	10	mA
Power dissipation (pkg. limitation)		
N package	900	mW
Operating temperature range		
MC1496	0 to +70	°C
MC1596	-55 to +125	°C
Storage temperature range	-65 to +150	°C

NOTES

1. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
2. Pin number references pertain to H package pinout only.

EQUIVALENT SCHEMATIC



BALANCED MODULATOR-DEMODULATOR

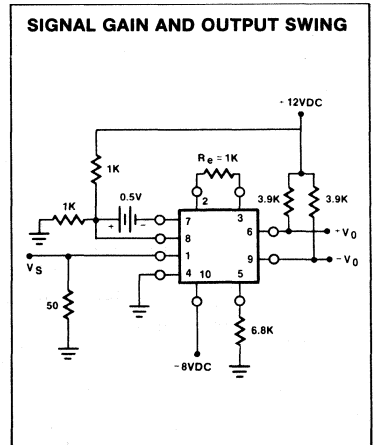
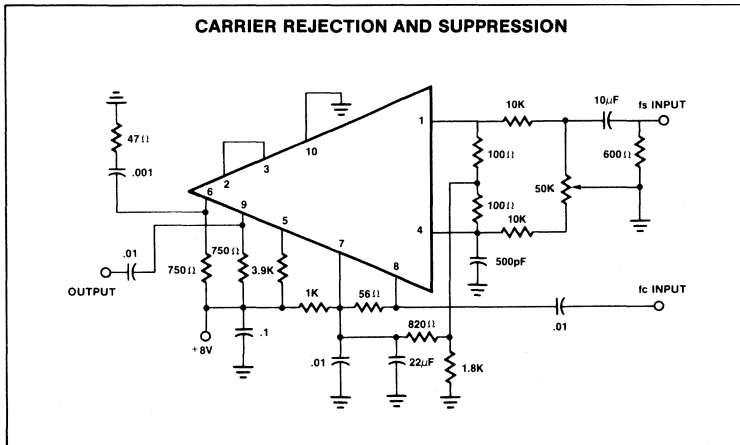
MC1496/MC1596

DC ELECTRICAL CHARACTERISTICS $V^+ = +12Vdc$, $V^- = -8.0Vdc$, $I_5 = 1.0mAdc$, $R_L = 3.9k\Omega$, $R_e = 1.0k\Omega$, $T_A = 25^\circ C$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
		Min	Typ	Max	Min	Typ	Max	
R_{ip} C_{ip}	Single-ended input impedance Parallel input resistance Parallel input capacitance		200 2.0			200 2.0		$k\Omega$ pF
R_{op} C_{op}	Single-ended output impedance Parallel output resistance Parallel output capacitance		40 5.0			40 5.0		$k\Omega$ pF
I_{bS} I_{bC}	Input bias current $I_{bS} = \frac{I_1 + I_4}{2}$ $I_{bC} = \frac{I_7 + I_8}{2}$		12 12	25 25		12 12	30 30	μA μA
I_{ioS} I_{ioC}	Input offset current $I_{ioS} = I_1 - I_4$ $I_{ioC} = I_7 - I_8$		0.7 0.7	5.0 5.0		0.7 0.7	7.0 7.0	μA μA
T_{cIio} I_{oo}	Average temperature coefficient of input offset current Output offset current $I_6 - I_9$		2.0 14			2.0 15		$nA/^\circ C$ μA
T_{cIoo} V_o	Average temperature coefficient of output offset current Common-mode quiescent Output voltage (Pin 6 or Pin 9)		90 8.0			90 8.0		$nA/^\circ C$ Vdc
I_{D+} I_{D-}	Power supply current $I_6 + I_9$ I_{10}		2.0 3.0	3.0 4.0		2.0 3.0	4.0 5.0	$mAdc$
P_D	DC power dissipation		33			33		mW

NOTE

Pin number references pertain to H package pinout only.



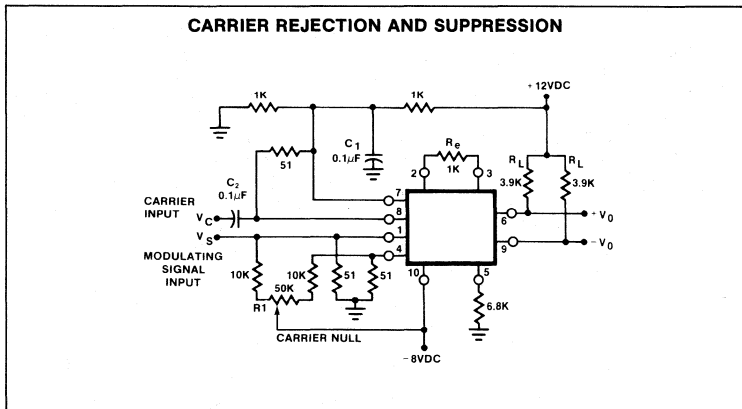
BALANCED MODULATOR-DEMODULATOR

MC1496/MC1596

AC ELECTRICAL CHARACTERISTICS $V^+ = +12Vdc$, $V^- = -9.0Vdc$, $I_S = 1.0mA$, $R_L = 3.9k\Omega$, $R_e = 1.0k\Omega$, $T_A = +25^\circ C$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	MC1596			MC1496			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{CFT} Carrier feedthrough	$V_C = 60mVrms$ sinewave and offset adjusted to zero $f_C = 1.0kHz$ $f_C = 10MHz$		40 140			40 140		$\mu Vrms$
	$V_C = 300mVp-p$ squarewave: Offset adjusted to zero $f_C = 1.0kHz$ Offset not adjusted $f_C = 1.0kHz$	0.04 20	0.2 100		0.04 20	0.4 200		$mVrms$
V_{CS} Carrier suppressions	$f_S = 10kHz$, $300mVrms$ sinewave $f_C = 500kHz$, $60mVrms$ sinewave $f_C = 10MHz$, $60mVrms$ sinewave	50	65 50		40	65 50		dB
BW_{3dB} Transadmittance bandwidth (Magnitude) ($R_L = 50\Omega$)	Carrier input port, $V_C = 60mVrms$ sinewave $f_S = 1.0kHz$,		300			300		MHz
	Signal input port, $V_S = 300mVrms$ sinewave $ V_C = 0.5Vdc$		80			80		MHz
AV_S Signal gain	$V_S = 100mVrms$; $f = 1.0kHz$ $ V_C = 0.5Vdc$	2.5	3.5		2.5	3.5		V/V
CMV Common-mode input swing ACM Common-mode gain	Signal port, $f_S = 1.0kHz$		5.0			5.0		$Vp-p$
	Signal port, $f_S = 1.0kHz$ $ V_C = 0.5Vdc$		-85			-85		dB
DV_{OUT} Differential output voltage swing capability			8.0			8.0		$Vp-p$

NOTE
Pin number references pertain to H package pinout only.



AM RECEIVER CIRCUIT

TCA440

DESCRIPTION

TCA440 is a monolithic IC, especially developed for AM receivers up to 30MHz. It includes a RF stage with AGC, a balanced mixer, separate oscillator and an IF amplifier with AGC. Because of its low current consumption and of its internal stabilization the TCA440 is perfectly suited for battery operated portables, car and home radios.

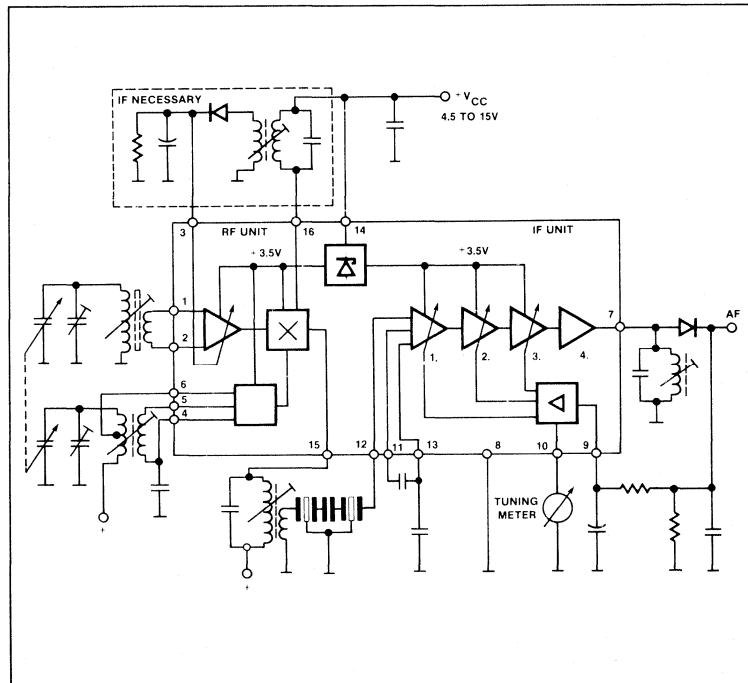
FEATURES

- **Balanced circuit**
- **Separately controllable prestage**
- **Multiplicative push-pull mixer with separate oscillator**
- **High signal handling capability even with 4.5V supply voltage**
- **100dB feedback control range in 5 stages**
- **Direct connection for tuning meter**
- **Minimum external components**

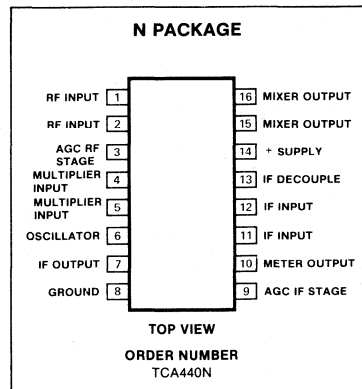
ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _{CC}	Supply voltage	15	V
T _{amb}	Ambient temperature in operation	-15 to +80	°C
T _s	Storage temperature	-30 to +125	°C
V _{CC}	Range of operation	4.5 to 15	V

BLOCK DIAGRAM



PIN CONFIGURATION



TUNING METER

Recommended instruments:

- 500 μ A ($R_1 = 800\Omega$)
- 300 μ A ($R_1 = 1.5k\Omega$)

The IC offers at pin 10 a tuning meter voltage of 600 mV_{EMF} max. with a source impedance of approx. 400 Ω .

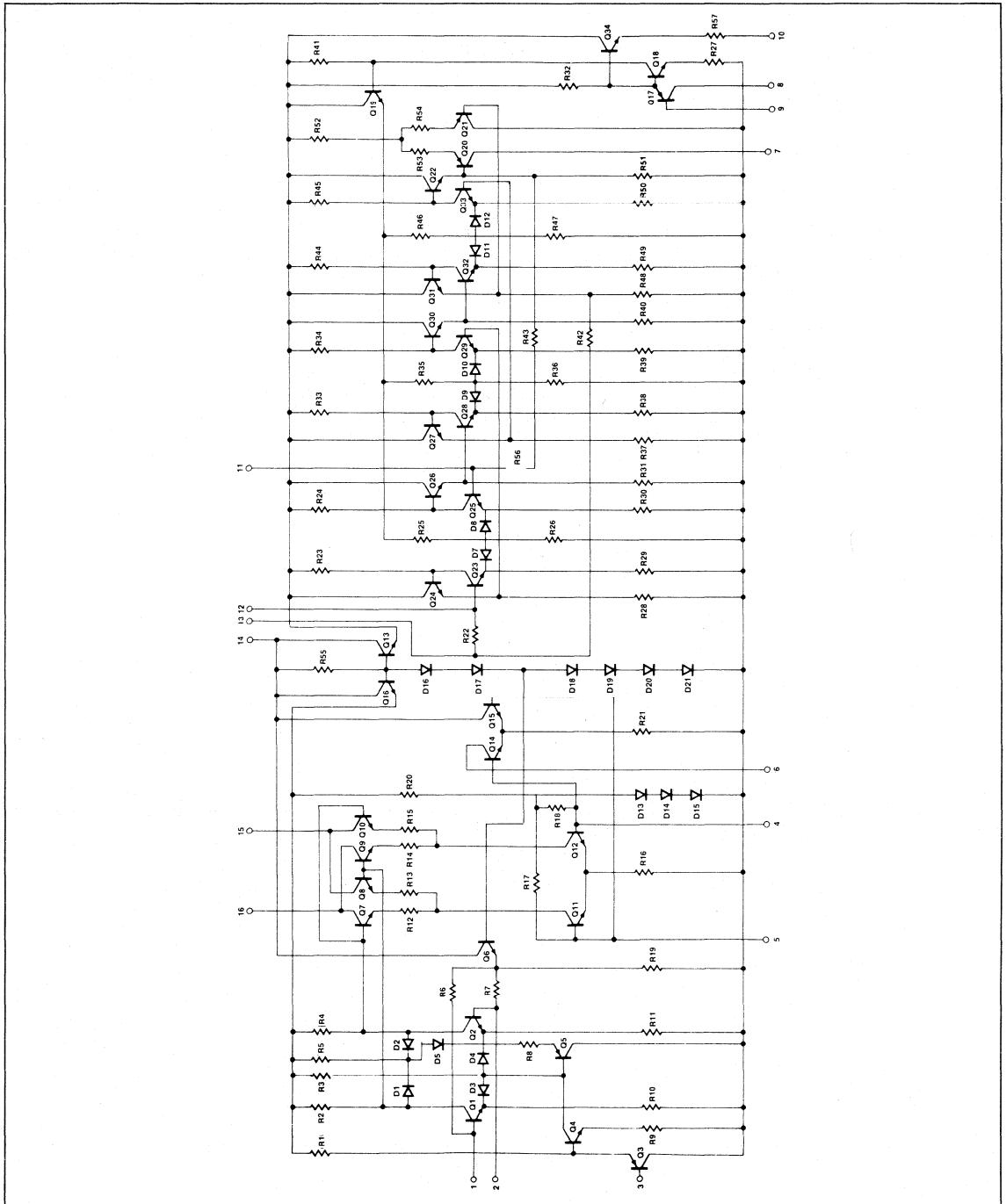
FUNCTION

As pictured in the circuit diagram the TCA440 comprises two control loops independent of each other which control the RF stage and the IF stages. By AGCing the RF stage, excellent signal handling is obtained. A voltage of 2.6V_{pp} on the IC input can be handled with very low distortion. The push-pull mixer operates multiplicatively, thereby resulting in few harmonic mixing products and whistling points. The oscillator which is separated from the mixer is also apted excellently for short waves. From the AGC of the RF amplifier a voltage is derived for a tuning meter which can be connected directly to the meter. The symmetric composition of the circuit provides high stability against oscillation and, at the same time, an AGC range of more than 100dB. The bridge circuit of the mixer provides good isolation of the oscillator.

AM RECEIVER CIRCUIT

TCA440

EQUIVALENT SCHEMATIC



AM RECEIVER CIRCUIT

TCA440

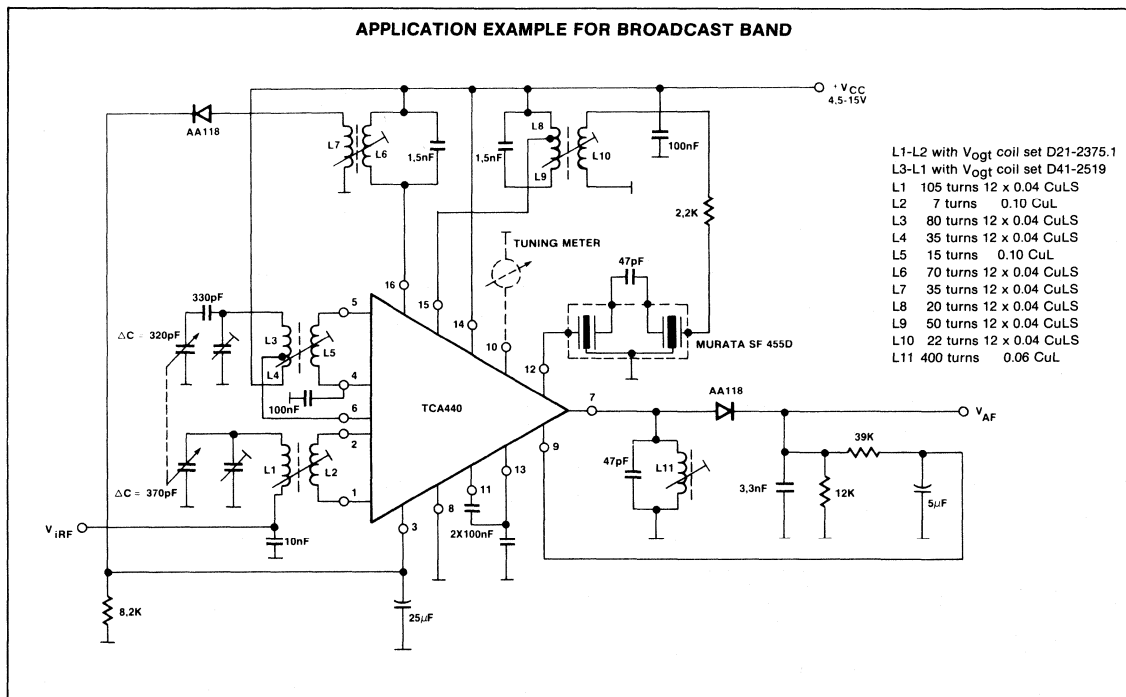
DC ELECTRICAL CHARACTERISTICS $V_{CC} = 9V, T_A = 25^\circ C$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	TCA 440			UNIT
		Min	Typ	Max	
I_{CC} Total current consumption at:	$V_{CC} = 4.5V$		7		mA
	$V_{CC} = 9V$		10.5		mA
	$V_{CC} = 15V$		12		mA

AC ELECTRICAL TEST $V_{CC} = 9V, T_A = 25^\circ C, f_c = 1MHz, f_{MOD} = 1kHz$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	TCA 440			UNIT
		Min	Typ	Max	
V_O Audio output voltage	$m = 30\% \quad V_{IN} = 1.0mV$		100		mV
SEN Input sensitivity ($f_c = 1MHz, m = 30\%/0\%, R_G = 540\Omega$)	$V_O = 30mV$		10		μV
Noise	$V_{IN} = 1.0mV$ NO MOD.		1.5		mV
M_O Meter Output	$V_{IN} = 4\mu V$		150		μV

TYPICAL APPLICATIONS

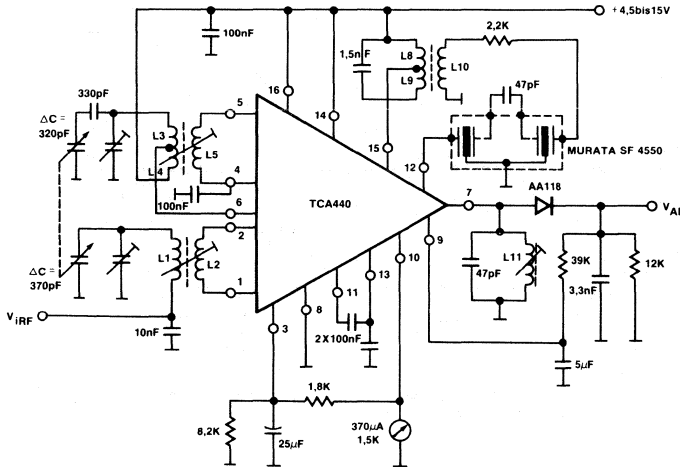


AM RECEIVER CIRCUIT

TCA440

TYPICAL APPLICATIONS (Cont'd)

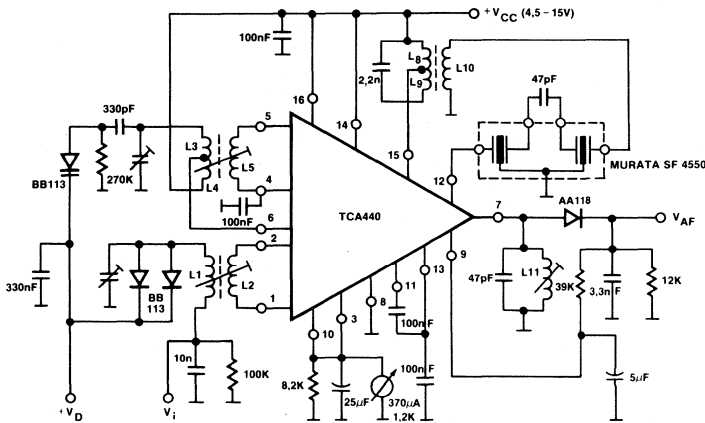
APPLICATION EXAMPLE FOR BROADCAST BAND



Prestage control is derived from IF control

- L1 105 turns 12 x 0.04 CuLS
- L2 7 turns 0.10 CuL
- L3 80 turns 12 x 0.04 CuLS
- L4 35 turns 12 x 0.04 CuLS
- L5 15 turns 0.10 CuL
- L8 20 turns 12 x 0.04 CuLS
- L9 50 turns 12 x 0.04 CuLS
- L10 22 turns 12 x 0.04 CuLS
- L11 400 turns 0.04 CuL
- L1-L2 with Vogt coil set D21-23751
- L3-L11 with Vogt coil set D41-2519

APPLICATION EXAMPLE FOR AM USING VARICAP DIODES BB 113



- L1 105 turns 12 x 0.04 CuLS
- L2 7 turns 0.10 CuL
- L3 80 turns 12 x 0.04 CuLS
- L4 35 turns 12 x 0.04 CuLS
- L5 15 turns 0.10 CuL
- L8 20 turns 12 x 0.04 CuLS
- L9 50 turns 12 x 0.04 CuLS
- L10 22 turns 12 x 0.04 CuLS
- L11 400 turns 0.06 CuL

L1-L2 with Vogt coil set D21-23751
L3-L11 with Vogt coil set D41-2519

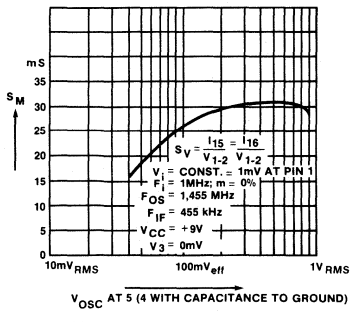
$V_D = 8.5V - f_i = 800kHz$
 $V_D = 30V - f_i = 1620kHz$

AM RECEIVER CIRCUIT

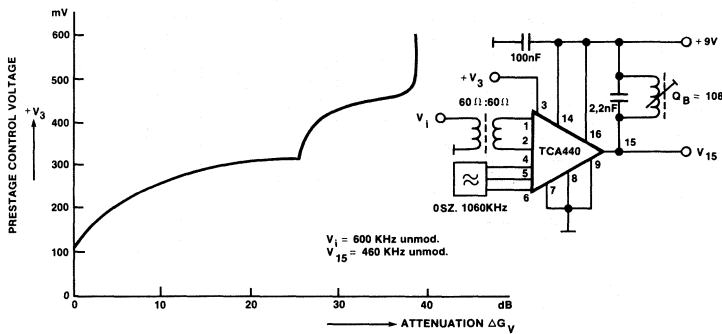
TCA440

TYPICAL APPLICATIONS (Cont'd)

CONVERSION CONDUCTANCE vs OSCILLATOR VOLTAGE

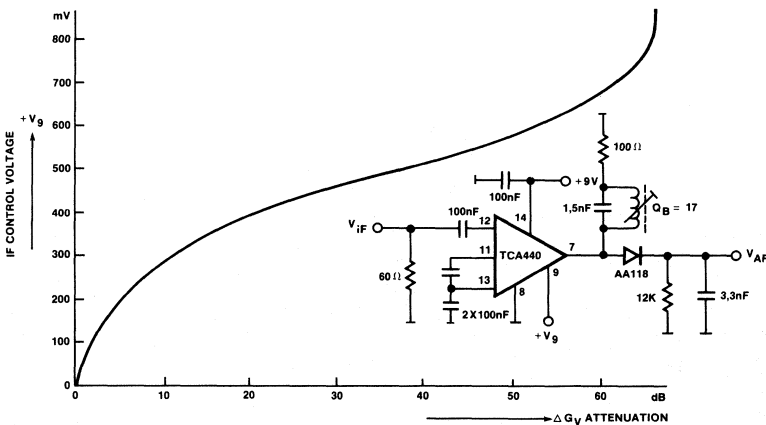


RF STAGE CONTROL



The input is not power matched and can be driven with a higher resistance, V_i is chosen so that a constant V_{15} is obtained (50mV_{pp}).

IF CONTROL



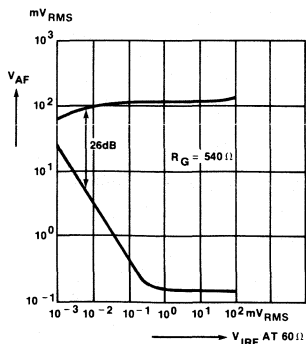
V_{iF} (469kHz; $m = 80\%$; $f_{mod} = 1kHz$) is chosen so that always a constant V_{AF} is obtained (200mV_{RMS})

AM RECEIVER CIRCUIT

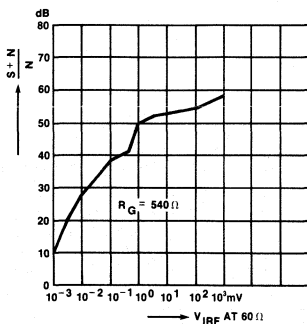
TCA440

TYPICAL PERFORMANCE CHARACTERISTICS

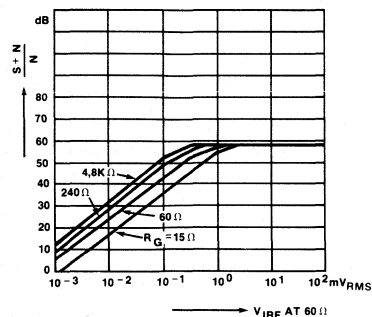
AF OUTPUT VOLTAGE AND NOISE FIGURE vs RF INPUT VOLTAGE (switching position 1)



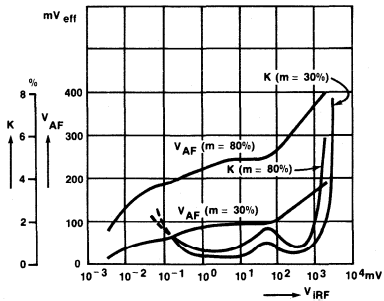
SIGNAL TO NOISE RATIO vs RF INPUT VOLTAGE (switching position 2)



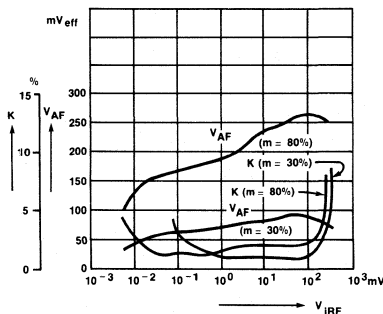
SIGNAL TO NOISE RATIO vs RF INPUT VOLTAGE (parameter is generator impedance) (switching position 1)



TEST FIGURES FOR APPLICATION EXAMPLE FOR MW HARMONIC DISTORTION AND AF OUTPUT VOLTAGE vs RF INPUT VOLTAGE MEASURED SYMMETRICALLY AT PINS 1 AND 2 $f_i = 1\text{MHz}$, $f_{mod} = 1\text{kHz}$, $f_{IF} = 455\text{kHz}$, $V_{CC} = 9\text{V}$



TEST FIGURES FOR APPLICATION EXAMPLE FOR AM USING BB 113 $f_i = 1\text{MHz}$, $f_{mod} = 1\text{kHz}$, $f_{IF} = 455\text{kHz}$, $V_{CC} = 9\text{V}$, V_{IRF} measured symmetrically at pins 1 and 2

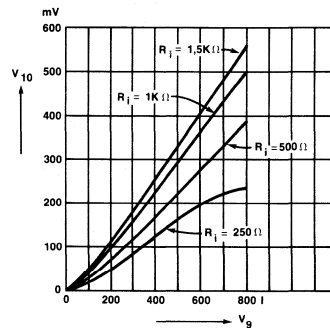


Example for moving coil instruments

R_i for full-scale deflection

1.5kΩ	100μA
1.5kΩ	170μA
2kΩ	200μA
350Ω	500μA

TUNING METER VOLTAGE vs IF CONTROL VOLTAGE (parameter is impedance of tuning meter)

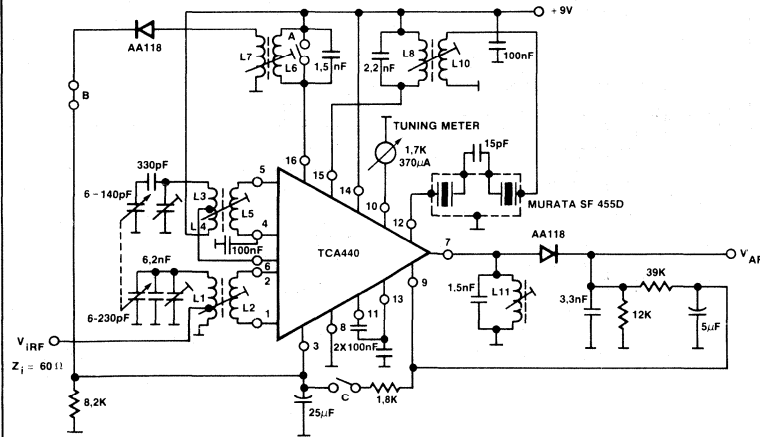


AM RECEIVER CIRCUIT

TCA440

TEST CIRCUITS

TEST CIRCUIT FOR NOISE FIGURE



L1-L2 M25 pot core
L3-L11 with Vogt coil set D41-2519

L1	2 + 6	turns	6 x 12 x 0.04 CuLS
L2	n		0.15 CuL
L3	90	turns	12 x 0.04 CuLS
L4	35	turns	12 x 0.04 CuLS
L5	15	turns	0.10 CuL
L6	70	turns	12 x 0.04 CuLS
L7	35	turns	12 x 0.04 CuLS
L8	60	turns	12 x 0.04 CuLS
L10	22	turns	12 x 0.04 CuLS
L11	68	turns	0.06 CuL

switch
A B C
off on off separate RF stage control
on off on RF stage control voltage derived from IF control voltage

f_i = 1MHz; m = 30%

n(turns)	R _{Generator} (Ω)
1	15
2	60
4	240
6	540
9	1.2K
12	2.2K
18	4.8K

FM STEREO MULTIPLEX DECODER, PHASE LOCKED LOOP

μ A758

DESCRIPTION

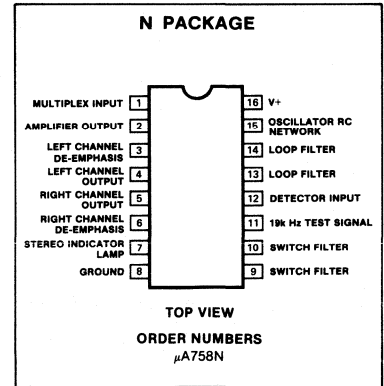
The μ A758 is a monolithic phase-locked loop FM stereo multiplex decoder. The device decodes an FM stereo multiplex signal into right and left audio channels while inherently suppressing SCA information when it is contained in the composite input signal. The device includes automatic mono-stereo mode switching and drive for an external lamp to indicate stereo mode operation.

The μ A758 operates over a large voltage range and requires a minimum number of external components. A simple setting of an external potentiometer adjusts the oscillator frequency. No coils are required.

FEATURES

- 45dB channel separation
- Automatic stereo/mono switching
- 70dB SCA rejection
- 10V to 16V supply range
- High impedance input—low impedance output

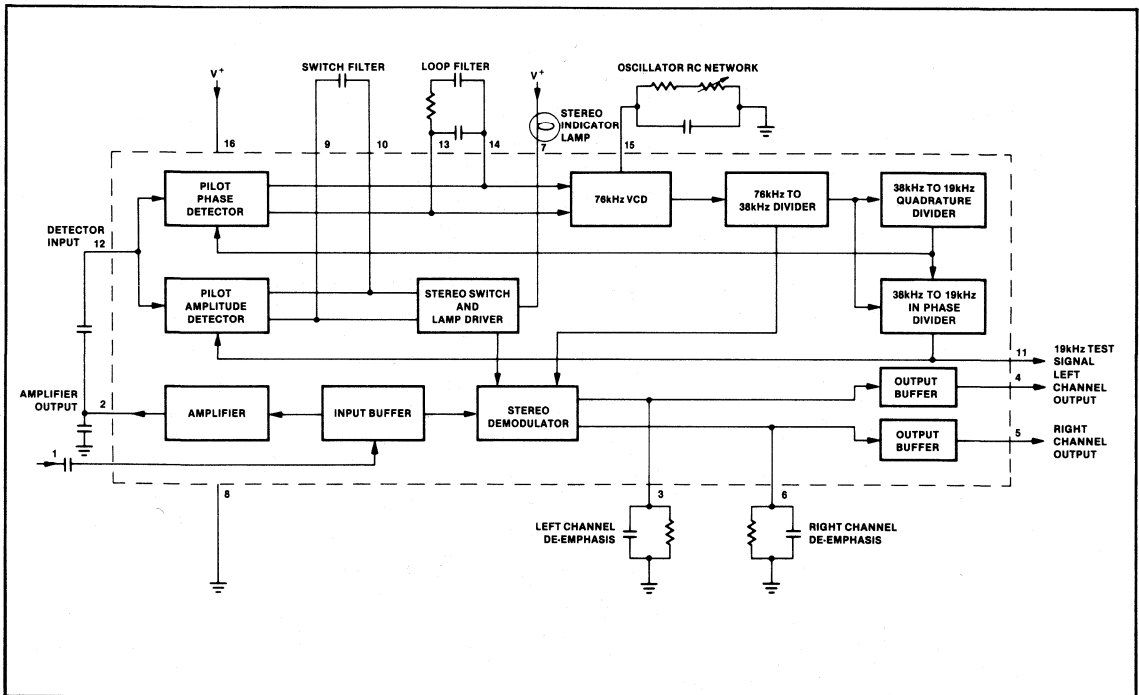
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+18	V
Supply voltage (\leq 15 seconds)	+22	V
Voltage at lamp driver terminal (Lamp OFF)	+22	V
Internal power dissipation	730	mW
Operating temperature range	-40 to +85	$^{\circ}$ C
Storage temperature range	-55 to +125	$^{\circ}$ C
Lead temperature (60sec)	300	$^{\circ}$ C

BLOCK DIAGRAM

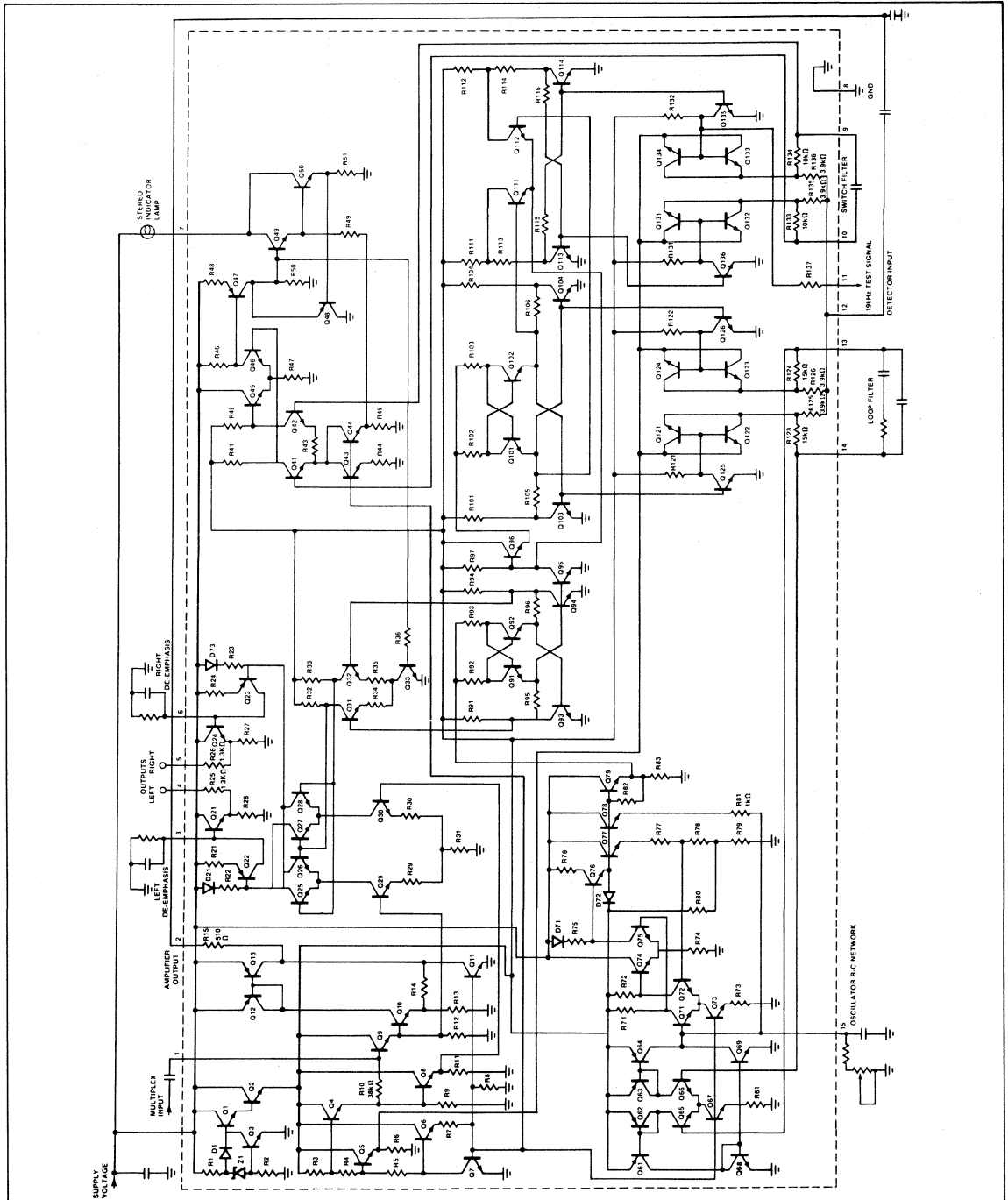


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FM STEREO MULTIPLEX DECODER, PHASE LOCKED LOOP

μA758

EQUIVALENT SCHEMATIC



FM STEREO MULTIPLEX DECODER, PHASE LOCKED LOOP

μ A758

DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, $V_+ = +12\text{V}$, 19kHz pilot level = 30mVRMS, multiplex signal (L = R, pilot OFF) = 300mVRMS, modulation frequency = 400Hz or 1Hz, test circuit 1, unless otherwise specified.

PARAMETER	TEST CONDITIONS	μ A758			UNIT
		Min	Typ	Max	
I_{CC} Supply current	Lamp OFF		31	38	mA
I_L Maximum available lamp current		75	150		mA
V_7 Voltage at lamp driver terminal	Lamp = 50mA		1.3	1.8	V
r_i Input resistance		20	35		k Ω
r_o Output resistance		0.9	1.3	2.0	k Ω

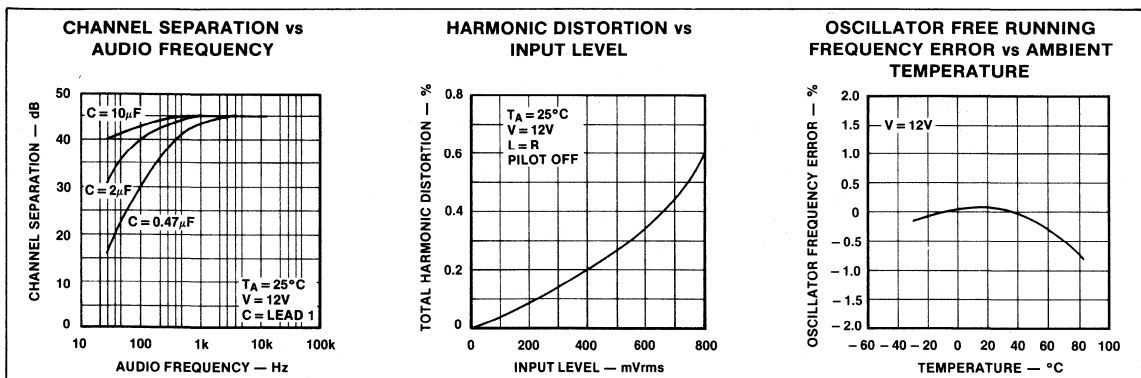
AC ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	μ A758			UNIT
		Min	Typ	Max	
$\Delta(V_4 \& V_5)$ DC voltage shift at either output terminal	Stereo to mono operation		30	150	mV
$P_{S.R.R.}$ Power supply ripple rejection SEP Channel separation	200Hz, 200mVRMS	35	40		dB
	100Hz	30	45		dB
	400Hz		45		dB
	10kHz		0.3	1.5	dB
$BAL.$ Channel balance					
A_v Voltage gain	1kHz	0.5	0.9	1.4	V/V
Pilot input level	Lamp turn-on		18	25	mVRMS
	Lamp turn-off	2.0	7.0		mVRMS
Pilot input level hysteresis	Lamp turn-off to turn-on	3.0	7.0		dB
T.H.D. Total harmonic distortion	Capture range	2.0	4.0	6.0	%
	Multiplex level = 600mVRMS pilot OFF		0.4	1.0	%
19kHz rejection 38kHz rejection SCA rejection ¹		25	35		dB
		25	45		dB
			70		dB
VCO Tuning resistance ²		21.0	23.3	25.5	k Ω
VCO Frequency drift	$0^\circ\text{C} \leq T_A \leq 25^\circ\text{C}$		+0.1	± 2	%
	$25^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		-0.4	± 2	%

NOTES

- Measured with a stereo composite signal consistency of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on Broadcasting.
- Total resistance from pin 15 to ground, in test circuit, required to set reference frequency at pin 11 to 19kHz \pm 10hz.

TYPICAL PERFORMANCE CHARACTERISTICS

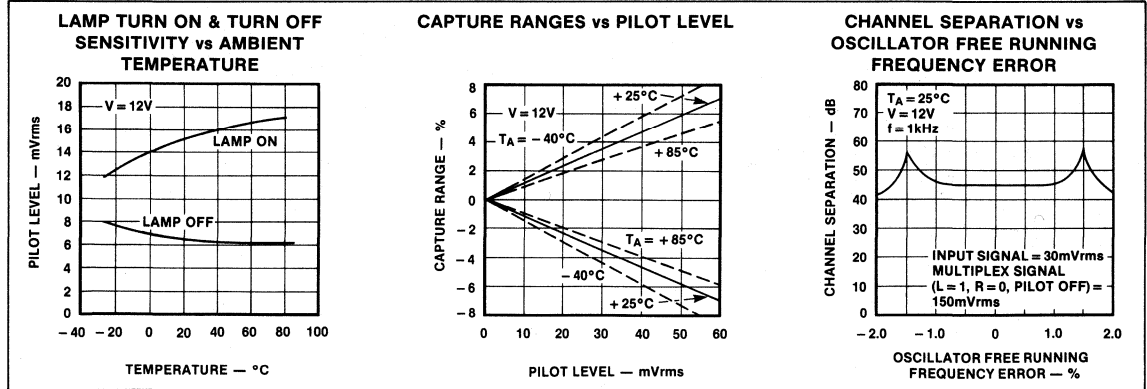


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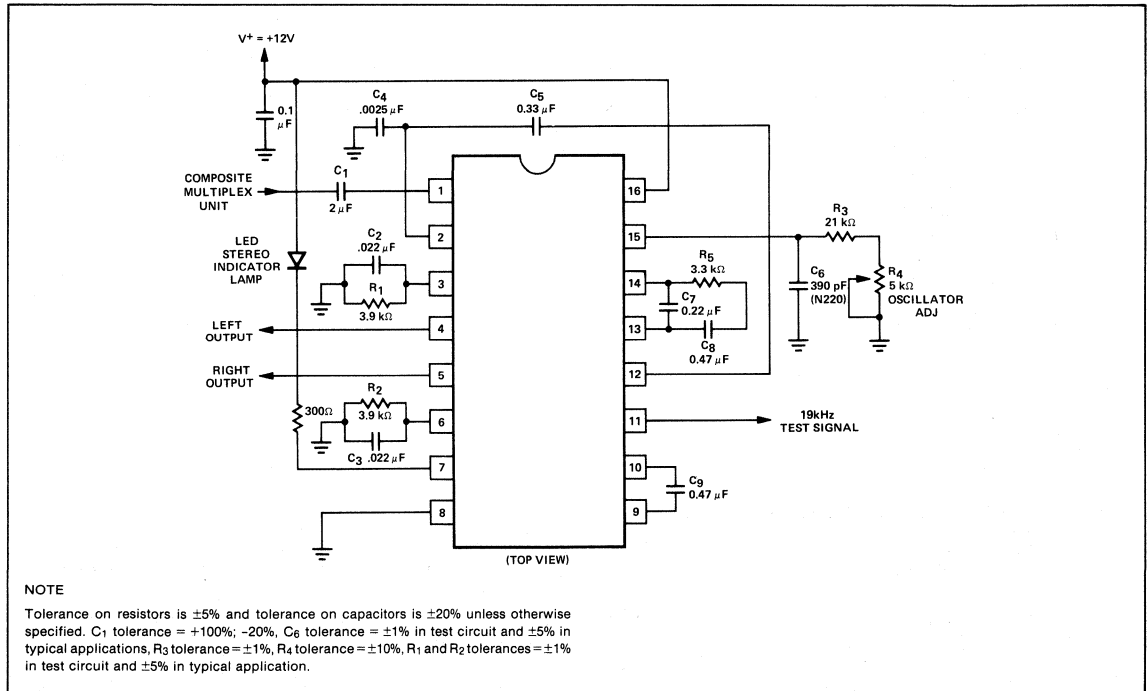
FM STEREO MULTIPLEX DECODER, PHASE LOCKED LOOP

μ A758

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



TEST CIRCUIT AND TYPICAL APPLICATION



Section 15 Audio Circuits

INDEX

Section 15 — Audio Circuits

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LM387	Dual Low-Noise Preamp	15-3
NE/SE540	Power Driver	15-7
NE542	Dual Low Noise Preamp	15-12
NE570/571/SA571	Companor	15-15
NE572	Programmable Analog Companor	15-17
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NE648/649	Low Voltage Dolby Noise Reduction Circuit	15-23
NE650	Dolby B/C Type Noise Reduction Circuit	15-27

DUAL LOW-NOISE PREAMP

LM387

DESCRIPTION

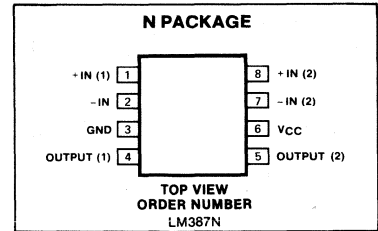
The LM387 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with an internal power supply decoupler-regulator, providing 110dB supply rejection and 60dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing ($V_{CC} - 2V$ p-p), and wide power bandwidth (75kHz, 20V p-p). The LM387 operates from a single supply across the wide range of 9 to 40V.

The amplifiers are internally compensated for all gains greater than 10. The LM387 is available in an 8 lead dual-in-line package.

FEATURES

- Low noise— $0.8\mu V$ total input noise
- High gain—104dB open loop
- Single supply operation
- Wide supply range 9 to 40V
- Power supply rejection—110dB
- Large output voltage swing ($V_{CC} - 2V$ p-p)
- Wide bandwidth 15MHz unity gain
- Power bandwidth 75kHz, 20V p-p
- Internally compensated
- Short circuit protected

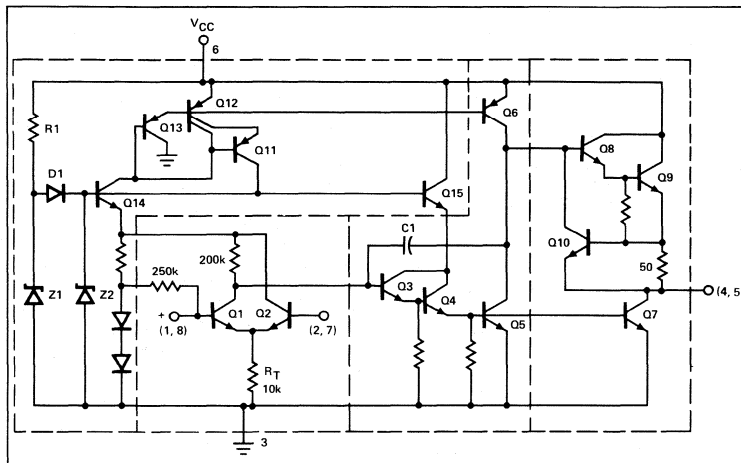
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+40	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

EQUIVALENT CIRCUIT



DUAL LOW-NOISE PREAMP

LM387

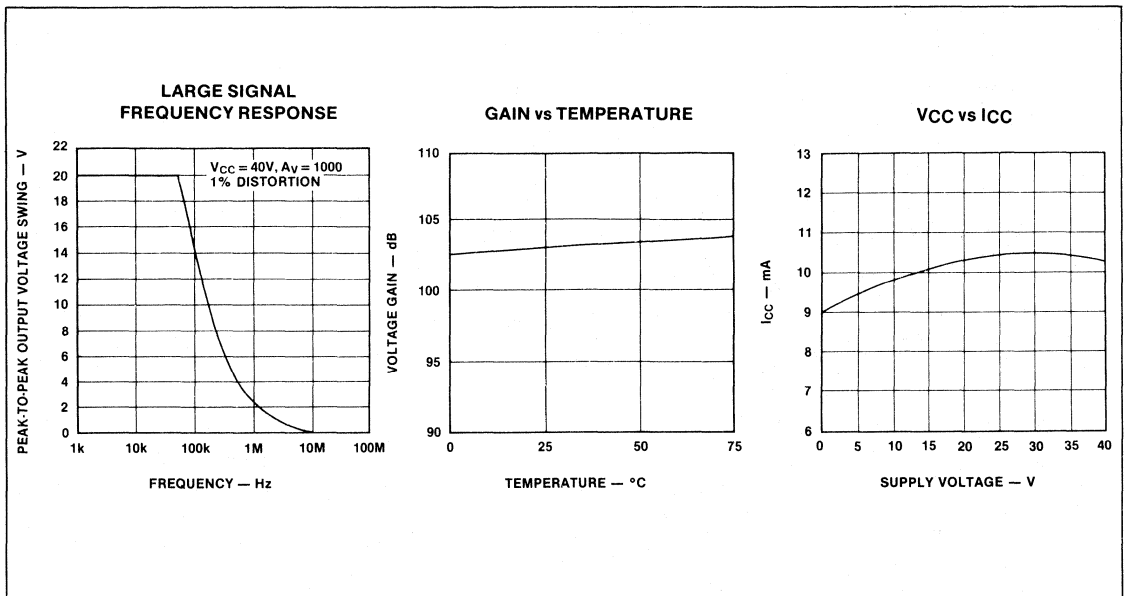
DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 14\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LM387			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Supply current	V_{CC} 9 to 40V, $R_L = \infty$		10		mA
Input resistance	Positive input		100		k Ω
	Negative input		200		k Ω
Input current	Negative input		0.5		μA
Output resistance	Open loop		150		Ω
Output current	Source		8		mA
	Sink		2		mA
Output voltage swing	Peak-to-peak		$V_{CC}-2$		V

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 14\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	LM387			UNIT
		Min	Typ	Max	
Small signal bandwidth	20V p-p ($V_{CC} = 24\text{V}$) Linear operation		15		MHz
Power bandwidth			75		kHz
Maximum input voltage					300
Supply rejection ratio	$f = 1\text{kHz}$		110		dB
Channel separation	$f = 1\text{kHz}$		60		dB
Total harmonic distortion	75dB gain, $f = 1\text{kHz}$		0.1		%
Total equivalent input noise	$R_S = 600\Omega$, 100-10,000Hz		0.8	1.4	μVrms
Noise figure	50k Ω , 100-10,000Hz		1.0		dB
	10k Ω , 100-10,000Hz		1.6		dB
	5k Ω , 100-10,000Hz		2.8		dB

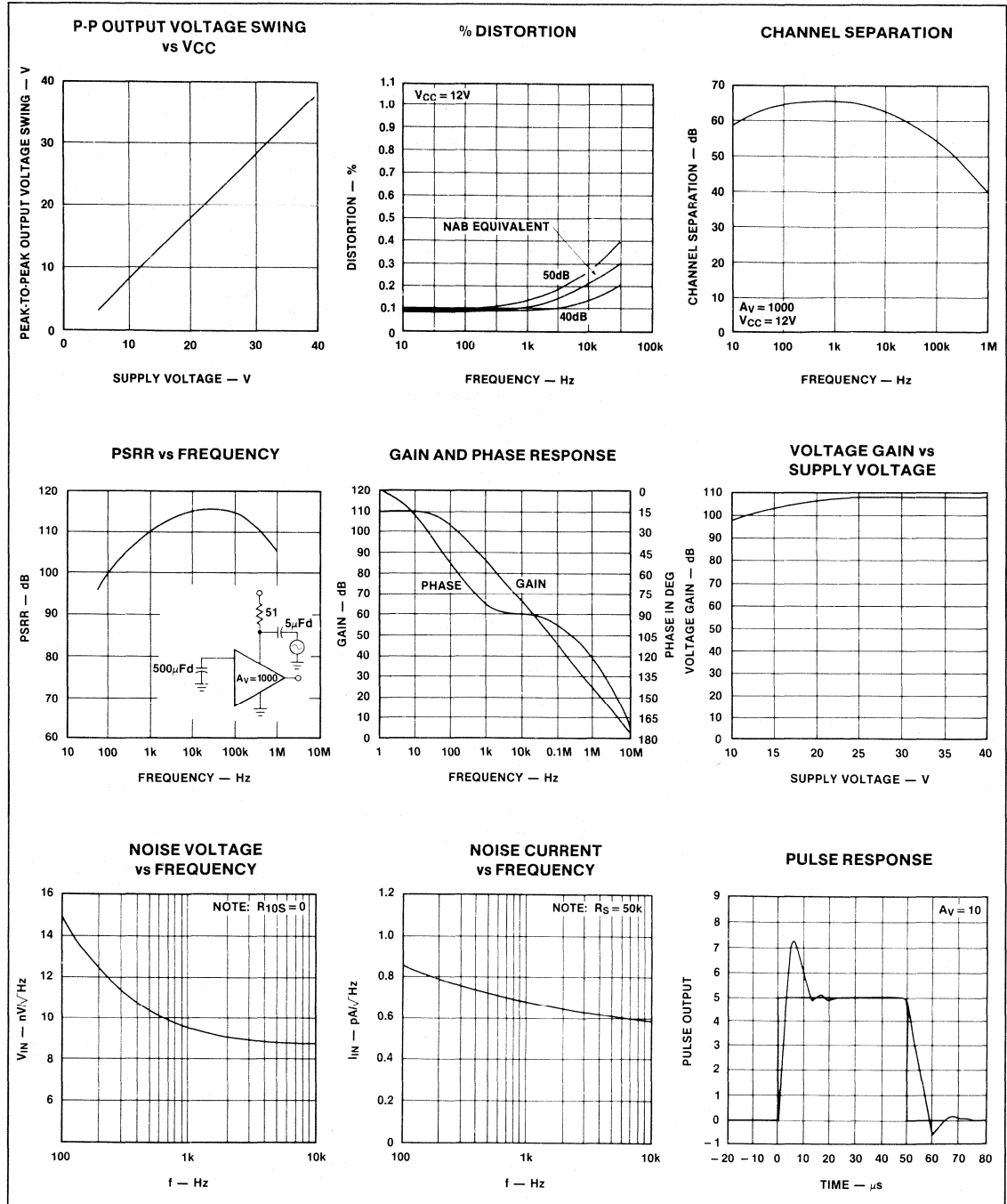
TYPICAL PERFORMANCE CHARACTERISTICS



DUAL LOW-NOISE PREAMP

LM387

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



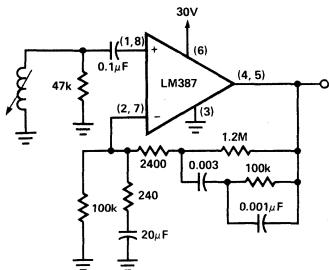
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DUAL LOW-NOISE PREAMP

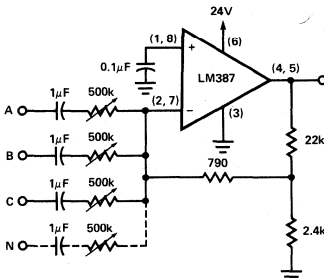
LM387

TYPICAL APPLICATIONS

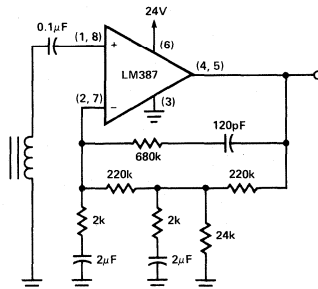
TYPICAL MAGNETIC PHONO PREAMPLIFIER



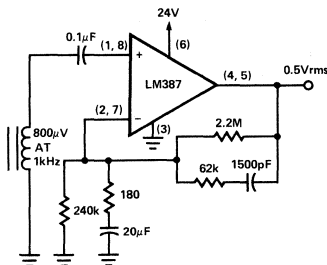
AUDIO MIXER



TWO-POLE FAST TURN-ON NAB TAPE PREAMPLIFIER



TYPICAL TAPE PLAYBACK AMPLIFIER



POWER DRIVER

NE/SE540

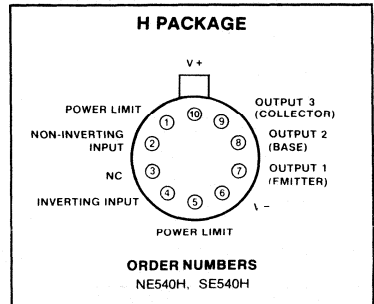
DESCRIPTION

The NE/SE540 is a monolithic, class AB power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use as an audio power amplifier.

FEATURES

- Internal current limiting
- Low standby current
- High output current capability
- Wide power bandwidth
- Low distortion

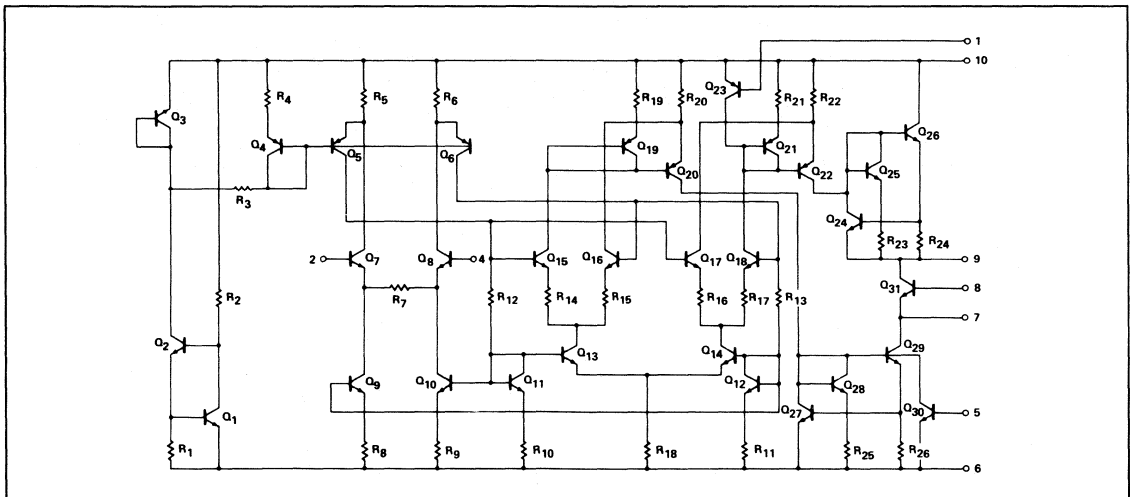
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE540	±27	V
NE540	±22	V
Operating temperature range		
SE540	-55 to +125	°C
NE540	0 to +70	°C
Storage temperature range	-65 to +150	°C
Output short circuit duration (Not exceeding maximum dissipation.)	Indefinite	

EQUIVALENT SCHEMATIC



POWER DRIVER

NE/SE540

DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ and $V_{CC} = \pm 20\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Operating supply voltage		± 5		± 25	± 5		± 20	V
Quiescent current			13	20		13	20	mA
Input offset voltage			5	7		7	10	mV
Input offset current			0.3	0.7		0.5	1	μA
Input bias current			1.5	3		2	5	μA
Input impedance			20			20		k Ω
Current gain		80	100		70	90		dB
Gain variation over temperature range	40dB gain		± 0.1			± 0.1		dB
Power supply rejection ratio		80	90		60	80		dB
Common mode rejection ratio	40dB gain		110			90		dB
Output drive current		± 120	± 150		± 80	± 100		mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ and $V_{CC} = \pm 20\text{V}$ unless otherwise specified.

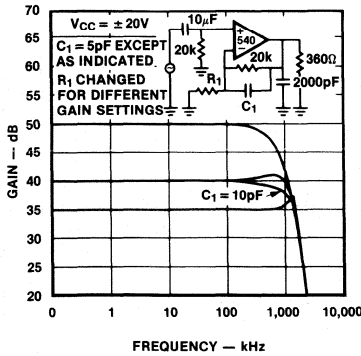
PARAMETER	TEST CONDITIONS	SE540			NE540			UNIT
		Min	Typ	Max	Min	Typ	Max	
Frequency response	40dB gain $\pm 1\text{dB}$		500			100		kHz
Distortion	40dB gain, Output 3dB below clipping $R_L = 600\Omega$ $R_L = 2k\Omega$		0.25	0.5		0.5	1.0	%
Equivalent input noise voltage	$R_S = 600\Omega$ 50Hz to 500kHz		0.06			0.06		μV
Slew rate	$V_{CC} = \pm 20\text{V}$ $V_{OUT} = \pm 15\text{V}$		10			10		$\mu\text{V}/\mu\text{s}$
			200			200		$\text{V}/\mu\text{s}$

POWER DRIVER

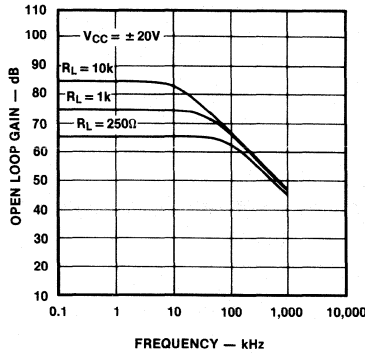
NE/SE540

TYPICAL PERFORMANCE CHARACTERISTICS

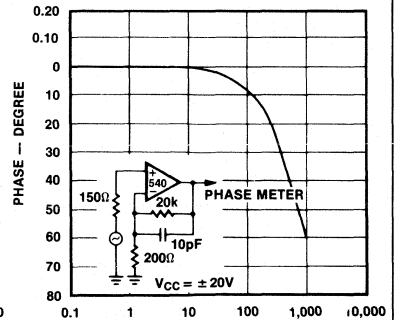
CLOSED LOOP FREQUENCY RESPONSE



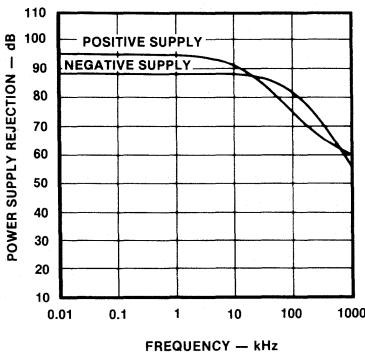
OPEN LOOP GAIN AND FREQUENCY RESPONSE



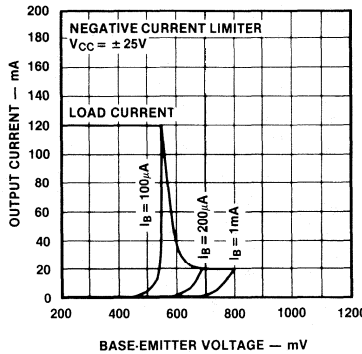
PHASE RESPONSE vs FREQUENCY



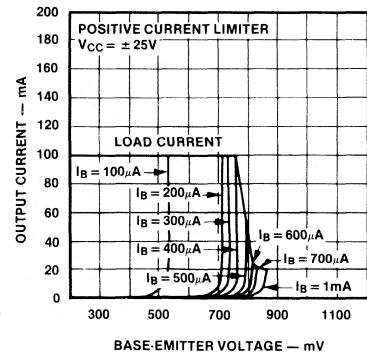
POWER SUPPLY REJECTION vs FREQUENCY



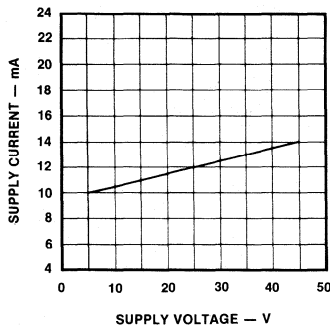
OUTPUT CURRENT vs IB/VBE OF CURRENT LIMITER



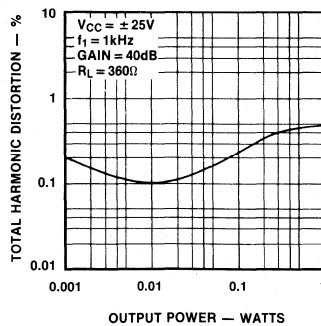
OUTPUT CURRENT vs IB/VBE OF CURRENT LIMITER



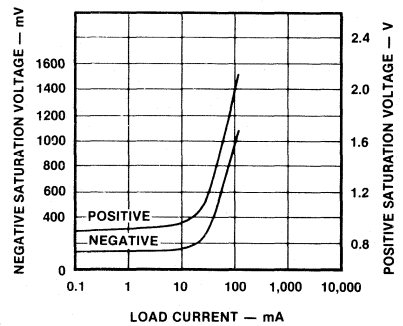
QUIESCENT CURRENT vs SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION vs OUTPUT



OUTPUT SATURATION VOLTAGE vs LOAD

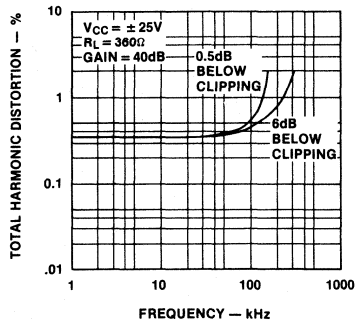


POWER DRIVER

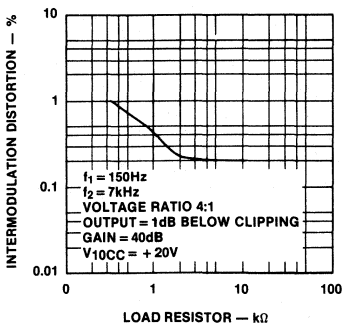
NE/SE540

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

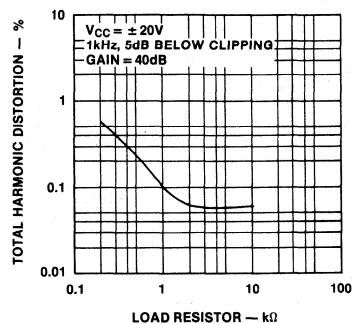
TOTAL HARMONIC DISTORTION vs FREQUENCY



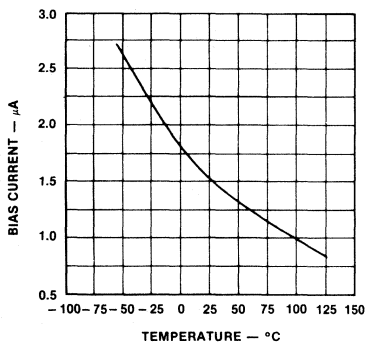
INTERMODULATION DISTORTION vs LOAD



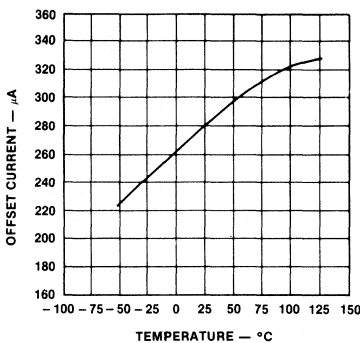
TOTAL HARMONIC DISTORTION vs LOAD



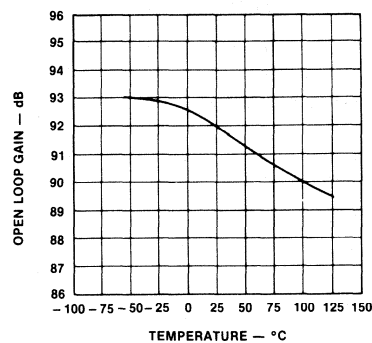
BIAS CURRENT vs TEMPERATURE



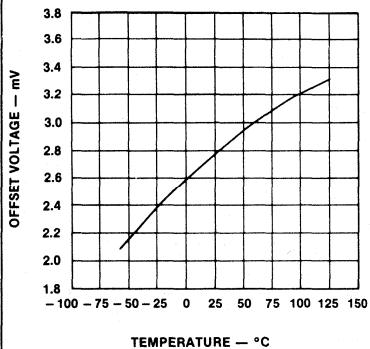
OFFSET CURRENT vs TEMPERATURE



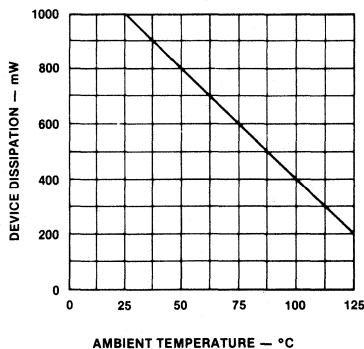
OPEN LOOP GAIN vs TEMPERATURE



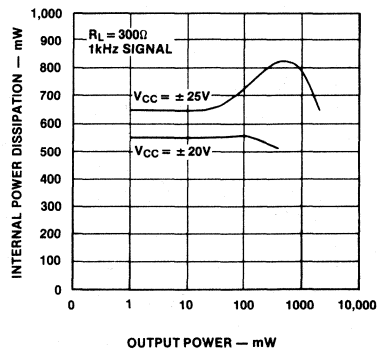
OFFSET VOLTAGE vs TEMPERATURE



MAXIMUM DISSIPATION vs AMBIENT TEMPERATURE



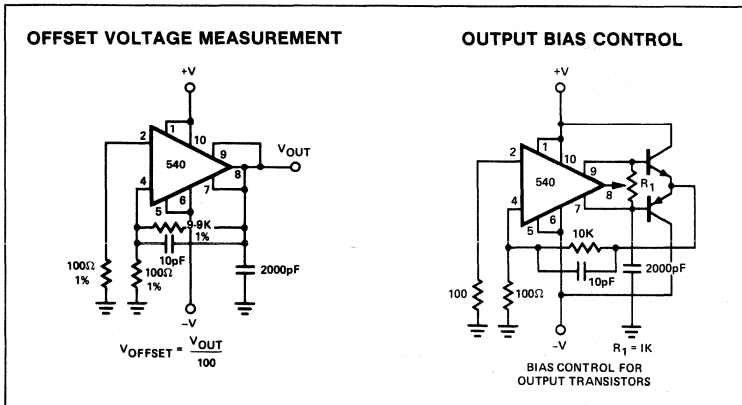
INTERNAL POWER DISSIPATION vs LOAD POWER



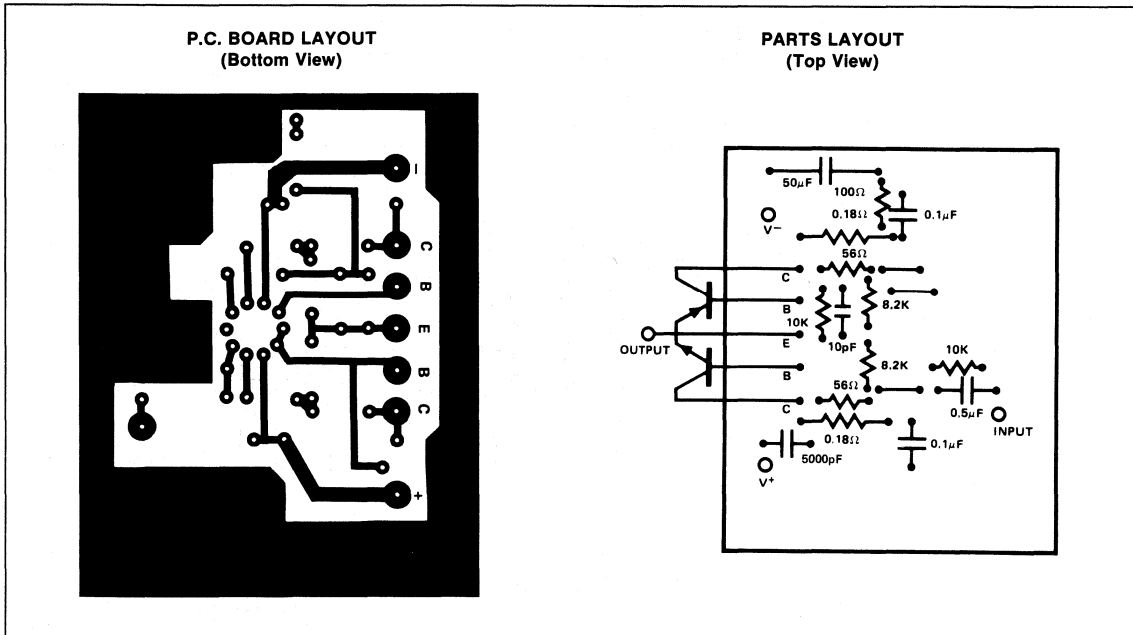
POWER DRIVER

NE/SE540

TEST CIRCUITS



35 WATT AMPLIFIER



DUAL LOW-NOISE PREAMP

NE542

DESCRIPTION

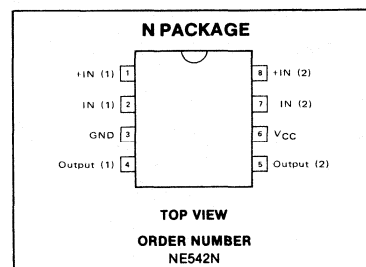
The NE542 is a dual preamplifier for the amplification of low level signals in applications requiring optimum noise performance. Each of the two amplifiers is completely independent, with individual internal power supply decoupler-regulator, providing 110dB supply rejection and 70dB channel separation. Other outstanding features include high gain (104dB), large output voltage swing (V_{CC} -2Vp-p), and internal compensation to 10dB. The NE542 operates from a single supply across the wide range of 9 to 24V.

The NE542 is ideal for use in stereo phono, tape, or microphone preamps and other applications requiring low noise amplification of small signals.

FEATURES

- Low noise— $.7\mu V$ total input noise
- High gain—104dB open loop
- Single supply operation
- Wide supply range 9 to 24V
- Power supply rejection 110dB
- Large output voltage swing (V_{CC} -2V p-p)
- Wide bandwidth 15MHz unity gain
- Power bandwidth 100kHz (15V p-p)
- Internally compensated (stable at 10dB)
- Short circuit protected
- High slew rate 5V/ μs

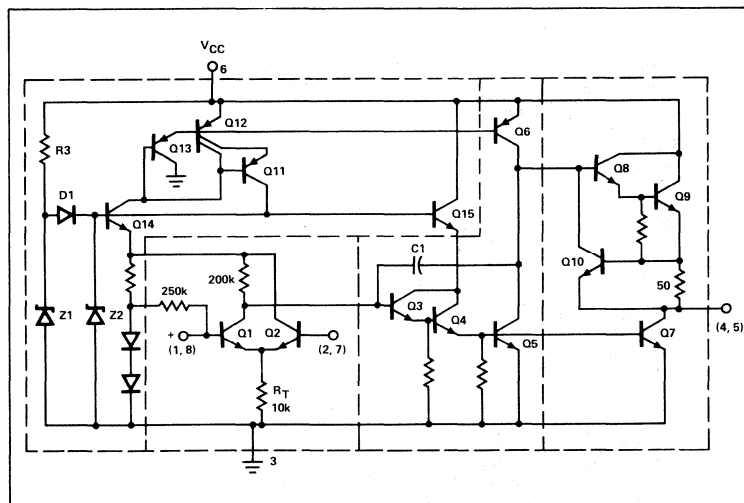
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	+24	V
Power dissipation	500	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	+300	°C

EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ C$, $V_{CC} = 14V$
unless otherwise specified.

PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Supply voltage		9		24	V
Supply current	$V_{CC} = 9$ to 18V, $R_L = \infty$		9	15	mA
Input resistance					
Positive input			100		k Ω
Negative input			200		k Ω
Output resistance	Open loop		150		Ω

DUAL LOW-NOISE PREAMP

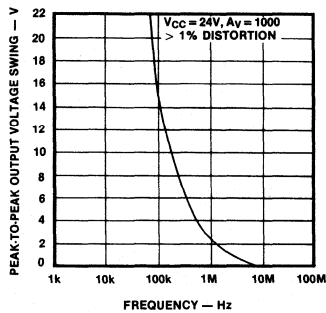
NE542

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 14\text{V}$ unless otherwise specified.

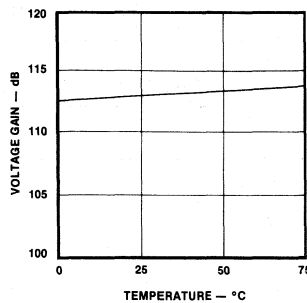
PARAMETER	TEST CONDITIONS	NE542			UNIT
		Min	Typ	Max	
Voltage gain	Open loop		160,000		V/V
Input current Negative input			.5		μA
Output current	Source Sink (linear operation)	8 2	14 3		mA mA
Output voltage swing		$V_{CC} - 2.5$	$V_{CC} - 2$		V
Small signal bandwidth			15		MHz
Slew rate			5		V/ μs
Power bandwidth	15V p-p		100		kHz
Maximum input voltage	Linear operation			300	mVrms
Supply rejection ratio	$f = 60, 120\text{Hz}$		100		dB
Channel separation	$f = 1\text{kHz}$		110		dB
Total harmonic distortion	75dB gain, $f = 1\text{kHz}$.1		%
Total equivalent input Noise	$R_S = 600\Omega$, 100 - 10,000Hz		.7	1.2	μVrms
Noise figure	$R_S = 50\text{k}\Omega$, 10 - 10,000Hz		1.2		dB
	$R_S = 20\text{k}\Omega$, 10 - 10,000Hz		1.2		dB
	$R_S = 10\text{k}\Omega$, 10 - 10,000Hz		1.5		dB
	$R_S = 5\text{k}\Omega$, 10 - 10,000Hz		2.4		dB

TYPICAL PERFORMANCE CHARACTERISTICS

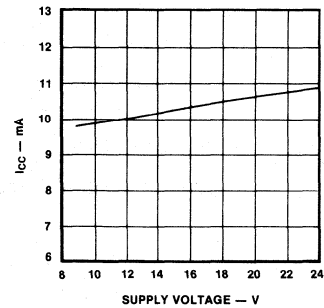
LARGE SIGNAL FREQUENCY RESPONSE



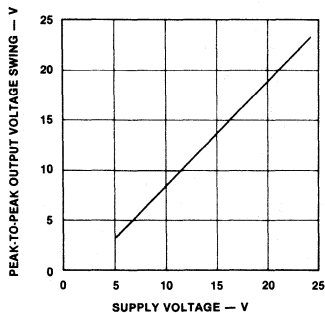
GAIN vs TEMPERATURE



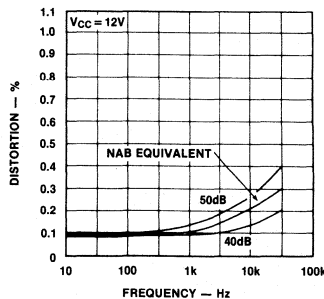
V_{CC} vs I_{CC}



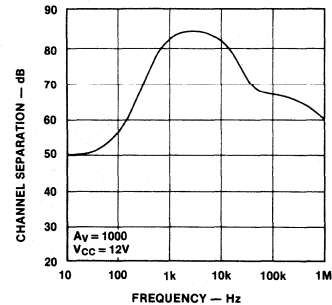
P-P OUTPUT VOLTAGE SWING vs V_{CC}



% DISTORTION



CHANNEL SEPARATION

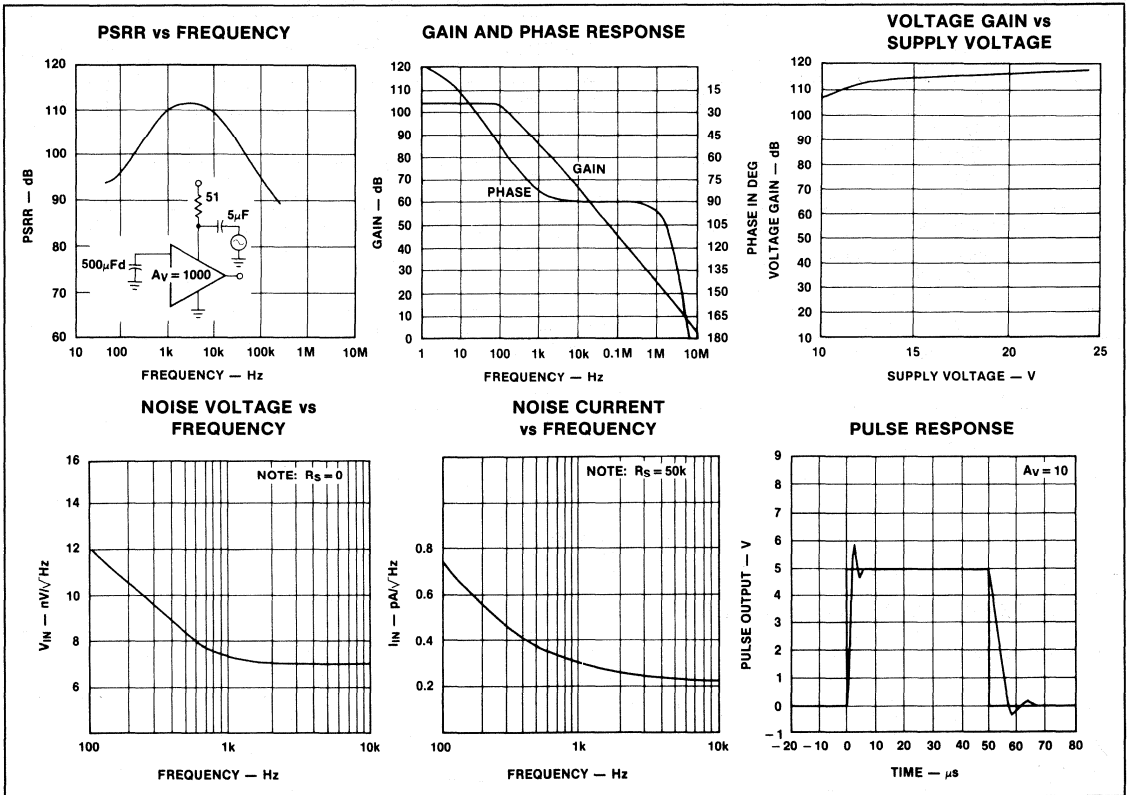


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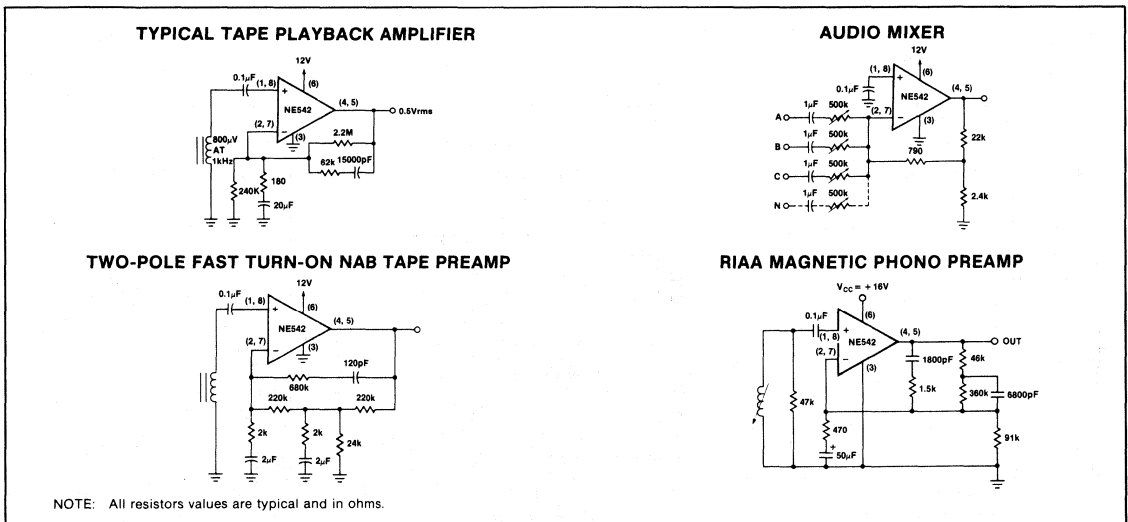
DUAL LOW-NOISE PREAMP

NE542

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



TYPICAL APPLICATIONS



COMPANDOR

NE570/571/SA571

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expander. Each channel has a full wave rectifier to detect the average value of the signal; a linearized, temperature compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

FEATURES

- Complete compressor and expander in 1 IC
- Temperature compensated
- Greater than 110dB dynamic range
- Operates under 6Vdc
- System levels adjustable with external components
- Distortion may be trimmed out

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF} . The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than $.1\mu A$.

$$G \propto \frac{|V_{IN} - V_{REF}|_{ave}}{R_1}$$

or

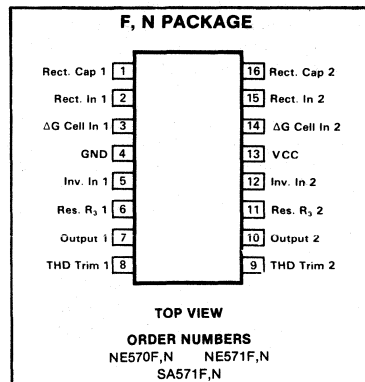
$$G \propto \frac{|V_{IN}|_{ave}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expander or com-

APPLICATIONS

- Telephone trunk compandor—570
- Telephone subscriber compandor—571
- High level limiter
- Low level expander—noise gate
- Dynamic noise reduction systems
- Voltage controlled amplifier
- Dynamic filters

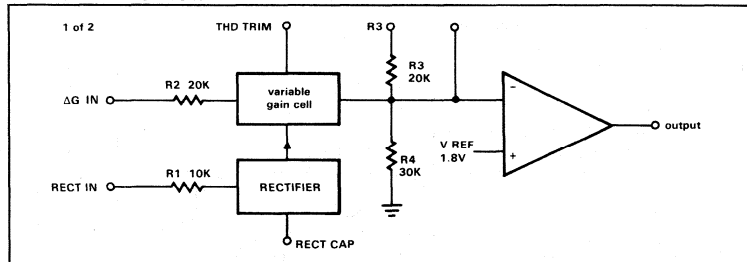
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply	24	Vdc
570	18	
571		
T_A Operating temperature range	0 to 70	$^{\circ}C$
NE	-40 to +85	$^{\circ}C$
SA	400	mW
PD Power dissipation		

BLOCK DIAGRAM



pressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final}) e^{-t/\tau} + G_{final}; \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF} . The following equation applies for capacitively coupled inputs. The output current, I_{OUT} , is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF} , and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3 , is brought out from the summing node and allows compressor or expander gain to be determined only by internal components.

COMPANDOR

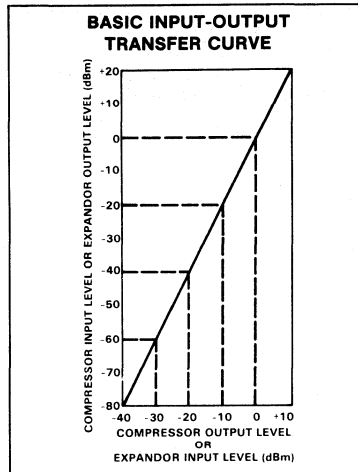
NE570/571/SA571

The output stage is capable of $\pm 20\text{mA}$ output current. This allows a $+13\text{dBm}$ (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in $+13\text{dBm}$ with a 600Ω output impedance.

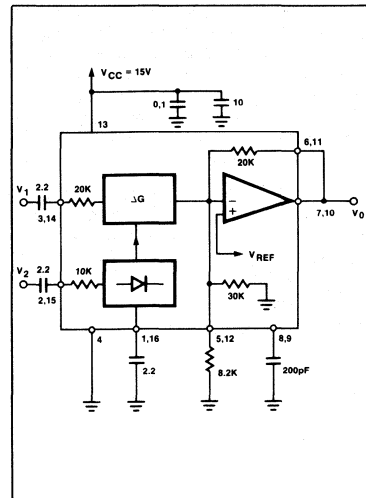
A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempo of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expander circuits.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 15\text{V}^1$

PARAMETER	TEST CONDITIONS	NE570			NE/SA571 ⁶			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Supply voltage	No signal	6		24	6		18	V
I_{CC} Supply current			3.2	4.0		3.2	4.8	mA
Output current capability			± 20					mA
Output slew rate	Untrimmed		$\pm .5$			$.5$		V/us
Gain cell distortion ²		Trimmed		$.3$	1.0		$.1$	2.0
Resistor tolerance			± 5	± 15				%
Internal reference voltage	Untrimmed	1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift ³		Trimmed		± 20	± 50		$+30$	± 100
Expander output noise	No signal, 20Hz-20kHz		20					μV
Unity gain level		-1	0	+1	-1.5	0	+1.5	dBRNC
Gain change ^{2,4}	$-40^\circ\text{C} < T < 70^\circ\text{C}$		± 1			± 1		dB
Reference drift ⁴	$0^\circ\text{C} < T < 70^\circ\text{C}$		± 1	± 2		± 1	± 4	mV
	$-40^\circ\text{C} < T < 70^\circ\text{C}$		$+2, -25$	$-10, -40$		$+2, -25$	$+20, -50$	
	$0^\circ\text{C} < T < 70^\circ\text{C}$		± 5	± 10		± 5	± 20	
Resistor drift ⁴	$-40^\circ\text{C} < T < 70^\circ\text{C}$		$+8, -0$					%
	$0^\circ\text{C} < T < 70^\circ\text{C}$		$+1, -0$					
Tracking error ⁵ , input $V_1 = 0\text{dBm}$	Rectifier input, $V_2 = +6\text{dBm}$		± 2					dB
	-10dBm		$+2$	$-2, +4$		$+2$	$-2, +5$	
	-20dBm		$+2$	$-3, +6$		$+2$	$-4, +7$	
	-30dBm		$+2$	$-5, +1$		$+2$	$-1, +1.5$	
	-40dBm		$+2, -4$			$+2, -4$		

NOTES

1. Except where indicated, the 571 specifications are identical to the 570
2. Measured at 0dBm , 1kHz
3. Expander ac input change from no signal to 0dBm
4. Relative to value at $T_A = 25^\circ\text{C}$
5. Relative to 0dBm
6. Electrical characteristics for the SA571 only are specified over -40 to $+85^\circ\text{C}$ temperature range.

PROGRAMMABLE ANALOG COMPANDOR

NE572

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

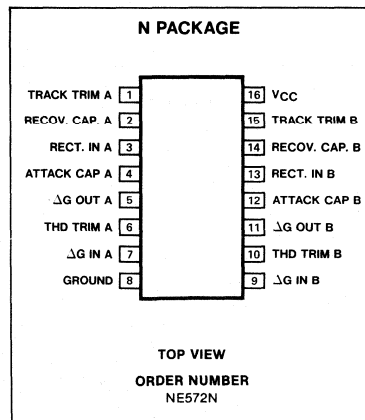
FEATURES

- Independent control of attack and recovery time.
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external Op Amp
- Wide dynamic range—greater than 110dB
- Temperature compensated gain control
- Low distortion gain cell
- Low noise— $6\mu V$ typical
- Wide supply voltage range—6V–22V
- System level adjustable with external components.

APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expander
- Automatic level control
- High level limiter
- Low level noise gate
- State variable filter

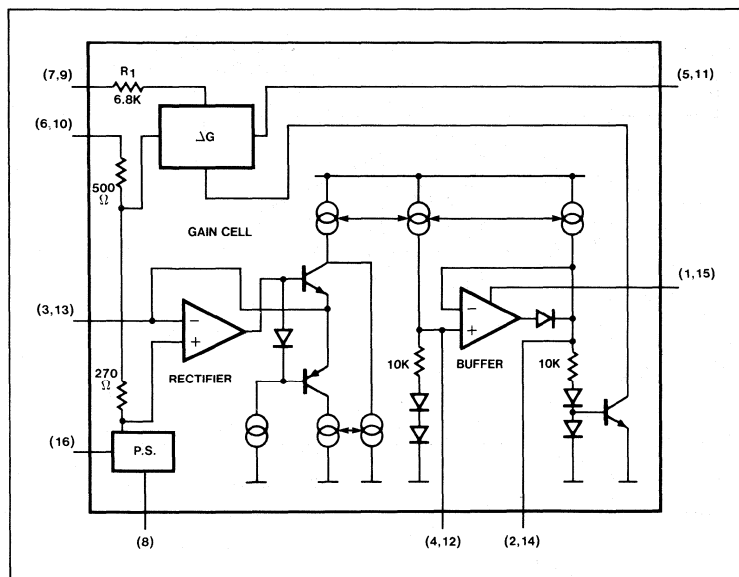
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC}	Supply voltage	22	VDC
T _A	Operating temperature range	0 to 70	°C
P _D	Power dissipation	500	mW

BLOCK DIAGRAM



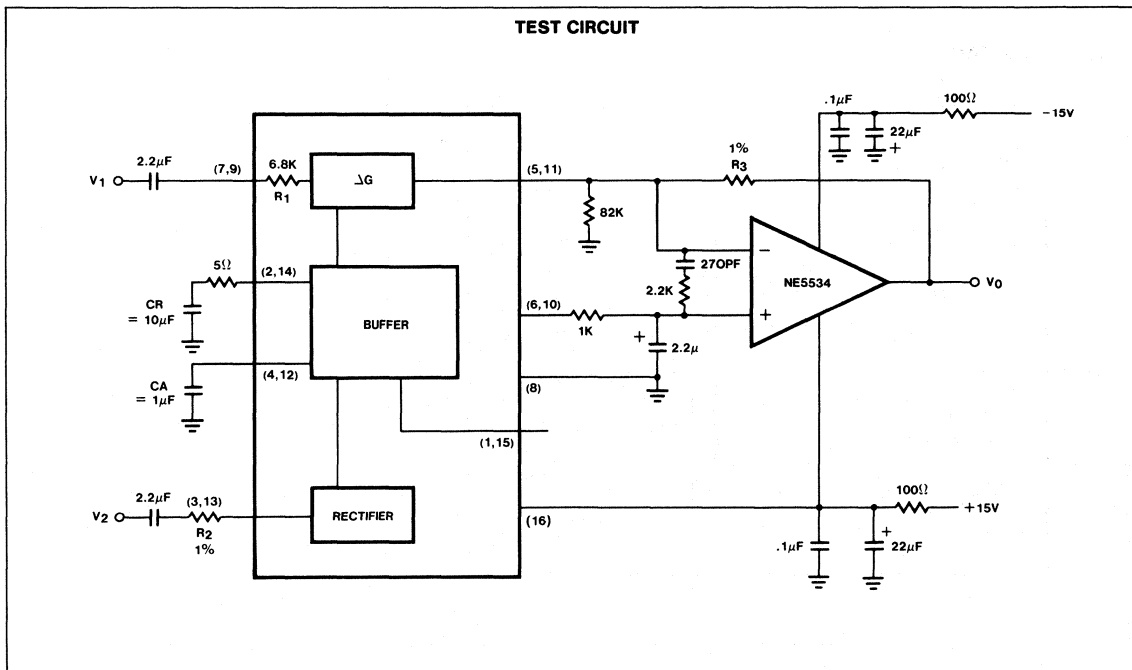
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PROGRAMMABLE ANALOG COMPANDOR

NE572

ELECTRICAL CHARACTERISTICS Standard Test Conditions (unless otherwise noted) $V_{CC} = 15V$ $T_A = 25^\circ C$ Expander mode (see test circuit) Input signals at unity gain level = 100mV RMS at 1KHz, $V_1 = V_2$, $R_2 = 3.3K$, $R_3 = 17.3K$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		6		22	V_{DC}
I_{CC}	Supply current	No Signal			6	mA
	Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD	(untrimmed)	1kHz $C_A = 1.0\mu F$.2	1.0	%
THD	(trimmed)	1kHz $C_R = 10\mu F$.05		%
THD	(trimmed)	100Hz		.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20-20kHz)		6	25	μV
	DC level shift (untrimmed)	Input change from no signal to 100mV RMS		± 20	± 50	MV
	Unity gain level		-1	0	+1	dB
	Large signal distortion	$V_1 = V_2 = 400mV$		0.7	3.0	%
	Tracking error measured relative to value at unity gain output	Rectifier input $V_2 = +6dB$ $-30dB$		$\pm .2$ $\pm .5$	-1.5 $+ .8$	dB
	Channel crosstalk	200mV RMS into channel A, measured output on channel B	60			dB
	Power supply rejection ratio	120Hz		70		dB



DOLBY NOISE REDUCTION CIRCUIT

NE645/46

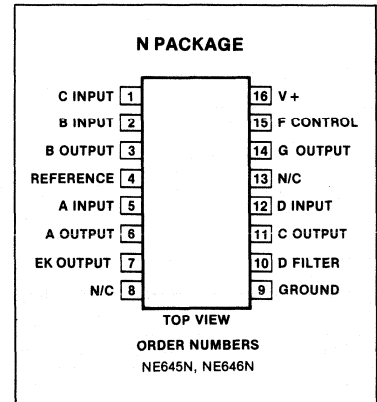
DESCRIPTION

The NE645/646 is a monolithic audio noise reduction circuit designed as a direct replacement device for the NE645B/NE646B in Dolby* B- and C-Type noise reduction systems. The NE645/646 is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape, and to improve the noise level in FM broadcast reception. This circuit is available only to licensees of Dolby Laboratories Licensing Corporation, San Francisco, California.

FEATURES

- Accurate record mode frequency response
- Excellent frequency response tracking with temperature and $V_{CC} \pm 0.4$ dB typical
- Excellent back-to-back dynamic response — D.C. shift less than 20 mV typical
- Improved stability of all op amps
- High reliability packaging

PIN CONFIGURATION



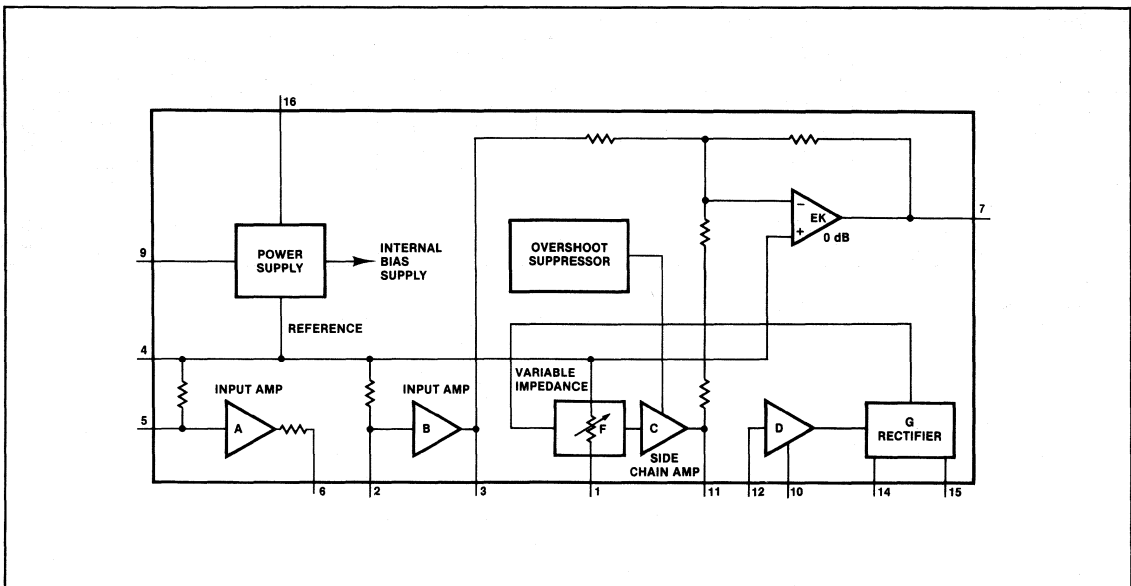
NOTE

*T.M. Dolby Laboratories Licensing Corporation.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	24	V
Temperature range		
Operating	0 to +70	°C
Storage	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

BLOCK DIAGRAM



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DOLBY NOISE REDUCTION CIRCUIT

NE645/46

ELECTRICAL CHARACTERISTICS

 $V_{CC} = 12$ volts, $f = 20$ Hz to 20 kHz.All levels referenced to 580 mVrms (0 dB) at Pin 3, $T_A = +25^\circ\text{C}$

Unless otherwise noted.

PARAMETER	TEST CONDITIONS	NE645			NE646			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage Range		8		20	8		20	V
Supply Current, I_{CC}	$V_{CC} = 12\text{V}$		16	24		16	24	mA
Voltage gain (Pins 5-3)	$f = 1$ kHz (Pins 6 and 2 connected)	24.5	26	27.5	24.5	26	27.5	dB
Voltage gain (Pins 3-7)	$f = 1$ kHz, 0 dB at pin 3, noise reduction out	-0.5	0	+0.5	-0.5	0	+0.5	dB
Distortion THD, 2nd and 3rd harmonic	$f = 20$ Hz - 10 kHz, 0dB		0.05	0.1		0.05	0.2	%
	$f = 20$ Hz - 10 kHz, +10 dB		0.15	0.3		0.2	0.5	%
Signal handling ¹ ($V_{CC} = 12\text{V}$)	1% dist at 1 kHz	+12	+15		+12	+15		dB
Signal-to-noise ratio ²	Record mode	67	72		64	72		dB
	Playback mode	77	82		74	82		dB
Record mode Frequency response (at pin 7) referenced to encode monitor point (pin 3)	$f = 1.4\text{kHz}$ 0dB -20dB -30dB	-1	0	+1	-1.5	0	+1.5	dB
		-16.6	-15.6	-14.6	-17.1	-15.6	-14.1	dB
		-23.5	-22.5	-21.5	-24.0	-22.5	-21.0	dB
	$f = 5\text{kHz}$ 0dB -20dB -30dB -40dB	-0.7	+0.3	+1.3	-1.2	+0.3	+1.8	dB
		-17.8	-16.8	-15.8	-18.3	-16.8	-15.3	dB
		-22.8	-21.8	-20.8	-23.3	-21.8	-20.3	dB
		-30.2	-29.7	-28.7	-30.2	-29.7	-28.2	dB
	$f = 20\text{kHz}$ 0dB -20dB -30dB	-0.3	+0.7	+1.7	-0.8	+0.7	+2.2	dB
		-18.3	-17.3	-16.3	-18.8	-17.3	-15.8	dB
-24.5		-23.5	-22.5	-25.0	-23.5	-22.0	dB	
Back-to-back frequency response	Using typical record mode frequency response test points	-1	0	+1	-1.5	0	+1.5	dB
Input resistance	Pin 5	35	50	65	35	50	65	k Ω
	Pin 2	3.1	4.2	5.3	3.1	4.2	5.3	k Ω
Output resistance	Pin 6	1.9	2.4	3.1	1.9	2.4	3.1	k Ω
	Pin 3		80	120		80	120	Ω
	Pin 7		80	120		80	120	Ω
Back-to-back frequency response shift	Versus temperature Versus supply voltage	0°-70°C						
		8-20V		± 0.4		± 0.4		dB
			± 0.4			± 0.4		dB

NOTES

1. See maximum signal handling versus supply voltage characteristics.

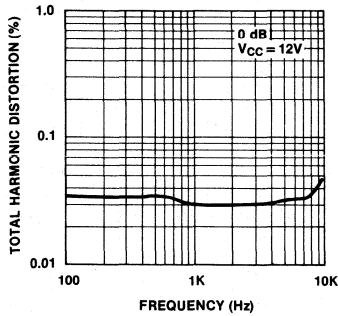
2. All noise levels are measured CCIR/ARM weighted using a 10K source with respect to Dolby level. See Dolby Laboratories Bulletin 19.

DOLBY NOISE REDUCTION CIRCUIT

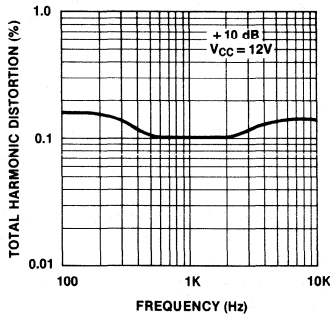
NE645/46

PERFORMANCE CHARACTERISTICS

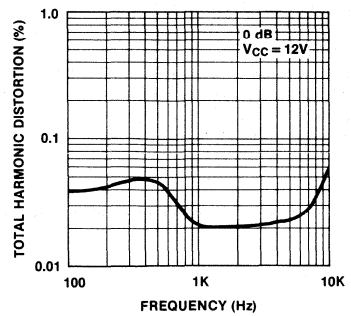
THD vs FREQUENCY RECORD MODE



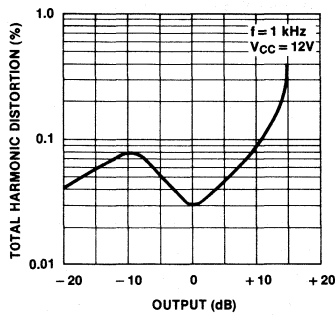
THD vs FREQUENCY RECORD MODE



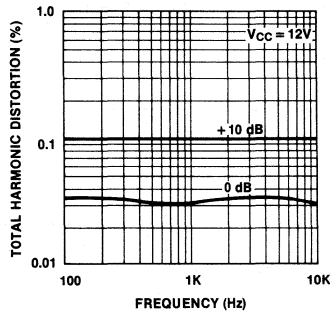
THD vs FREQUENCY PLAY MODE



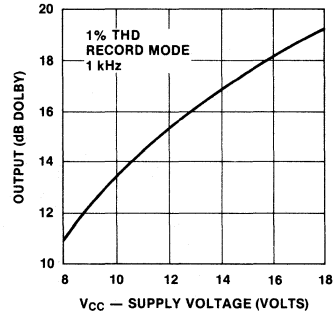
THD vs OUTPUT RECORD MODE



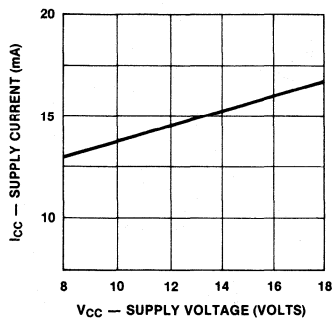
THD vs FREQUENCY NOISE REDUCTION (NR) OFF



MAXIMUM SIGNAL HANDLING vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE



DOLBY NOISE REDUCTION CIRCUIT

NE645/46

APPLICATION INFORMATION

The NE645/646 is a direct replacement for the NE645B/646B. The NE645/646 incorporates improved design techniques to insure excellent performance required in Dolby B and C Type Audio Noise Reduction Systems. Critical component values are unchanged except for C309 on Pin 1 which is now an optional component in specific applications defined by Dolby Laboratories. All circuit parameters are guaranteed at 12V V_{CC}.

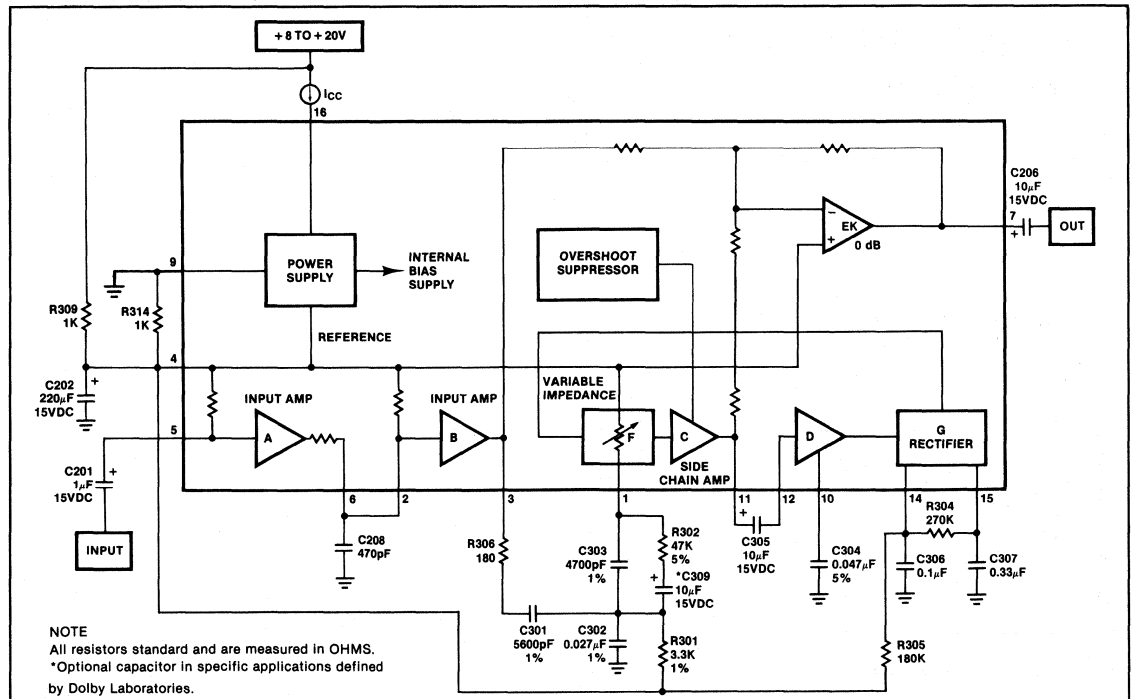
DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE

The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

TEST CIRCUIT NE645/646



NOTE
 All resistors standard and are measured in OHMS.
 *Optional capacitor in specific applications defined by Dolby Laboratories.

LOW VOLTAGE DOLBY NOISE REDUCTION CIRCUIT

NE648/49

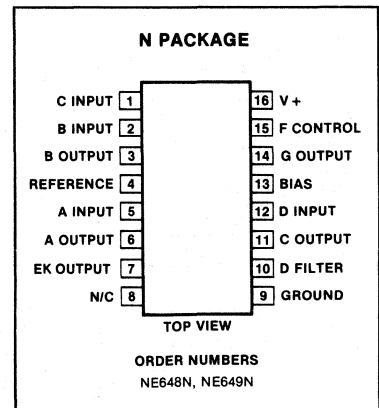
DESCRIPTION

The NE648/649 is an audio noise reduction circuit designed for use in low voltage entertainment systems. The circuit is used to reduce the level of background noise introduced during the recording and playback of audio signals on magnetic tape and improve the noise level in FM broadcast reception. The circuit is intended for use in automotive and portable cassette Dolby* B and C Type noise reduction systems. This circuit is available only to licensees of Dolby Laboratories Licensing Corp., San Francisco.

NOTE

*T.M. Dolby Laboratories Licensing Corporation

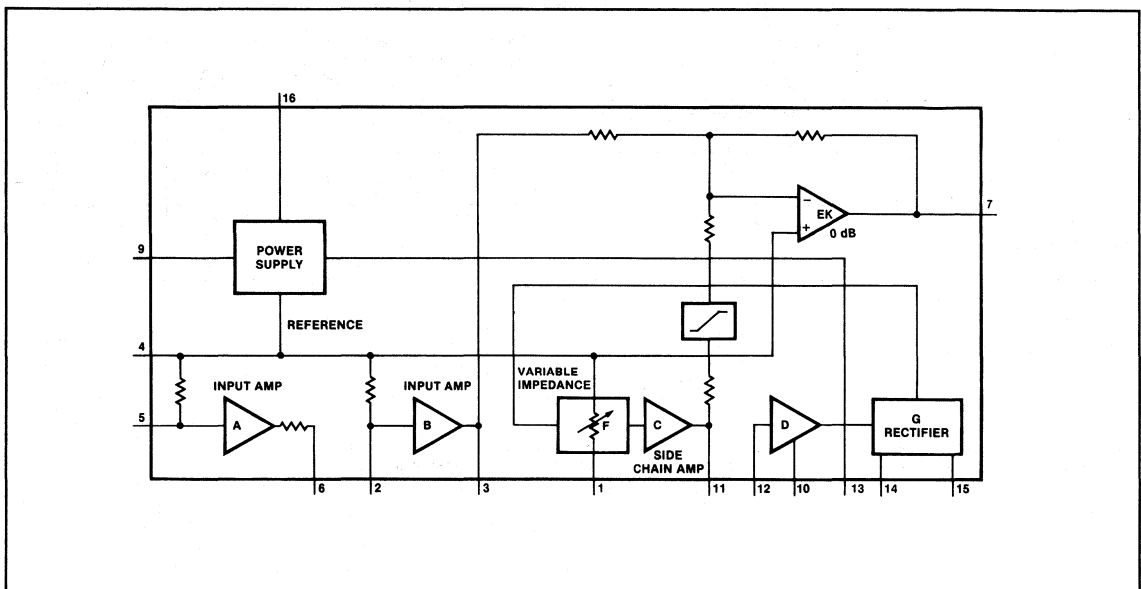
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	16	V
Temperature range		
Operating	- 40 to + 85	°C
Storage	- 65 to + 150	°C
Lead temperature (soldering 60sec)	+ 300	°C

BLOCK DIAGRAM



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LOW VOLTAGE DOLBY NOISE REDUCTION CIRCUIT

NE648/49

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 9V$, $f = 20\text{Hz}$ to 20kHz .

All levels referenced to 580mVrms (0dB) at pin 3, $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	TEST CONDITIONS	NE648			NE649			UNIT
		Min	Typ	Max	Min	Typ	Max	
Supply voltage range ³		6	9	14	6	9	14	V
Minimum voltage supply for 8dB headroom 10dB headroom	$f = 1.4\text{kHz}$ THD < 1%	6.5			6.5			V
		7.5			7.5			V
Supply Current, I_{CC}			11	18		11	18	mA
Supply Current, I_{CC}				20			20	mA
Voltage gain (pins 5-3)	$f = 1\text{kHz}$ (pins 6 and 2 connected)	24.5	26	27.5	24.5	26	27.5	dB
Voltage gain (pins 3-7)	$f = 1\text{kHz}$, 0dB at pin 3, noise reduction out	-0.5	0	+0.5	-0.5	0	+0.5	dB
Distortion	$f = 20\text{kHz}$ to 10kHz , 0dB $f = 20\text{Hz}$ to 10kHz , +10dB		0.05	0.1		0.05	0.2	%
			0.2	0.3		0.2	0.5	%
Signal Handling (See Performance Characteristics)								
Signal-to-noise ratio ²	Record (pins 6 and 2 connected)	67	72		64	72		dB
	Playback (pins 6 and 2 connected)	77	82		74	82		dB
Record mode frequency response (at pin 7) referenced to encode monitor point (pin 3)	$f = 1.4\text{kHz}$ 0dB -20dB -30dB	-1	0	+1	-1.5	0	+1.5	dB
		-16.6	-15.6	-14.6	-17.1	-15.6	-14.1	dB
		-23.5	-22.5	-21.5	-24.0	-22.5	-21.0	dB
	$f = 5\text{kHz}$ 0dB -20dB -30dB -40dB	-0.7	+0.3	+1.3	-1.2	+0.3	+1.8	dB
		-17.8	-16.8	-15.8	-18.3	-16.8	-15.3	dB
		-22.8	-21.8	-20.8	-23.3	-21.8	-20.3	dB
		-30.2	-29.7	-28.7	-30.2	-29.7	-28.2	dB
	$f = 20\text{kHz}$ 0dB -20dB -30dB	-0.3	+0.7	+1.7	-0.8	+0.7	+2.2	dB
		-18.3	-17.3	-16.3	-18.8	-17.3	-15.8	dB
-24.5		-23.5	-22.5	-25.0	-23.5	-22.0	dB	
Back-to-back frequency response	Using typical record mode response		± 1.0			± 1.5		dB
Input resistance	Pin 5	35	50	65	35	50	65	k Ω
	Pin 2	3.1	4.2	5.3	3.1	4.2	5.3	k Ω
Output resistance	Pin 6	1.9	2.4	3.1	1.9	2.4	3.1	k Ω
	Pin 3		80	120		80	120	Ω
	Pin 7		80	120		80	120	Ω
Record mode frequency response shift								
Versus temperature	0 to 70°C -40 to 85°C		± 0.3 ± 0.5					dB
Versus V_{CC}	6 to 14V		0.2					dB/V

NOTES

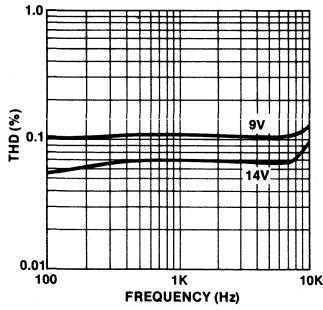
1. With electronic switching.
2. All noise levels are measured CCIR/ARM weighted using a 10K source with respect to Dolby level. See Dolby Laboratories Bulletin 19.
3. The circuit will function as low as $V_{CC} = 4.5V$ (i.e. output signal present). See graphs of I_{CC} and signal handling vs V_{CC} .

LOW VOLTAGE DOLBY NOISE REDUCTION CIRCUIT

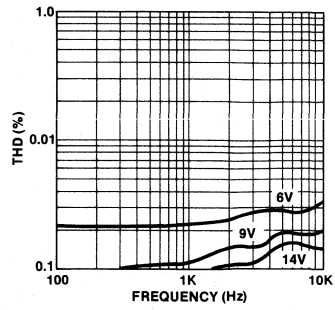
NE648/49

PERFORMANCE CHARACTERISTICS

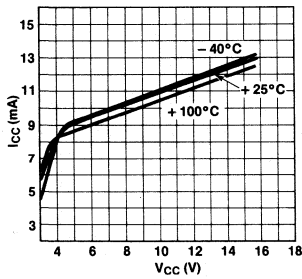
(+10dB) THD vs FREQUENCY



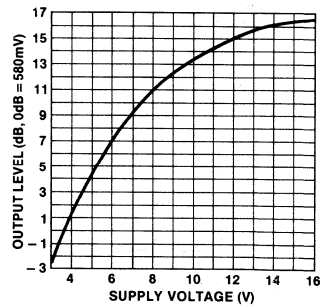
(0dB) THD vs FREQUENCY



CURRENT vs SUPPLY VOLTAGE



MAXIMUM SIGNAL HANDLING vs SUPPLY VOLTAGE FOR 1% THD (RECORD)



LOW VOLTAGE DOLBY NOISE REDUCTION CIRCUIT

NE648/49

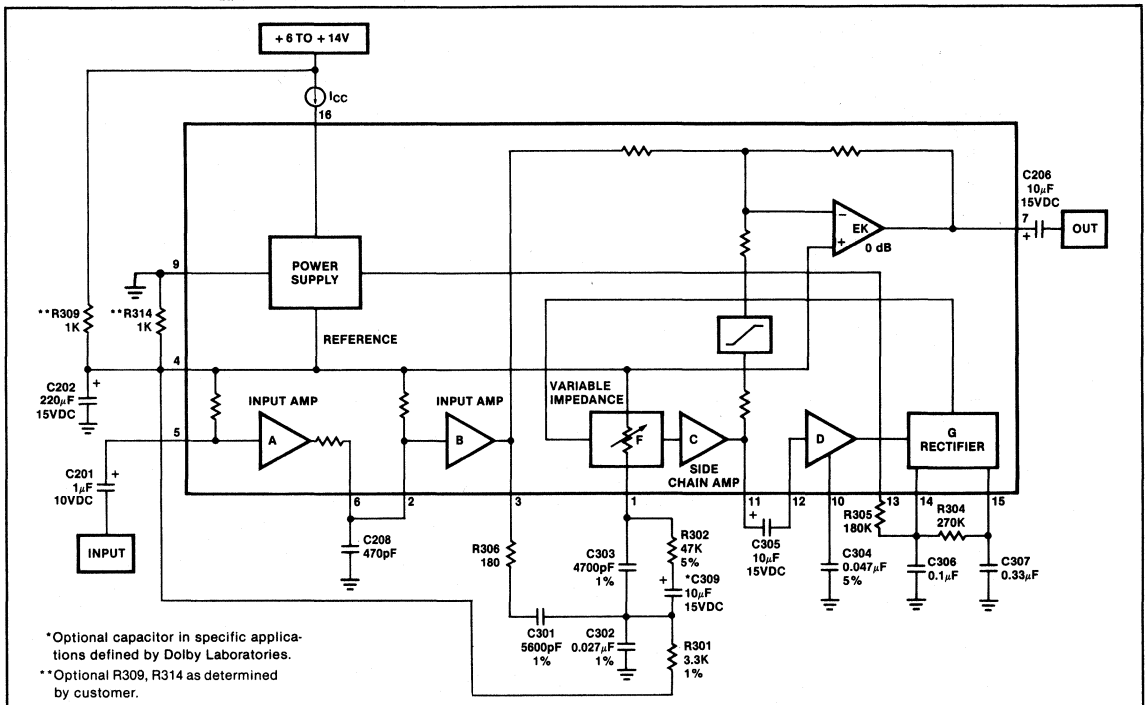
DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE

The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

TEST CIRCUIT NE648/49



DOLBY B/C TYPE NOISE REDUCTION CIRCUIT

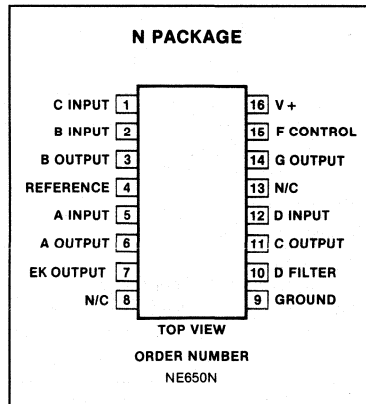
NE650

DESCRIPTION

The NE650 is a monolithic audio noise reduction circuit designed for use in Dolby* B/C Type noise reduction systems. The NE650 is used to reduce the level of background noise introduced during recording and playback of audio signals on magnetic tape. The NE650 features excellent dynamic characteristics over a wide range of operating conditions and is pin compatible with NE645/646. This circuit is available only to licensees of Dolby Laboratories Licensing Corp., San Francisco.

NOTE
*T.M. Dolby Laboratories Licensing Corporation.

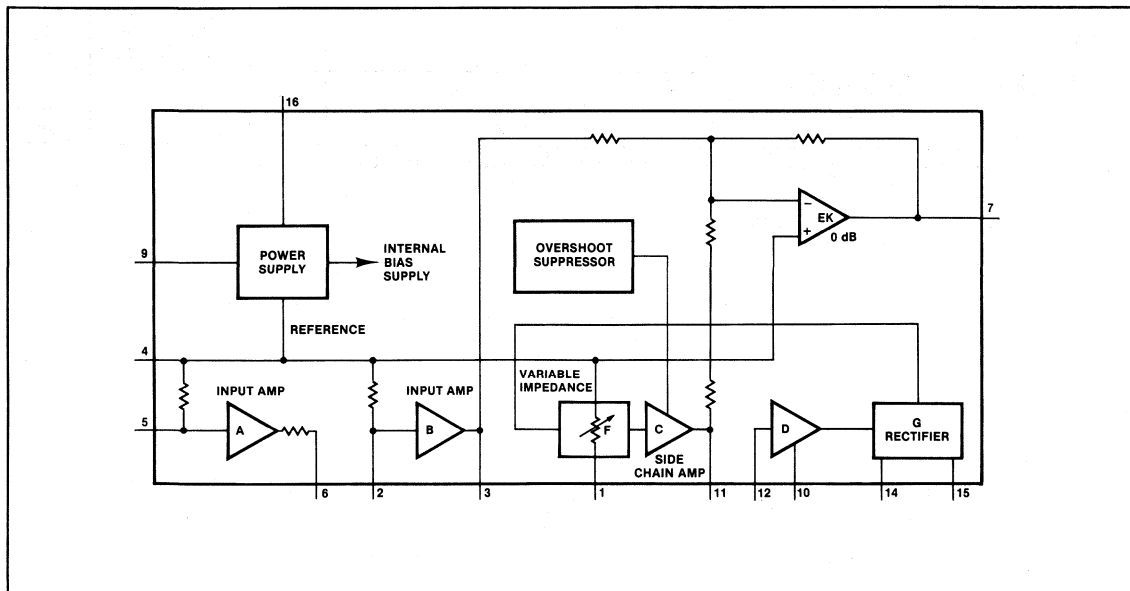
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage	24	V
Temperature range		
Operating	0 to +70	°C
Storage	-65 to +150	°C
Lead temperature (soldering 60sec)	+300	°C

BLOCK DIAGRAM



15

DOLBY B/C TYPE NOISE REDUCTION CIRCUIT**NE650****DC ELECTRICAL CHARACTERISTICS** $V_{CC} = 12V$, $f = 20\text{Hz}$ to 20kHz .All levels referenced to 580mVrms (0dB) at pin 3, $T_A = +25^\circ\text{C}$ unless otherwise noted.

PARAMETER	TEST CONDITIONS	NE650			UNIT
		Min	Typ	Max	
Supply voltage range		8		20	V
Supply current, I_{CC}	Electronic switching on		16	24	mA
Voltage gain (pins 5-3)	$f = 1\text{kHz}$ (pins 6 and 2 connected)	25.5	26	26.5	dB
Voltage gain (pins 3-7)	$f = \text{kHz}$, 0dB at pin 3, noise reduction out	-0.5	0	+0.5	dB
Voltage gain (pins 2-3)	$f = 1\text{kHz}$		13		dB
Distortion THD; 2nd and 3rd harmonic	$f = 20\text{Hz}$ to 10kHz , 0dB		0.05	0.1	%
	$f = 20\text{Hz}$ to 10kHz , +10dB		0.15	0.3	%
Signal handling	1% distortion at 1kHz	+12	+15		dB
Signal-to-noise ratio*	Record mode	68	72		dB
	Playback mode	78	82		dB
Back-to-back frequency response	Using typical record mode response		± 0.5		dB
Record mode frequency response (at pin 7) referenced to encode monitor point (pin 3)	$f = 1.4\text{kHz}$ 0dB	-0.5	0	+0.5	dB
	-20dB	-16.1	-15.6	-15.1	dB
	-30dB	-23.5	-22.5	-21.5	dB
	$f = 5\text{kHz}$ 0dB	-0.7	+0.3	+1.3	dB
	-20dB	-17.3	-16.8	-16.3	dB
	-30dB	-22.3	-21.8	-21.3	dB
	-40dB	-30.2	-29.7	-29.2	dB
	$f = 20\text{kHz}$ 0dB	-0.3	+0.7	+1.7	dB
	-20dB	-18.3	-17.3	-16.3	dB
-30dB	-24.5	-23.5	-22.5	dB	
Input resistance	Pin 5	35	50	65	k Ω
	Pin 2	3.1	4.2	5.3	k Ω
Output resistance	Pin 6	1.9	2.4	3.1	k Ω
	Pin 3		80	120	Ω
	Pin 7		80	120	Ω
Back-to-back frequency response shift Versus T_A Versus V_{CC}	0°C to -70°C 8 to 20V		± 0.4		dB
			± 0.4		dB

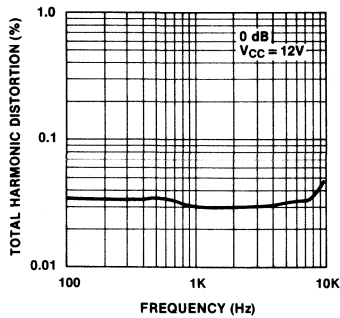
*All noise levels are measured CCIR/ARM weighted using a 10K source with respect to Dolby level. See Dolby Laboratories Bulletin 19.

DOLBY B/C TYPE NOISE REDUCTION CIRCUIT

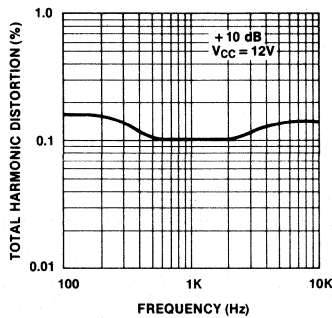
NE650

PERFORMANCE CHARACTERISTICS

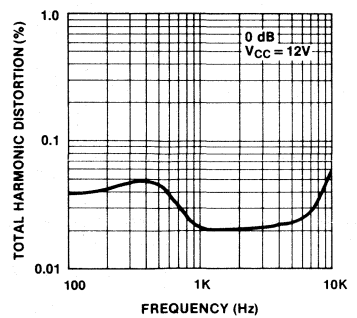
THD vs FREQUENCY RECORD MODE



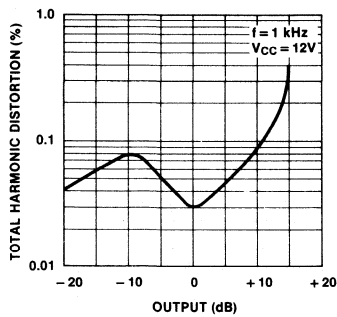
THD vs FREQUENCY RECORD MODE



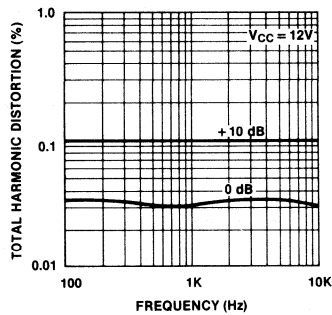
THD vs FREQUENCY PLAY MODE



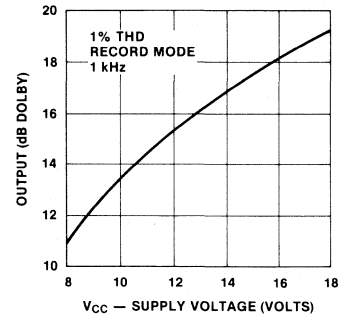
THD vs OUTPUT RECORD MODE



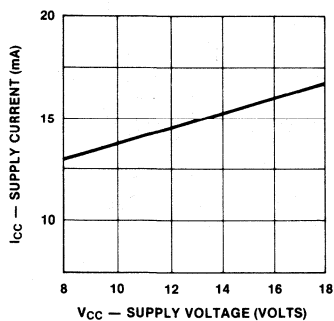
THD vs FREQUENCY NOISE REDUCTION (NR) OFF



MAXIMUM SIGNAL HANDLING vs SUPPLY VOLTAGE



SUPPLY CURRENT vs SUPPLY VOLTAGE



DOLBY B/C TYPE NOISE REDUCTION CIRCUIT

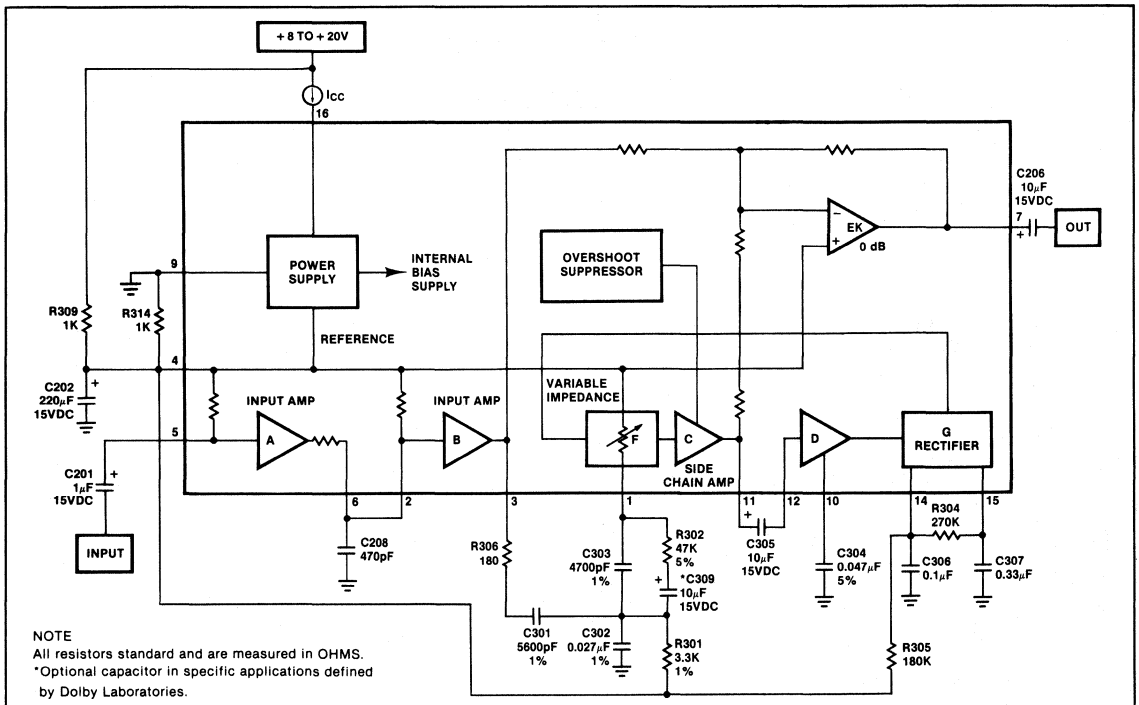
NE650

DOLBY ENCODER Output for constant level input (single tone frequency response)

Frequency (kHz)	Input Level (dB)								
	0 (Dolby Level)	-5	-10	-15	-20	-25	-30	-35	-40
0.1	0	0.1	0	0.1	0	0	0	0	0
0.14	0	0.2	0.2	0.2	0.2	0.2	0.1	0.2	0.1
0.2	0	0.3	0.4	0.5	0.5	0.6	0.6	0.5	0.5
0.3	0	0.3	0.6	1.1	1.3	1.3	1.3	1.3	1.3
0.4					2.0	2.1	2.2	2.3	2.1
0.5	0	0.3	0.8	1.8	2.6	2.9	2.9	3.0	2.9
0.6						3.6	3.7	3.8	3.7
0.7	0	0.4	0.9	2.1	3.5	4.3	4.4	4.5	4.4
0.8						4.8	5.0	5.3	5.1
0.9							5.6	5.8	5.6
1.0	0	0.4	1.0	2.3	4.2	5.7	6.1	6.3	6.2
1.2							6.9	7.1	7.1
1.4	0	0.3	0.9	2.3	4.4	6.6	7.5	7.7	7.7
2.0	0.1	0.4	0.9	2.2	4.3	7.0	8.5	8.9	8.9
3.0	0.2	0.6	0.9	1.9	3.9	6.6	8.8	9.7	9.7
5.0	0.3	0.6	1.0	1.7	3.2	5.4	8.2	10.0	10.3
7.0	0.3	0.6	1.0	1.7	2.8	4.7	7.3	9.7	10.4
10.0	0.4	0.7	1.1	1.7	2.6	4.2	6.5	9.1	10.4
14.0	0.5	0.8	1.1	1.8	2.7	4.4	6.5	8.7	10.3
20.0	0.7	0.7	1.2	1.9	2.7	4.4	6.5	8.7	10.3

NOTE
The figures given in this table are the average response of many of Dolby Laboratories' professional encoders, and are not intended to be taken as required consumer equipment performance characteristics. Thus, no inference should be drawn on the tolerances which licensees must retain in consumer equipment. The figures can, however, be used to plot typical characteristics.

TEST CIRCUIT NE650



Section 16 Phase Locked Loops

INDEX

Section 16 — Phase Locked Loops

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NE/SE567	Tone Decoder/Phase Locked Loop	16-20

PHASE-LOCKED LOOPS—SYMBOLS AND DEFINITIONS

T_A

Ambient temperature range. Range of the surrounding environment of the operating device.

T_J

Junction Temperature. The maximum temperature of the device. 150°C is standard for silicon devices.

TSTG

Storage temperature range. Temperature range that the device can be stored in a non-operating condition.

TSOLD

Soldering Temperature. The temperature which can be applied to the lead frame of the device for short periods of time (normally specified for a duration of 10 sec).

Truth Tables

0 is logic level low

1 is logic level high

X - don't care condition - has no effect under circuit conditions listed.

Absolute Maximum Rating

Operating safe zones exceeding these limits could cause permanent damage to the device and are not meant to imply that devices can operate at these limits.

Power Dissipation

The power that the device can safely handle at 25°C. The dissipation must be derated as indicated for the individual package type.

Package Type Designation

See full package designations in Appendix.

V_{CC} (-V_{CC})

Supply Voltage. The range of power supply voltage over which the device will operate safely.

FREE-RUNNING FREQUENCY (f₀['], ω₀[']).

Also called the *center frequency*, this is the frequency at which the loop VCO operates when not locked to an input signal. The "prime" superscripts are used to distinguish the free-running frequency from f₀['] and ω₀['] which are used for the general oscillator frequency. (Many references use f₀['] and ω₀['] for both the free-running and general oscillator frequency and leave the proper choice for the reader to infer from the context). The appropriate units for f₀['] and ω₀['] are Hz and radians per second respectively.

LOCK RANGE (2f_L, 2ω_L).*

The range of frequencies over which the loop will remain in lock. Normally the lock range is centered at the free-running frequency unless there is some nonlinearity in the system which limits the frequency deviation on one side of f₀[']. The deviations from f₀['] are referred to as the *Tracking Range* or *Hold-in Range*. (See figure 1.6). The tracking range is therefore one-half of the lock range.

CAPTURE RANGE (2f_C, 2ω_C).**

Although the loop will remain in lock throughout its lock range, it may not be able to acquire lock at the tracking range extremes because of the selectivity afforded by the low-pass filter. The cap-

ture range also is centered at f₀['] with the equal deviations called the *Lock-in* or *Pull-in Ranges*. The capture range can never exceed the lock range.

LOCK-UP TIME (t_L).***

The transient time required for a free-running loop to lock. This time depends principally upon the bandwidth selectivity designed into the loop with the low-pass filter. The lock-up time is inversely proportional to the selectivity bandwidth. Also, lock-up time exhibits a statistical spreading due to random initial phase relationships between the input and oscillator phases.

PHASE COMPARATOR CONVERSION GAIN (K_D).

The conversion constant relating the phase comparators output voltage to the phase difference between input and VCO signals when the loop is locked. At low input signal levels, K_D is also a function of signal amplitude. K_D has units of volts per radian (V/rad).

VCO CONVERSION GAIN (K_O).

The conversion constant relating the oscillators frequency shift from f₀['] to the applied input voltage. K_O has units of radians per second per volt (rad/sec/volt). K_O is a linear function of ω₀['] and must be obtained using a formula or graph provided or experimentally measured at the desired ω₀.

LOOP GAIN (K_V).

The product of K_D, K_O, and the low-pass filters gain at dc. K_D is evaluated at the appropriate input signal level and K_O at the appropriate ω₀[']. K_V has units of (sec)⁻¹.

CLOSED LOOP GAIN (CLG).

The output signal frequency and phase can be determined from a product of the CLG and the input signal where the CLG is given by

$$CLG = \frac{K_V}{1 + K_V} \quad (\text{Equation 1.4})$$

NATURAL FREQUENCY (ω_n).

The characteristic frequency of the loop, determined mathematically by the final pole positions in the complex plane or determined experimentally as the modulation frequency for which an underdamped loop gives the maximum frequency deviation from f₀['] and at which the phase error swing is the greatest.

DAMPING FACTOR (ζ).

The standard damping constant of a second order feedback system. For the PLL, ζ refers to the ability of the loop to respond quickly to an input frequency step without excessive overshoot.

LOOP NOISE BANDWIDTH (B_L).

A loop property relating ω_n and τ which describes the effective bandwidth of the received signal. Noise and signal components outside this bandwidth are greatly attenuated.

* Also called Synchronization Range.

** Also called Acquisition Range.

*** Also called Acquisition Time.

NOTE

Refer to Section 10 of the 1979 Analog Applications Manual for an in-depth explanation of Phase Locked Loops and their applications.

PHASE LOCKED LOOP

NE/SE564

DESCRIPTION

The NE564 is a versatile, high guaranteed frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

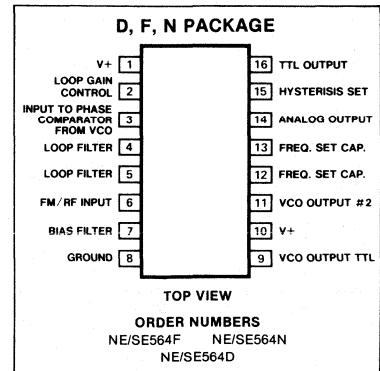
APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency synthesizers
- Signal generators
- Various satcom/TV systems

FEATURES

- Operation with single 5V supply
- TTL compatible inputs and outputs
- Guaranteed operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (Externally Controlled)

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V+	Supply voltage	V
	Pin 1	14
	Pin 10	6
P _D	Power dissipation	400 mW
T _A	Operating temperature	0 to 70 °C
	Operating temperature	SE -55 to +125
t _{stg}	Storage temperature	-65 to 150 °C

FUNCTIONAL DESCRIPTION

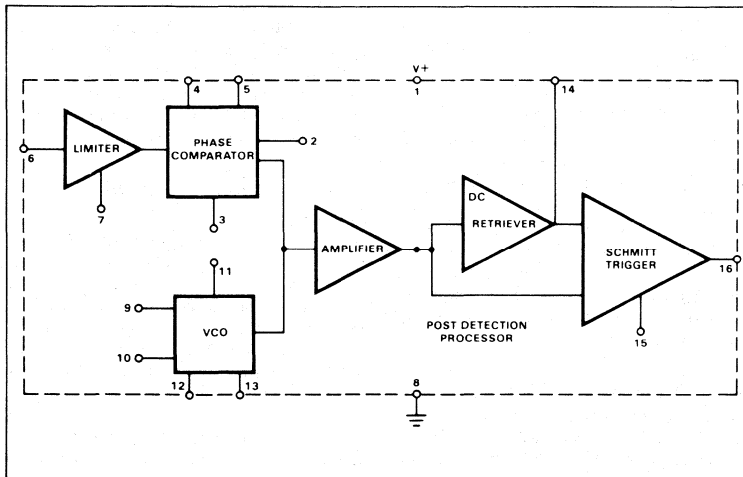
The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{in} - f_o)}{K_{VCO}} \quad \text{Equation 1}$$

K_{VCO} = conversion gain of the VCO (see figure 7)
 f_{in} = frequency of the input signal
 f_o = free running frequency of the VCO

BLOCK DIAGRAM



The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{in} from f_o. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the

PHASE LOCKED LOOP

NE/SE564

ELECTRICAL CHARACTERISTICS $V_{CC} = 5V$, $T_A = 25^\circ C$, $f_o = 5MHz$, $I_B = 400\mu A$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
		Min	Typ	Max	Min	Typ	Max	
VCO frequency	$C_1 = 6pF$	50	65		45	60		MHz
Lock range	Input $\geq 200mV_{rms}$ $T_A = 25^\circ C$ = $125^\circ C$ = $-55^\circ C$ = $0^\circ C$ = $70^\circ C$	40 20 70	70 30 90		40 50 25	70 70 40		% of f_o
Capture range	Input $\geq 200mV_{rms}$, $R_2 = R_3 = 27\Omega$	20	30		20	30		% of f_o
VCO frequency drift with temperature	$f_o = 5MHz$, $T_A = -55^\circ C$ to $125^\circ C$ = $0^\circ C$ to $70^\circ C$ $f_o = 500KHz$, $T_A = -55^\circ C$ to $125^\circ C$ = $0^\circ C$ to $70^\circ C$		400 250	1000 500		400 400 850	1250	PPM/ $^\circ C$
VCO free running frequency	$f_o = \frac{1}{25R_C C_1}$, $C_1 = 80pF$ $R_C = 100\Omega$ "Internal"	4	5	6	3.5	5	7	MHz
VCO frequency change with supply voltage	$V_{CC} = 4.5V$ to $5.5V$		3	8		3	8	% of f_o
Demodulated output voltage	Modulation frequency: 1KHz $f_o = 5MHz$, input deviation: 2%T = $25^\circ C$ 1%T = $25^\circ C$ = $0^\circ C$ = $-55^\circ C$ = $70^\circ C$ = $125^\circ C$	18 8 6 12	24 14 10 16		18 8 9.0 11.0	24 14 13 15		mVrms mVrms mVrms mVrms mVrms
Distortion Signal to noise ratio AM rejection	Deviation: 1% to 8% Std. condition, 1% to 10% dev. Std. condition, 30% AM		1 40 35			1 40 35		% dB dB
Demodulated Output at operating voltage	Modulation frequency: 1KHz $f_o = 5MHz$, input deviation: 1% $V_{CC} = 4.5V$ $V_{CC} = 5.5V$	7 8	12 14		7 8	12 14		mVrms mVrms
Supply current	$V_{CC} = 5V$ I_1 , I_{10}		45	60		45	60	mA
Output "1" output leakage current "0" output voltage	$V_{OUT} = 5V$, Pin 16, 9 $I_{OUT} = 2mA$, Pin 16, 9 $I_{OUT} = 6mA$, Pin 16, 9		1 0.3 0.4	20 0.6 0.8		1 0.3 0.4	20 0.6 0.8	μA V V

PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_o due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources Q_{25} – Q_{26} form the basic oscillator. The free running frequency of the oscillator is shown in the following equation:

$$f_o = \frac{1}{16R_C C_1} \quad \text{Equation 2}$$

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)
 C_1 = external frequency setting capacitor

Variation of V_d (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_Q with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped

vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transconductance

PHASE LOCKED LOOP

NE/SE564

amplifier Q42-Q43 together with an external capacitor which is connected at the amplifier output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_0 = \frac{g_m}{C_2} V_{in} dt \quad \text{Equation 3}$$

- g_m = transconductance of the amplifier
- C_2 = capacitor at the output (pin 14)
- V_{in} = signal voltage at amplifier input

With proper selection of C_2 , the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear modulation.

The comparator with hysteresis is made up of Q49-Q50 with positive feedback being provided by Q47-Q48. The hysteresis is varied by changing the current in Q52 with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

The free running frequency of the VCO is shown by the following equation:

$$f_0 = \frac{1}{16R_C C_1} \text{ in Hz} \quad \text{Equation 4}$$

- $R_C = 100\Omega$
- $C_1 = \text{external cap in farads}$

The loop filter diagram shown is explained by the following equation:

$$F(s) = \frac{1}{1 + sRC_3} \quad \text{Equation 5}$$

$$R = R_{12} = R_{13} = 1.3k\Omega \text{ (INTERNAL)}$$

By adding capacitors to pins 4 and 5, two poles are added to the loop transfer function

$$\omega = \frac{1}{RC_3}$$

FM DEMODULATOR

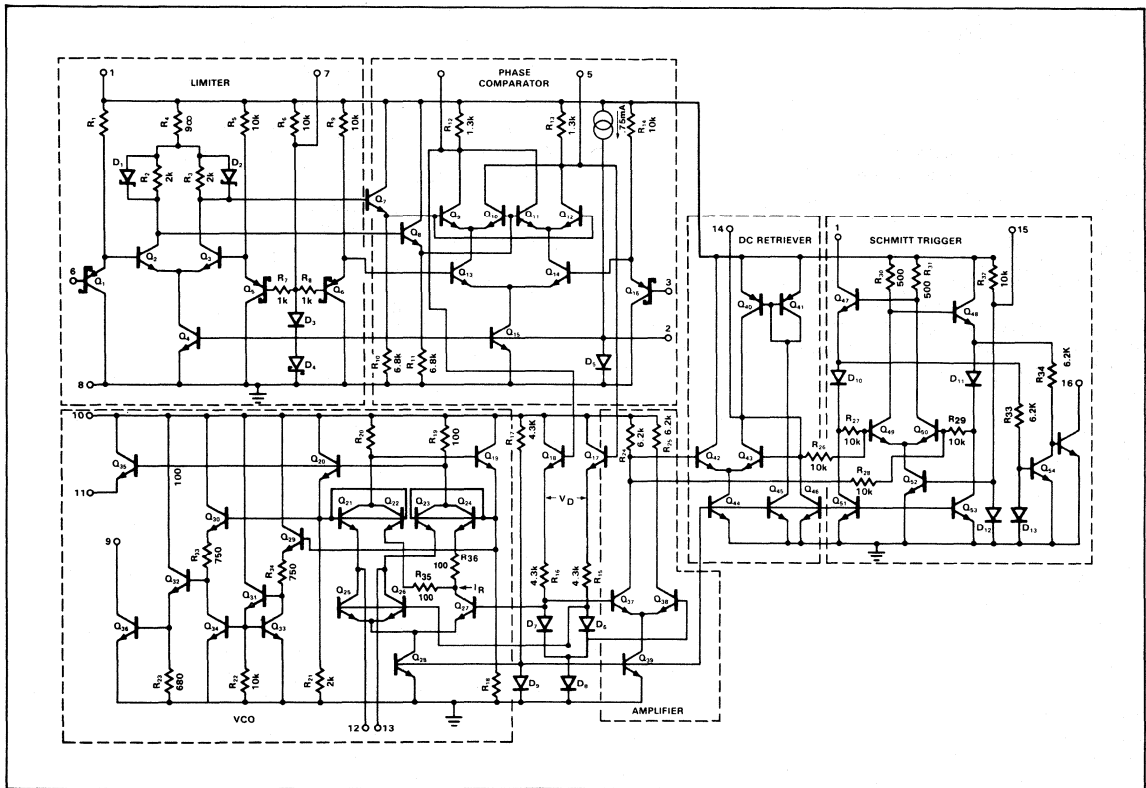
The NE564 can be used as an FM demodulator. The connections for operation

at 5V and 12V are shown in figures 2 and 3 respectively. The input signal is ac coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be fairly high (1% or higher).

MODULATION TECHNIQUES

The NE564 phase locked loop can be modulated at either the loop filter ports (pins 4 and 5) or the input port (pin 6) as shown in figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in figure 5. This curve will be appropriate for signals injected into pins 4 and 5 as shown in figure 4.

EQUIVALENT SCHEMATIC



PHASE LOCKED LOOP

NE/SE564

FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5 volt power supply. Demodulated dc voltages associated with the mark and space frequencies are recovered with a single external capacitor in a dc retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 6 shows a high-frequency FSK decoder designed for input frequency deviations of $\pm 1.0\text{MHz}$ centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_0 to 10.8MHz.

Figure 9 indicates that the $\pm 1.0\text{MHz}$ frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_0' frequencies.

The hysteresis was adjusted experimentally via the 10k Ω potentiometer and 2k Ω bias arrangement to give the waveshape shown in figure 7 for 20K, 500K, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparators outputs.

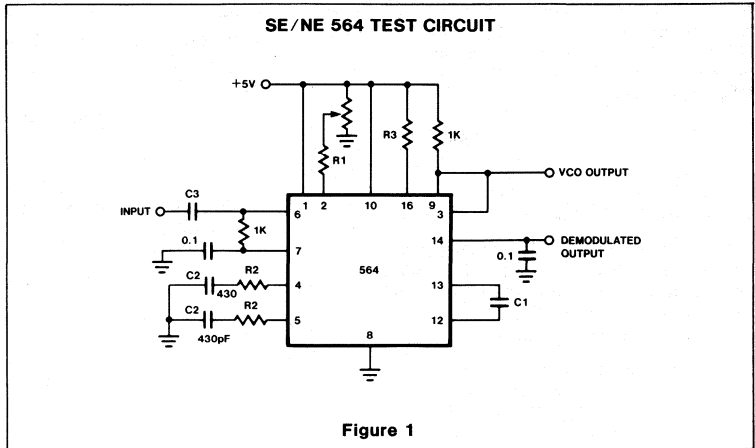


Figure 1

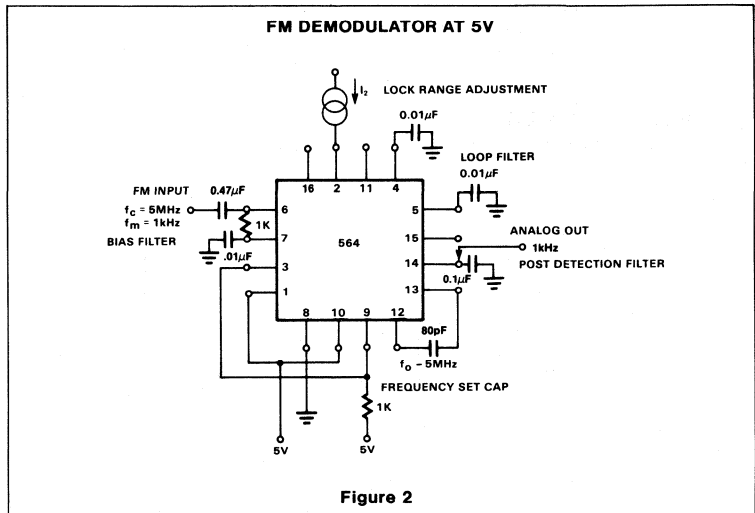
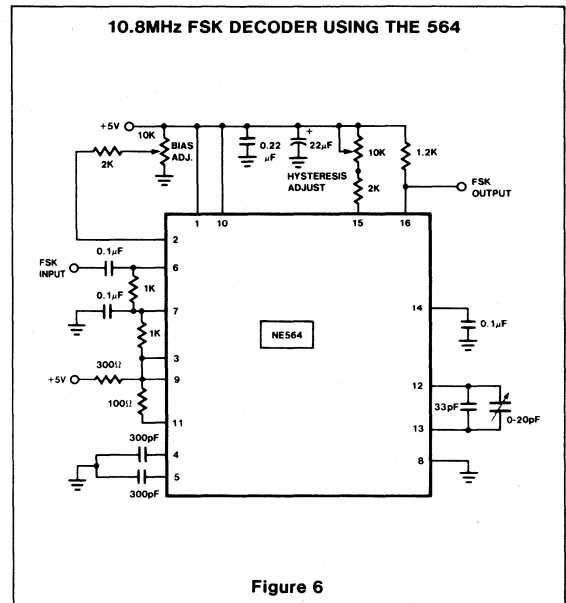
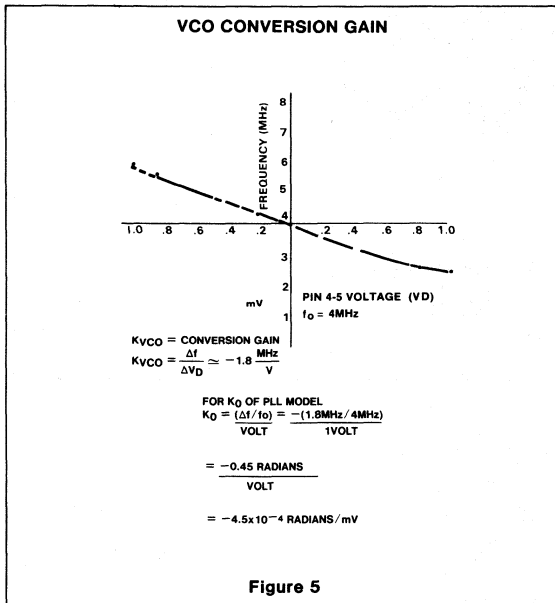
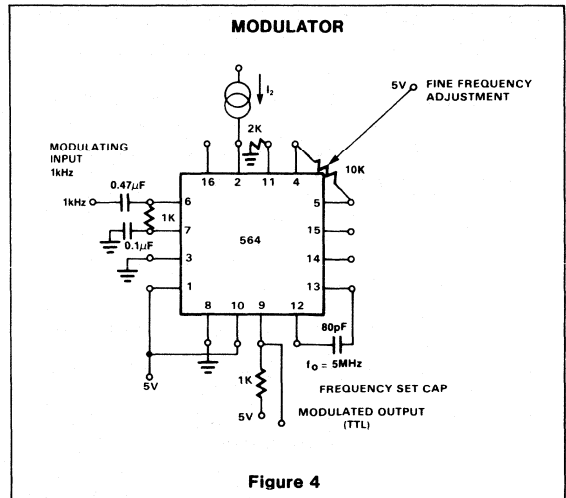
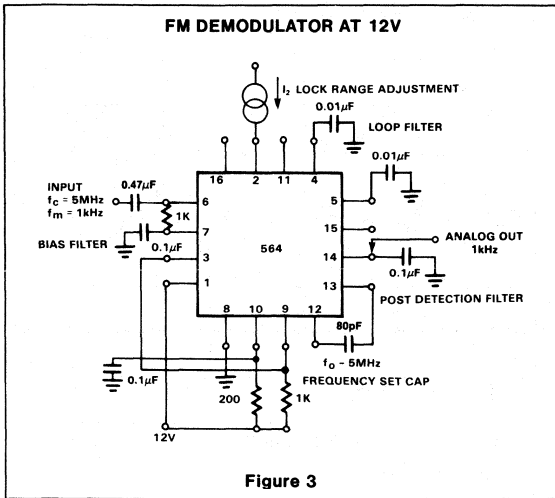


Figure 2

PHASE LOCKED LOOP

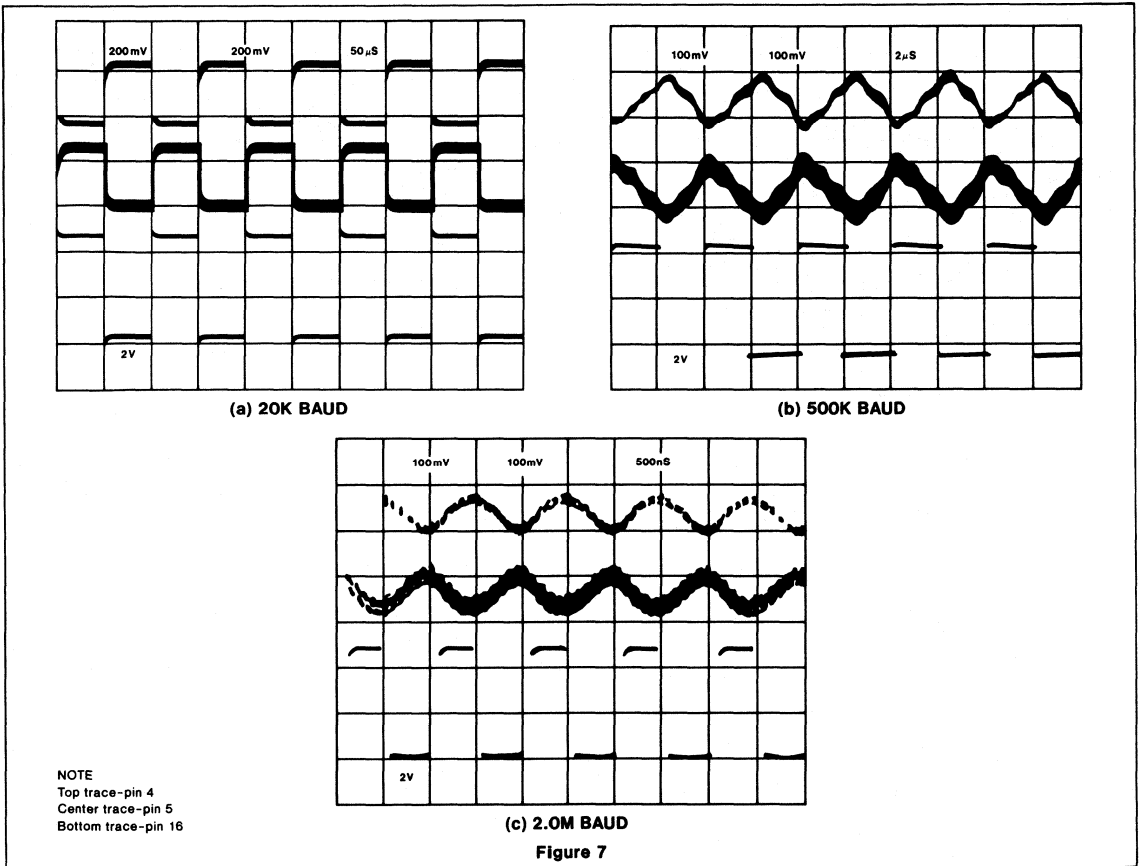
NE/SE564



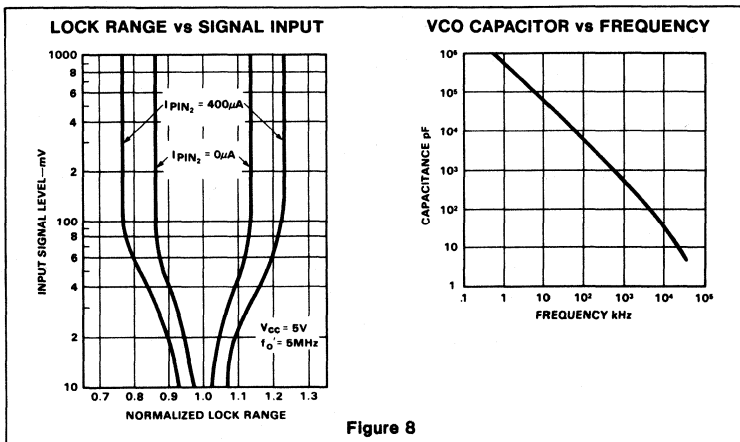
PHASE LOCKED LOOP

NE/SE564

PHASE COMPARATOR (PINS 4 AND 5) AND FSK (PIN 16) OUTPUTS FOR DATA RATES OF



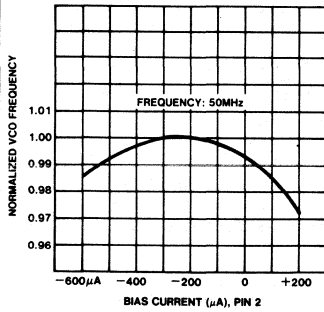
TYPICAL PERFORMANCE CHARACTERISTICS



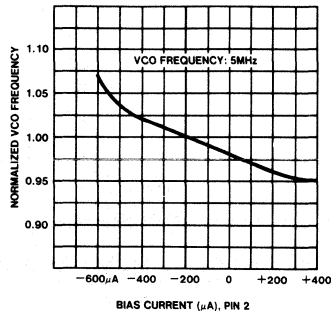
PHASE LOCKED LOOP

NE/SE564

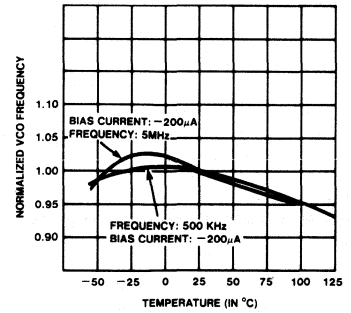
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



NORMALIZED VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



PHASE LOCKED LOOP

NE/SE565

DESCRIPTION

The SE/NE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001Hz to 500kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

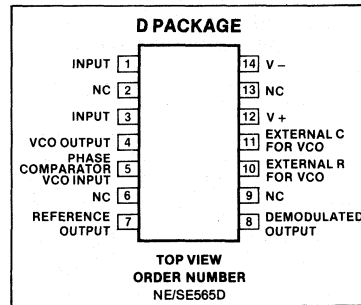
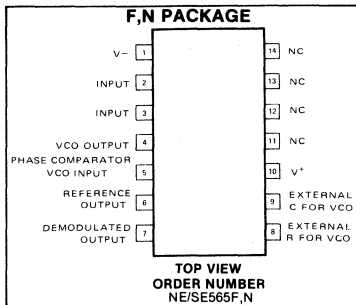
FEATURES

- Highly stable center frequency (200ppm/°C typ.)
- Wide operating voltage range (± 6 to ± 12 volts)
- Highly linear demodulated output (0.2% typ.)
- Center frequency programming by means of a resistor or capacitor, voltage or current
- TTL and DTL compatible square-wave output; loop can be opened to insert digital frequency divider
- Highly linear triangle wave output
- Reference output for connection of comparator in frequency discriminator
- Bandwidth adjustable from $< \pm 1\%$ to $> \pm 60\%$
- Frequency adjustable over 10 to 1 range with same capacitor

APPLICATIONS

- Frequency shift keying
- Modems
- Telemetry receivers
- Tone decoders
- SCA receivers
- Wideband FM discriminators
- Data synchronizers
- Tracking filters
- Signal restoration
- Frequency multiplication & division

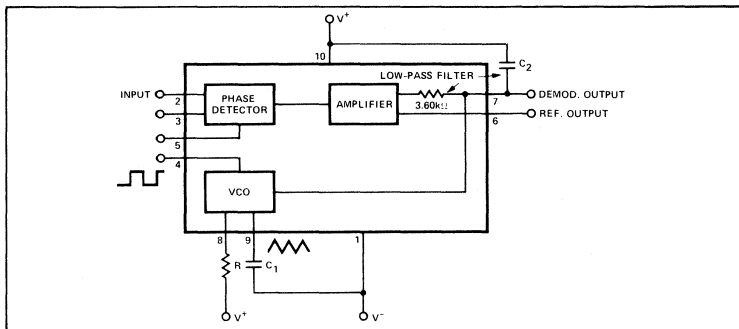
PIN CONFIGURATIONS



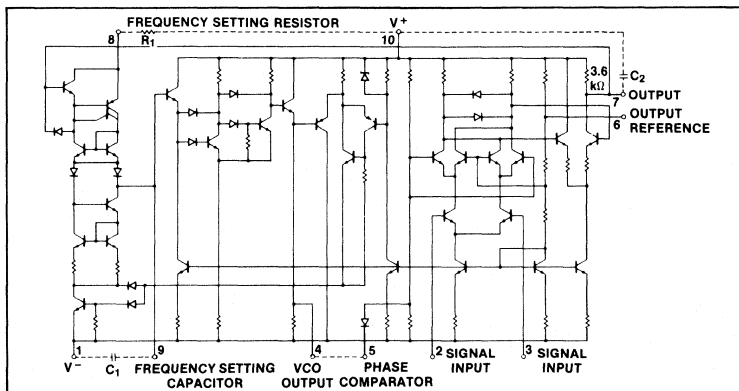
ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	V _{p-p}
Storage temperature	-65 to +150	°C
Operating temperature range	0 to +70	°C
NE565	-55 to +125	°C
SE565	300	mW
Power dissipation		

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



PHASE LOCKED LOOP

NE/SE565

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 6\text{V}$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE565			NE565			UNIT
		Min	Typ	Max	Min	Typ	Max	
SUPPLY REQUIREMENTS Supply voltage Supply current		12	8	± 12 12.5	± 6	8	± 12 12.5	V mA
INPUT CHARACTERISTICS Input impedance ¹ Input level required for tracking	$f_o = 50\text{kHz}$, $\pm 10\%$ frequency deviation	7 10	10 1		5 10	10 1		$k\Omega$ mVrms
VCO CHARACTERISTICS Center frequency Maximum value Distribution ²	$C_1 = 300\text{pF}$ Distribution taken about $f_o = 50\text{kHz}$, $R_1 = 5.0k\Omega$, $C_1 = 1200\text{pF}$	300	500			500		kHz
Drift with temperature Drift with supply voltage	$f_o = 50\text{kHz}$ $f_o = 50\text{kHz}$, $V_{CC} = \pm 6$ to ± 7 volts		200 0.1	1.0		300 0.2	1.5	ppm/ $^\circ\text{C}$ %/V
Triangle wave Output voltage level Amplitude Linearity		1.9	0 2.4 0.2	3	1.9	0 2.4 0.5	3	V Vp-p %
Square wave Logical "1" output voltage Logical "0" output voltage	$f_o = 50\text{kHz}$ $f_o = 50\text{kHz}$	+4.9	+5.2 -0.2	+0.2	+4.9	+5.2 -0.2	+0.2	V V
Duty cycle	$f_o = 50\text{kHz}$	45	50	55	40	50	60	%
Rise time Fall time			20 50	100 200		20 50		ns ns
Output current (sink) Output current (source)		0.6 5	1 10		0.6 5	1 10		mA mA
DEMODULATED OUTPUT CHARACTERISTICS Output voltage level Maximum voltage swing ³ Output voltage swing Total harmonic distortion Output impedance ⁴ Offset voltage (V6-V7) Offset voltage vs temperature (drift) AM rejection	Measured at pin 7 $\pm 10\%$ frequency deviation	4.25	4.5 2 300 0.2 3.6 30 50 30	4.75 0.75 100	4.0	4.5 2 300 0.4 3.6 50 100 40	5.0 200	V Vp-p mVp-p % $k\Omega$ mV $\mu\text{V}/^\circ\text{C}$ dB

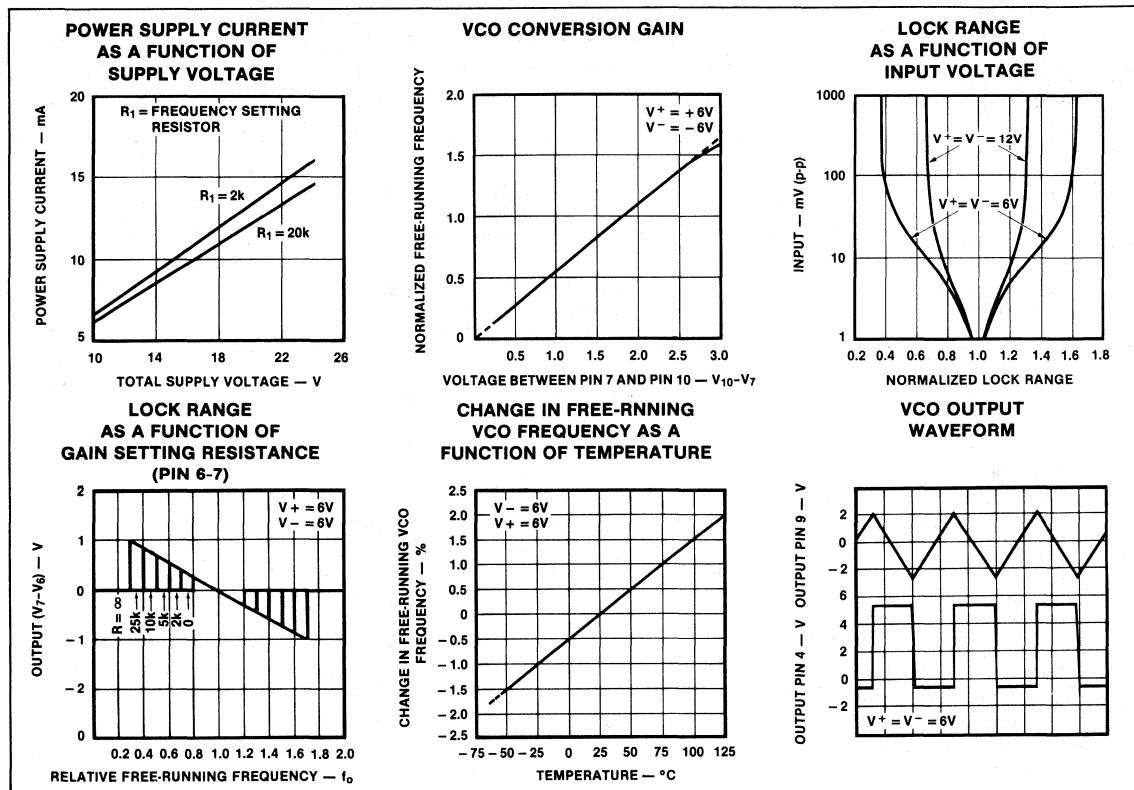
NOTES

- Both input terminals (pins 2 and 3) must receive identical dc bias. This bias may range from 0 volts to -4 volts.
- The external resistance for frequency adjustment (R1) must have a value between 2k Ω and 20k Ω .
- Output voltage swings negative as input frequency increases.
- Output not buffered.

PHASE LOCKED LOOP

NE/SE565

TYPICAL PERFORMANCE CHARACTERISTICS



DESIGN FORMULAS

(See Figure 1)

Free-running frequency of VCO: $f_0 \approx \frac{1.2}{4R_1C_1}$ in Hz

Lock-range: $f_L = \pm \frac{8f_0}{V_{CC}}$ in Hz

Capture-range: $f_C \approx \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C_2$

TYPICAL APPLICATIONS

FM Demodulation

The 565 Phase Locked Loop is a general purpose circuit designed for highly linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide bandwidth (typically $\pm 60\%$) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by

$f_0 = \frac{1.2}{4R_1C_1}$ and should be adjusted to be at the center of the input signal frequency range. C1 can be any value, but R1 should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be

decreased with little change in the free-running frequency. In this manner the lock range can be decreased from $\pm 60\%$ of f_0 to approximately $\pm 20\%$ of f_0 (at $\pm 6V$).

A small capacitor (typically 0.001 μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C2, connected between pin 7 and the positive supply, and an internal resistance of approximately 3600 ohms.

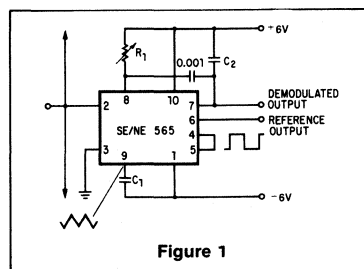


Figure 1

PHASE LOCKED LOOP

NE/SE565

Frequency Shift Keying (FSK)

FSK refers to data transmission by means of a carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070Hz and 1270Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

The loop filter capacitor C2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150Hz) and twice the input frequency (approximately 2200Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R1 so as to result in a slightly-positive voltage at the output with $f_{IN} = 1070\text{Hz}$.

The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600-ohm input impedance).

Frequency Multiplication

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be

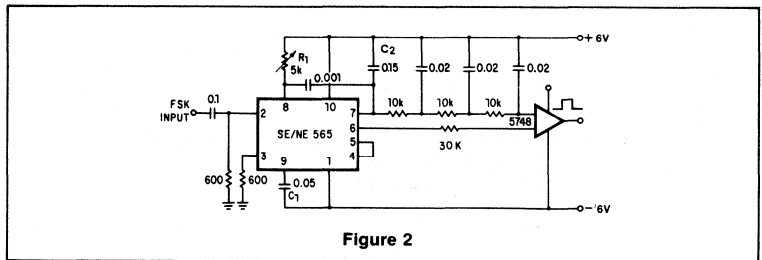


Figure 2

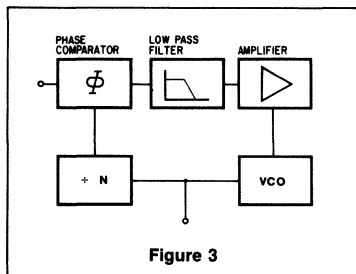


Figure 3

a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R1 and C1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C2, should be large enough to eliminate variations in the demodulated output voltage (at pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_{IN}) as long as the loop is in lock.

SCA (Background Music) Decoder

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this a frequency modulated subcarrier of 67kHz is used. The frequency is chosen so

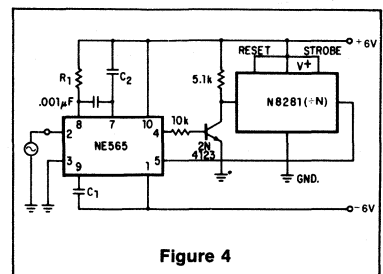


Figure 4

as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

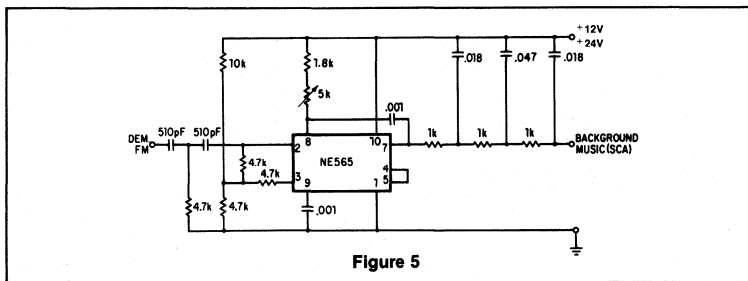
A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80mV and 300mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67kHz with a 5000 ohm potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50mV and the frequency response extends to 7kHz.

PHASE LOCKED LOOP

NE/SE565



FUNCTION GENERATOR

NE/SE566

DESCRIPTION

The NE/SE 566 Function Generator is a voltage controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage, with exceptional linearity.

FEATURES

- Wide range of operating voltage (up to 24 volts)
- High linearity of modulation
- Highly stable center frequency (200 ppm/°C typical)
- Highly linear triangle wave output
- Frequency programming by means of a resistor or capacitor, voltage or current
- Frequency adjustable over 10 to 1 range with same capacitor

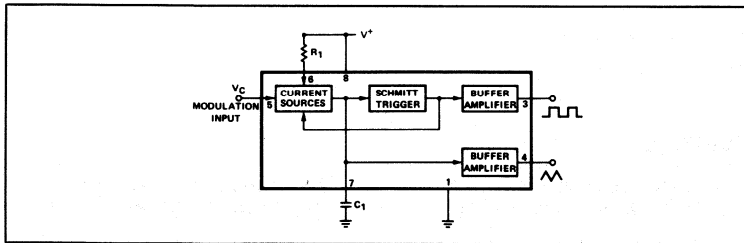
APPLICATIONS

- Tone generators
- Frequency shift keying
- FM modulators
- Clock generators
- Signal generators
- Function generators

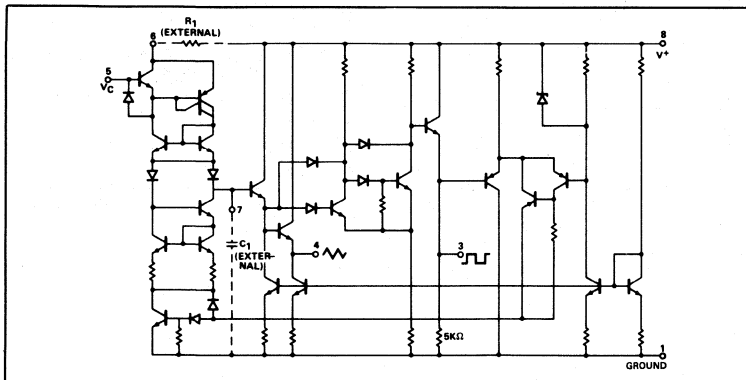
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Maximum operating voltage	26	V
Input voltage	3	V _{P-P}
Storage temperature	-65 to +150	°C
Operating temperature range		
NE566	0 to +70	°C
SE566	-55 to +125	°C
Power dissipation	300	mW

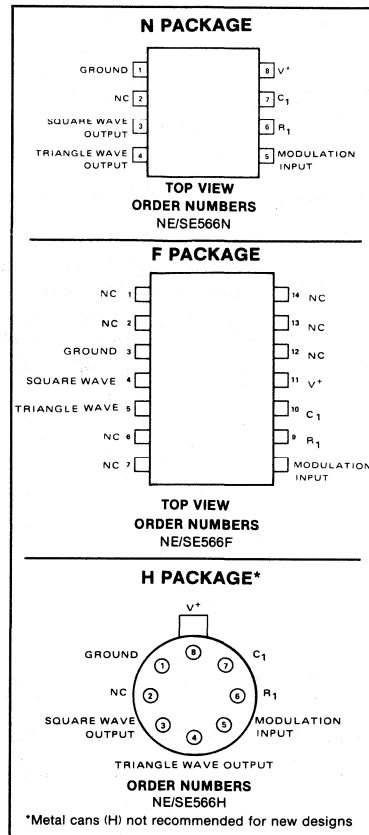
BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



PIN CONFIGURATIONS



FUNCTION GENERATOR

NE/SE566

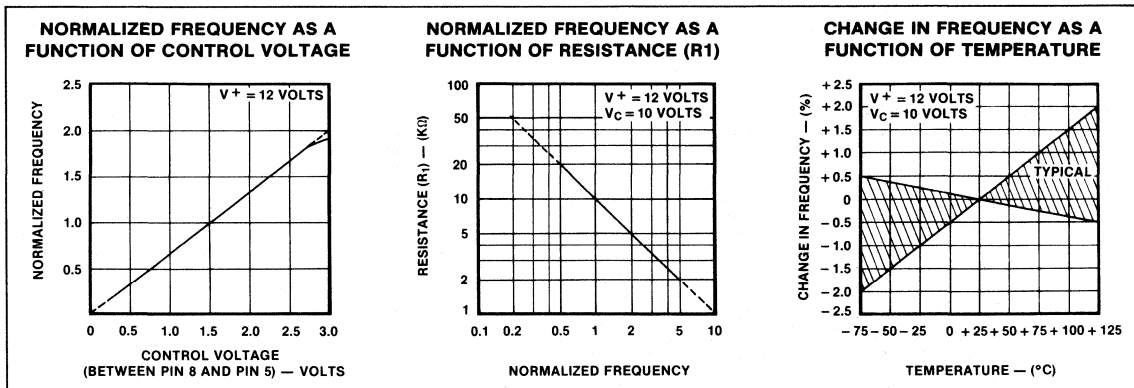
ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$; $V_{CC} = 12\text{V}$ unless otherwise specified.

PARAMETER	SE566			NE566			UNIT
	Min	Typ	Max	Min	Typ	Max	
GENERAL							
Operating temperature range	-55		125	0		70	$^\circ\text{C}$
Operating supply voltage			24			24	V
Operating supply current		7	12.5		7	12.5	mA
VCO¹							
Maximum operating frequency		1			1		MHz
Frequency drift with temperature		200			300		ppm/ $^\circ\text{C}$
Frequency drift with supply voltage		1			2		%/V
Control terminal input impedance ²		1			1		$\text{M}\Omega$
FM distortion ($\pm 10\%$ deviation)		0.2	0.75		0.4	1.5	%
Maximum sweep rate		1			1		MHz
Sweep range		10:1			10:1		
OUTPUT							
Triangle wave output							
Impedance		50			50		Ω
Voltage	1.9	2.4		1.9	2.4		V _{pp}
Linearity		0.2			0.5		%
Square wave input							
Impedance		50			50		Ω
Voltage	5	5.4		5	5.4		V _{pp}
Duty Cycle	45	50	55	40	50	60	%
Rise time		20			20		ns
Fall Time		50			50		ns

NOTES

- The external resistance for frequency adjustment (R_1) must have a value between $2\text{k}\Omega$ and $20\text{k}\Omega$.
- The bias voltage (V_C) applied to the control terminal (pin 5) should be in the range $3/4V^+ \leq V_C \leq V^+$.

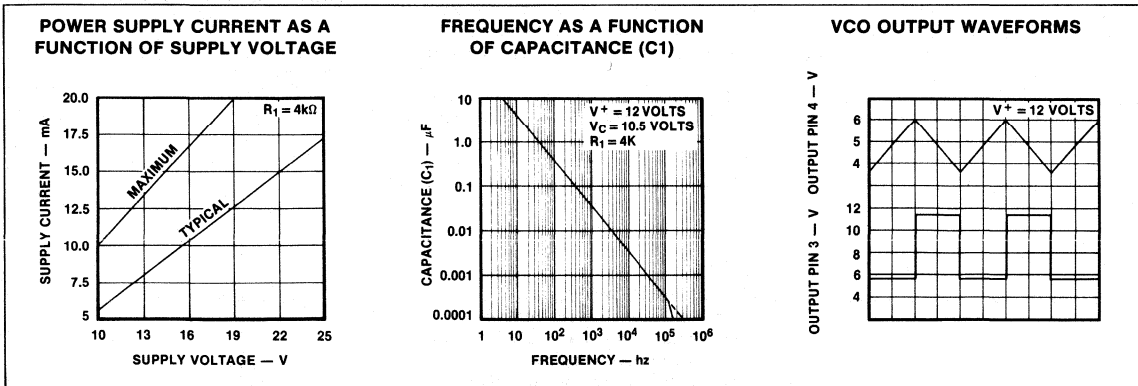
TYPICAL PERFORMANCE CHARACTERISTICS



FUNCTION GENERATOR

NE/SE566

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)



OPERATING INSTRUCTIONS

The SE/NE 566 Function Generator is a general purpose voltage controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1MHz. A typical connection diagram is shown in Figure 1. The control terminal (pin 5) must be biased externally with a voltage (V_C) in the range

$$3/4 V^+ \leq V_C \leq V^+$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3 . The modulating signal is then ac coupled with

the capacitor C_2 . The modulating signal can be direct coupled as well, if the appropriate dc bias voltage is applied to the control terminal. The frequency is given approximately by

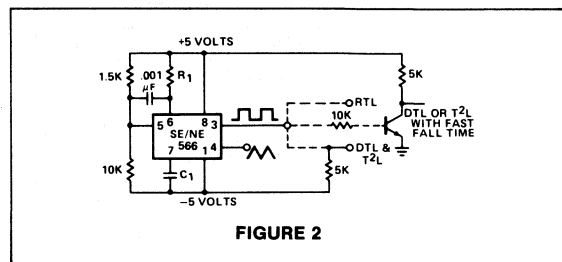
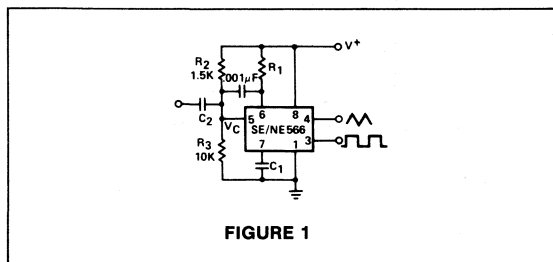
$$f_o = \frac{2[(V^+) - (V_C)]}{R_1 C_1 V^+}$$

and R_1 should be in the range $2k\Omega < R_1 < 20k\Omega$.

A small capacitor (typically $0.001\mu f$) should be connected between pins 5 and 6 to eliminate possible oscillation in the control current source.

If the VCO is to be used to drive standard

logic circuitry, it may be desirable to use a dual supply of ± 5 volts as shown in Figure 2. In this case the square wave output has the proper dc levels for logic circuitry. RTL can be driven directly from pin 3. For DTL or T2L gates, which require a current sink of more than 1mA, it is usually necessary to connect a $5k\Omega$ resistor between pin 3 and negative supply. This increases the current sinking capability to 2mA. The third type of interface shown uses a saturated transistor between the 566 and the logic circuitry. This scheme is used primarily for T2L circuitry which requires a fast fall time ($< 50ns$) and a large current sinking capability.



NE/SE567

TONE DECODER/PHASE LOCKED LOOP

DESCRIPTION

The SE/NE567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

FEATURES

- Wide frequency range (.01Hz to 500kHz)
- High stability of center frequency
- Independently controllable bandwidth (up to 14 percent)
- High out-band signal and noise rejection
- Logic-compatible output with 100mA current sinking capability
- Inherent immunity to false signals
- Frequency adjustment over a 20 to 1 range with an external resistor
- Military processing available

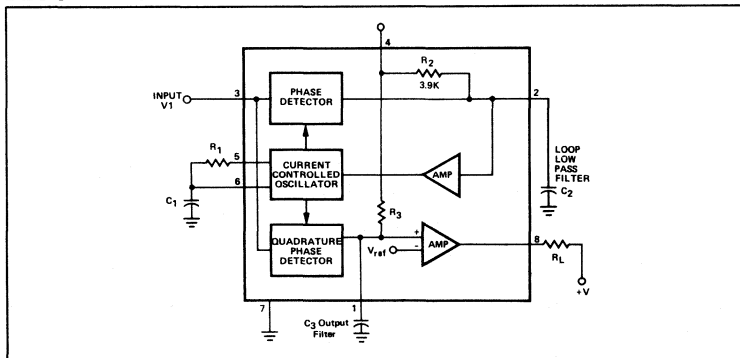
APPLICATIONS

- Touch Tone® decoding
- Carrier current remote controls
- Ultrasonic controls (remote TV, etc.)
- Communications paging
- Frequency monitoring and control
- Wireless intercom
- Precision oscillator

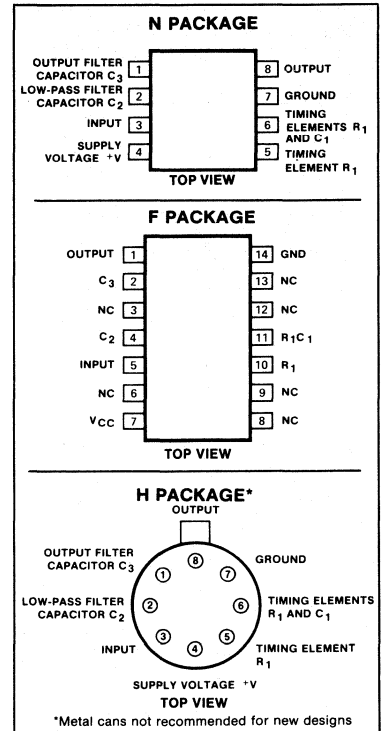
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Operating temperature		
NE567	0 to +70	°C
SE567	-55 to +125	°C
Operating voltage	10	V
Positive voltage at input	0.5 + V _S	V
Negative voltage at input	-10	Vdc
Output voltage (collector of output transistor)	15	Vdc
Storage temperature	-65 to +150	°C
Power dissipation	300	mW

BLOCK DIAGRAM



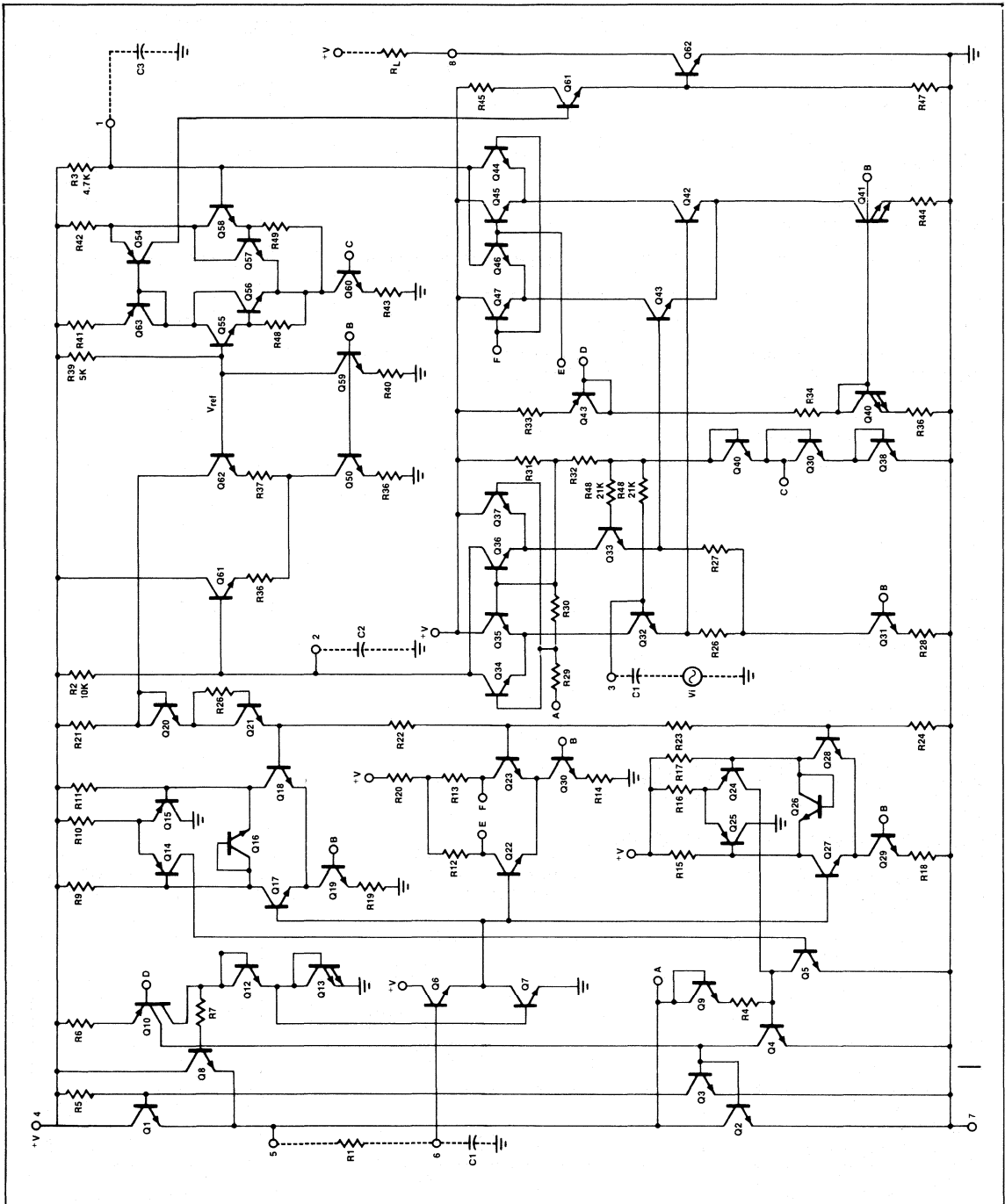
PIN CONFIGURATIONS



tone decoder/phase locked loop

NE/SE567

EQUIVALENT SCHEMATIC



TONE DECODER/PHASE LOCKED LOOP

NE/SE567

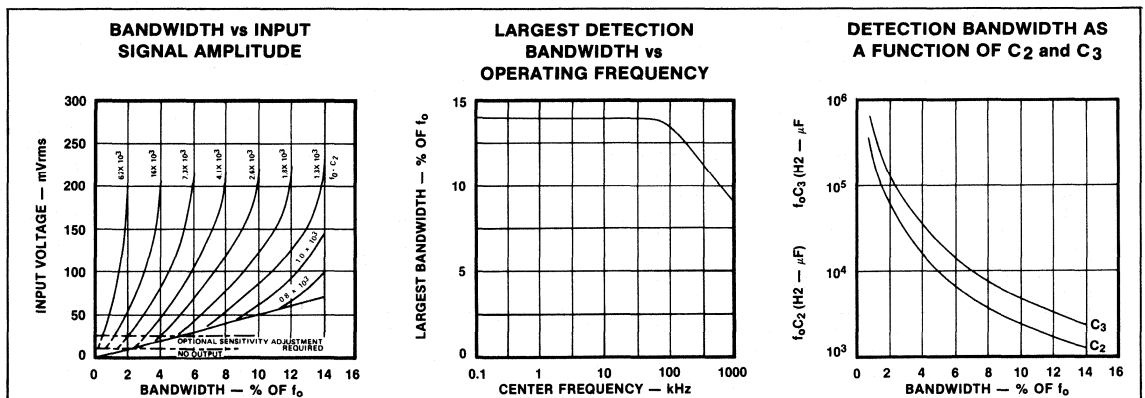
DC ELECTRICAL CHARACTERISTICS (V+ = 5.0V; TA = 25°C unless otherwise specified.)

PARAMETER	TEST CONDITIONS	SE567			NE567			UNIT
		Min	Typ	Max	Min	Typ	Max	
CENTER FREQUENCY ¹ Highest center frequency (fo) Center frequency stability ² Center frequency shift with supply voltage	-55 to +125°C 0 to +70°C fo = 100kHz	100	500 35±140 35±60 0.5		100	500 35±140 35±60 0.7		kHz ppm/°C ppm/°C %/V
DETECTION BANDWIDTH Largest detection bandwidth Largest detection bandwidth skew Largest detection bandwidth—variation with temperature Largest detection bandwidth—variation with supply voltage	fo = 100kHz Vi = 300mVrms Vi = 300mVrms	12	14 2 ±0.1 ±2	16 4	10	14 3 ±0.1 ±2	18 6	% of fo % of fo %/°C %/V
INPUT Input resistance Smallest detectable input voltage (Vi) Largest no-output input voltage Greatest simultaneous outband signal to inband signal ratio Minimum input signal to wideband noise ratio	IL = 100mA, fi = fo IL = 100mA, fi = fo Bn = 140kHz		20 10 15 +6 -6	25	10	20 15 +6 -6	25	kΩ mVrms mVrms dB dB
OUTPUT Fastest on-off cycling rate "1" output leakage current "0" output voltage Output fall time ³ Output rise time ³	IL = 30mA IL = 100mA RL = 50Ω RL = 50Ω		fo/20 0.01 0.2 0.6 30 150	25 0.4 1.0		fo/20 0.01 0.2 0.6 30 150	25 1.0	μA V V ns ns
GENERAL Operating voltage range Supply current quiescent Supply current—activated Quiescent power dissipation	RL = 20kΩ	4.75	6 11 30	9.0 8 13	4.75	7 12 35	9.0 10 15	V mA mA mW

NOTES

1. Frequency determining resistor R1 should be between 1 and 20kΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback RL network selected to eliminate pulsing during turn-on and turn-off.

TYPICAL PERFORMANCE CHARACTERISTICS

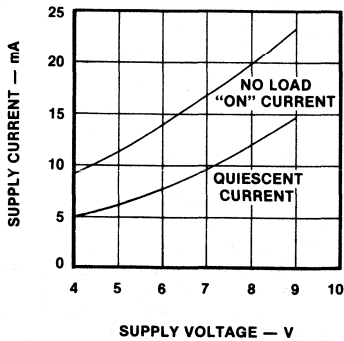


TONE DECODER/PHASE LOCKED LOOP

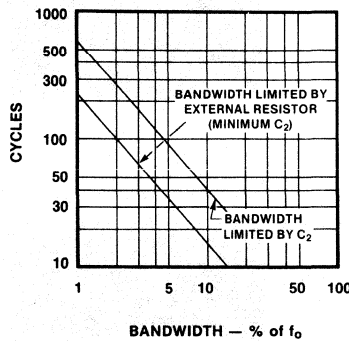
NE/SE567

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

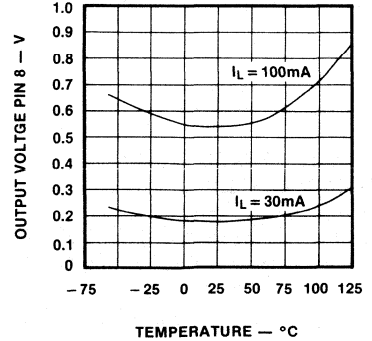
TYPICAL SUPPLY CURRENT vs SUPPLY VOLTAGE



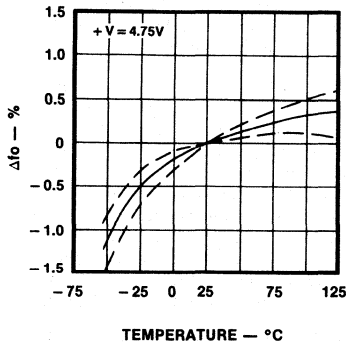
GREATEST NUMBER OF CYCLES BEFORE OUTPUT



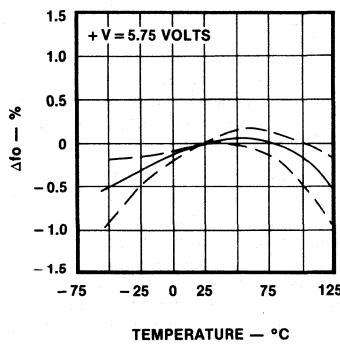
TYPICAL OUTPUT VOLTAGE vs TEMPERATURE



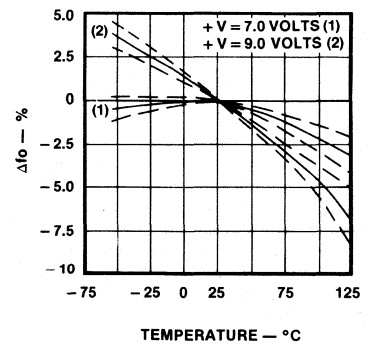
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



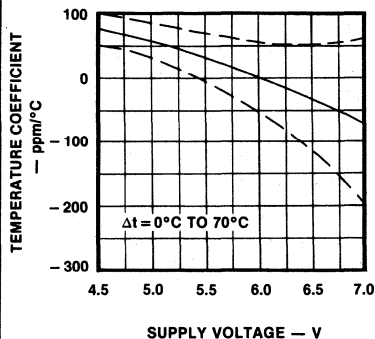
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



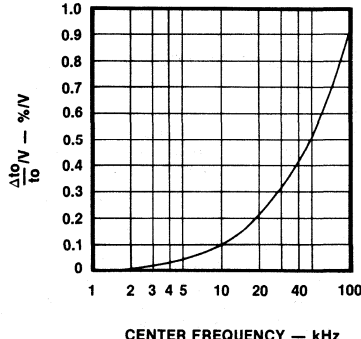
TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



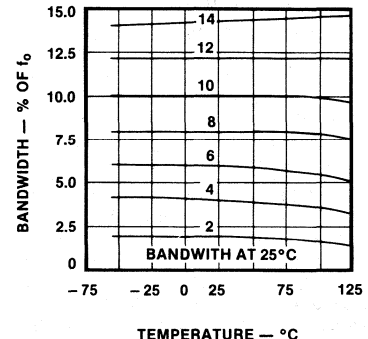
CENTER FREQUENCY TEMPERATURE COEFFICIENT (MEAN AND S.D.)



CENTER FREQUENCY SHIFT WITH SUPPLY VOLTAGE CHANGE vs OPERATING FREQUENCY



TYPICAL BANDWIDTH VARIATION WITH TEMPERATURE



tone decoder/phase locked loop

NE/SE567

DESIGN FORMULAS

$$f_0 = \frac{1.1}{R_1 C_1}$$

$$BW \approx 1070 \sqrt{\frac{V_1}{f_0 C_2}} \text{ in \% of } f_0, V_1 \leq 200\text{mVrms}$$

Where

$$V_1 = \text{Input Voltage (Vrms)}$$

$$C_2 = \text{Low-Pass Filter Capacitor } (\mu\text{F})$$

PHASE LOCKED LOOP TERMINOLOGY CENTER FREQUENCY (f_0)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

Detection Bandwidth (BW)

The frequency range, centered about f_0 , within which an input signal above the threshold voltage (typically 20mVrms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

Lock Range

The largest frequency range within which an input signal above the threshold voltage will hold a logical zero state on the output.

Detection Band Skew

A measure of how well the detection band is centered about the center frequency, f_0 . The skew is defined as $(f_{\max} + f_{\min} - 2f_0)/2f_0$ where f_{\max} and f_{\min} are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

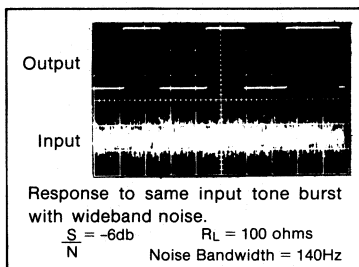
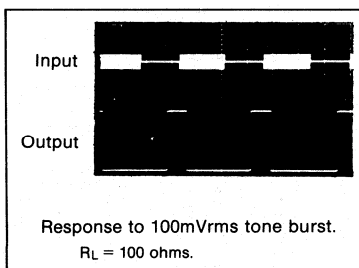
OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1 , C_1 , C_2 and C_3 .

1. Select R_1 and C_1 for the desired center frequency. For best temperature stability, R_1 should be between 2K and 20K ohm, and the combined temperature coefficient of the $R_1 C_1$ product should have sufficient stability over the projected temperature range to meet the necessary requirements.

2. Select the low pass capacitor, C_2 , by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of $f_0 C_2$ necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, con-

TYPICAL RESPONSE

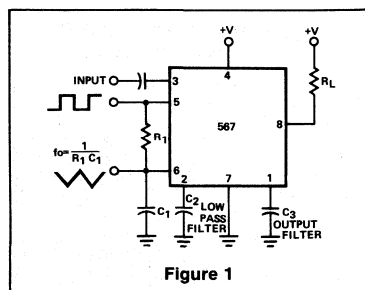


stant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the $f_0 C_2$ product (f_0 (Hz), C_2 (μ fd)).

3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is 2C2.

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output which is a linear function of frequency over the range of 0.95 to 1.05 f_0 with a slope of about 20mV per percent of frequency deviation. The average voltage at pin 1 is, during lock, a function of the inband input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave



output of magnitude $(+V - 2V_{BE}) \approx (+V - 1.4V)$ having a dc average of $+V/2$. A 1k Ω load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak with an average dc level of $+V/2$. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user achieve the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in-band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_0/3$, $f_0/5$, etc.

2. The 567 will lock onto signals near $(2n + 1) f_0$, and will give an output for signals near $(4n + 1) f_0$ where $n=0, 1, 2$, etc. Thus, signals at $5f_0$ and $9f_0$ can cause an unwanted output. If such signals are anticipated, they should be attenuated before reaching the 567 input.

3. Maximum immunity from noise and out-band signals is afforded in the low input level (below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs Bandwidth graph.

4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with a 0.01 μ F or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and

TONE DECODER/PHASE LOCKED LOOP

NE/SE567

unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_0/10$ baud.

$$C_2 = \frac{130}{f_0} \mu F$$

$$C_3 = \frac{260}{f_0} \mu F$$

In cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS (Figure 3)

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is

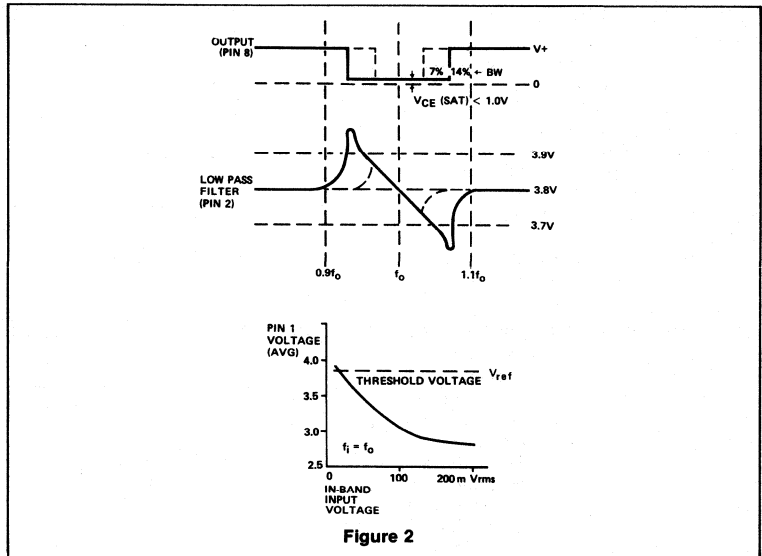


Figure 2

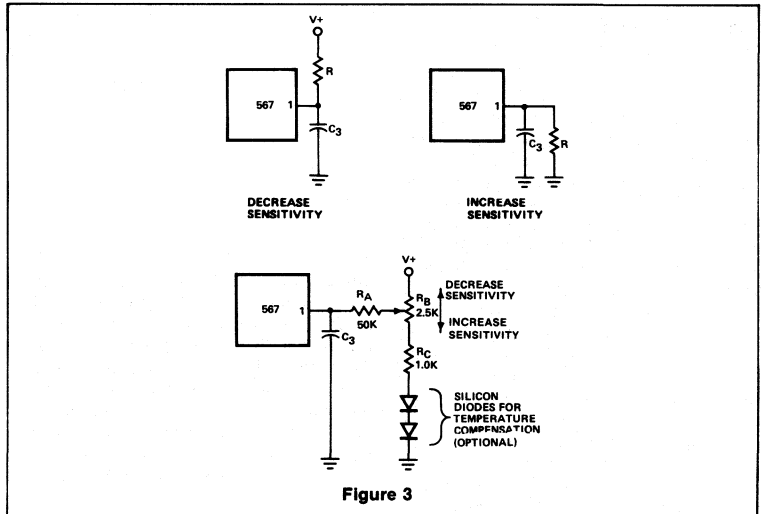


Figure 3

taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results the resistors used, except where noted, should have the same

temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

TONE DECODER/PHASE LOCKED LOOP

NE/SE567

SENSITIVITY ADJUSTMENT

(Figure 3)

When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10mV or lower).

By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION (Figure 4)

Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input (pin 1) the chatter can be eliminated. Three schemes for doing this are given in Figure 4. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT

(Figure 5)

When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the lock range, the

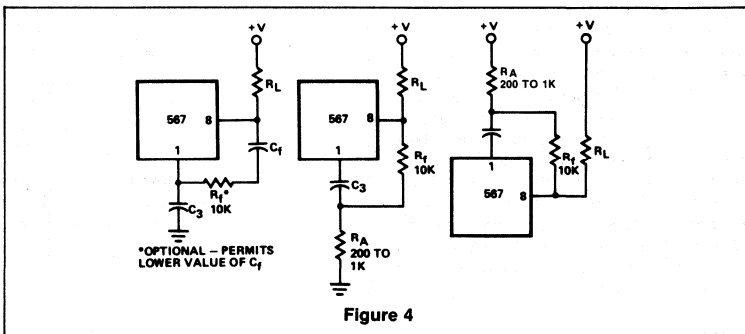


Figure 4

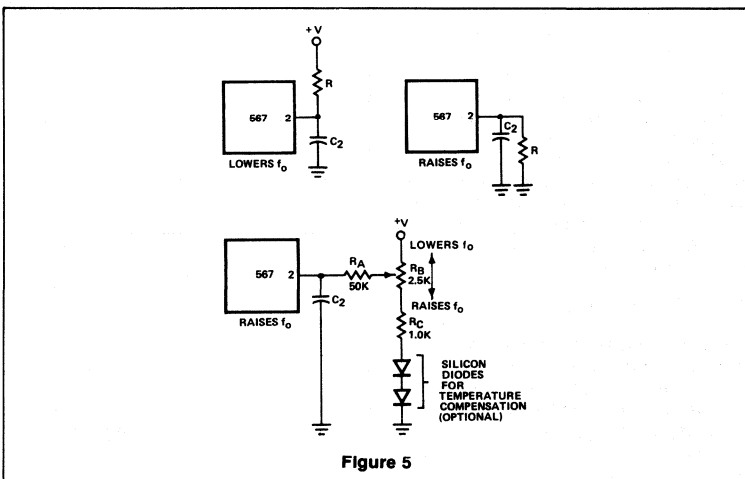


Figure 5

circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

(Figure 6)

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band conditions. Note that the reduced impedance level at terminal 2 will require that a larger

value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the network of R_B and R_C can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

OUTPUT LATCHING (Figure 7)

To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

REDUCTION OF C_1 VALUE

(Figure 8)

For precision very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

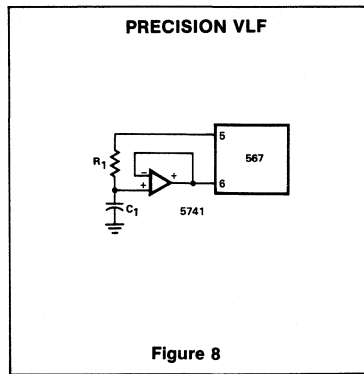
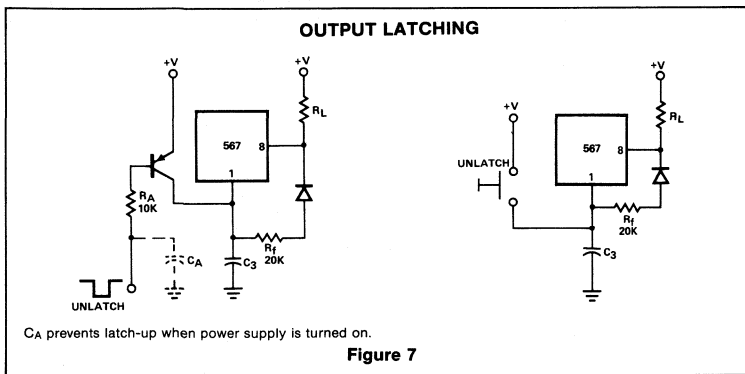
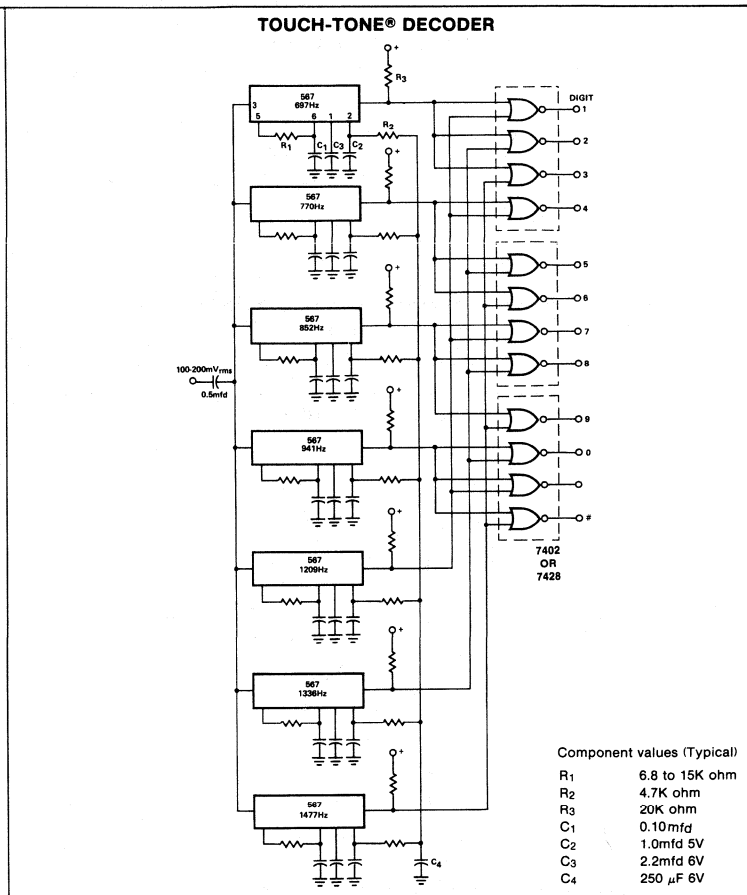
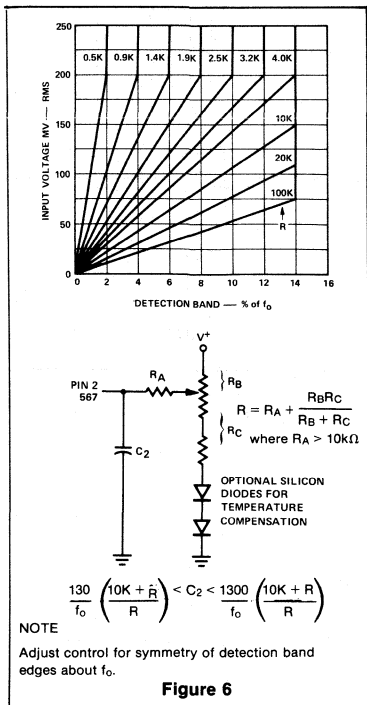
TONE DECODER/PHASE LOCKED LOOP

NE/SE567

PROGRAMMING

To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.

TYPICAL APPLICATIONS

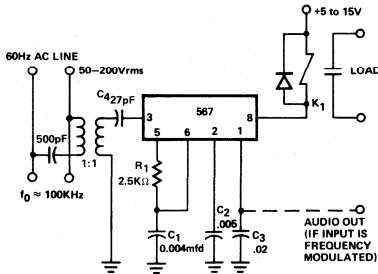


tone decoder/phase locked loop

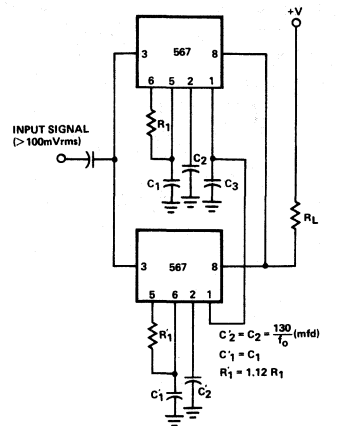
NE/SE567

TYPICAL APPLICATIONS (Cont'd)

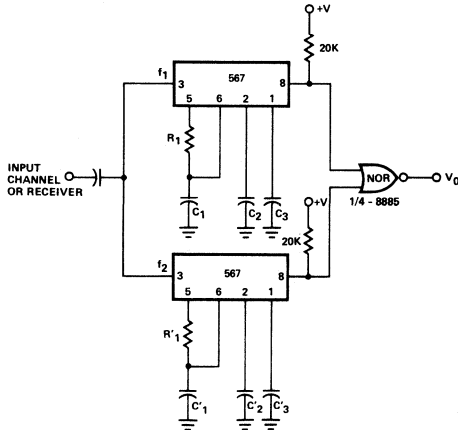
CARRIER-CURRENT REMOTE CONTROL OR INTERCOM



24% BANDWIDTH TONE DECODER

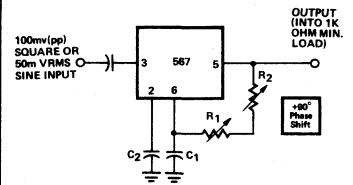


DUAL-TONE DECODER



1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential ($f_1 f_2$) tones is possible.

0° to 180° PHASE SHIFTER



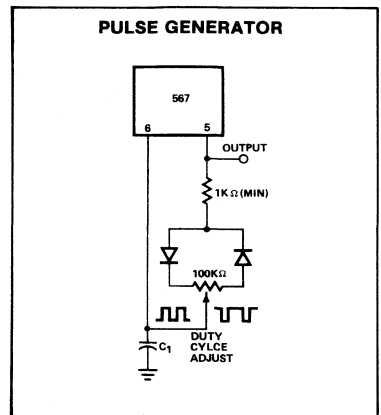
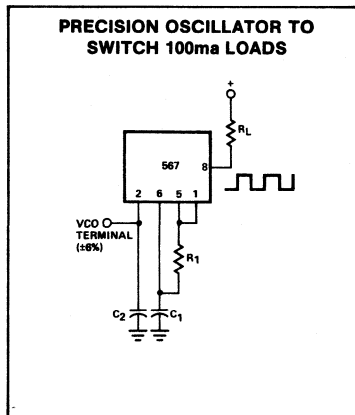
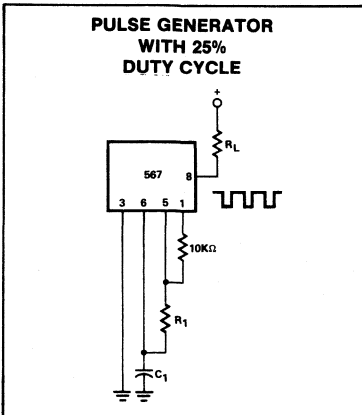
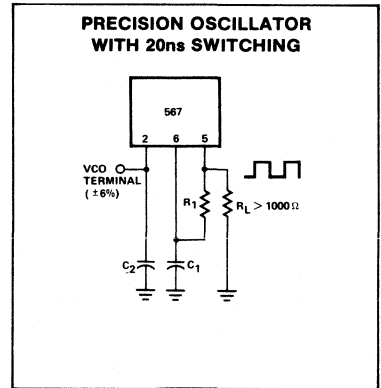
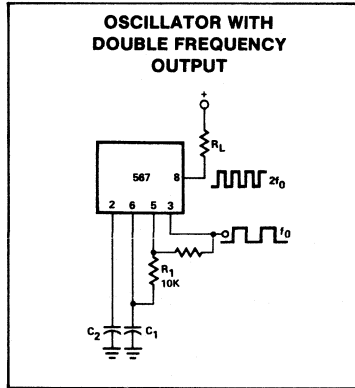
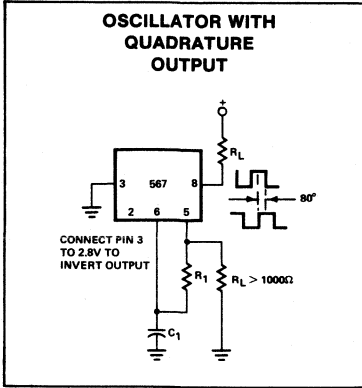
$R_2 = R_1/5$

Adjust R_1 so that $\phi = 90^\circ$ with control midway

TONE DECODER/PHASE LOCKED LOOP

NE/SE567

TYPICAL APPLICATIONS (Cont'd)



NOTE
Application information available on request.

Section 17 Military

INDEX

Section 17 — Military

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MILITARY PRODUCTS/PROCESS LEVELS

The Signetics MIL 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Fully compliant 883 flows on all products.
- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customer to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3, 4 and 5.

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES						
	CAN		DUAL-IN-LINE				
	8-PIN	10-PIN	8-PIN	14-PIN	16-PIN	18-PIN	24-PIN
PB	—	—	FE	—	—	—	—
CB	—	—	—	F	—	—	—
EB	—	—	—	—	F	—	—
JB	—	—	—	—	—	—	F
DB	—	—	—	W	—	—	—
FB	—	—	—	—	W	—	—
ZC	—	—	—	—	—	—	Q
GC	H	—	—	—	—	—	—
IC	—	H	—	—	—	—	—
VB	—	—	—	—	—	I	—

All products listed are also available in Die form

Table 1 MILITARY PACKAGE AVAILABILITY

	JB	RB	RC
	Jan Qualified	883B	883C
54	X	X	X
54LS	X	X	X
54S	X	X	X
82	X	X	X
8T	—	X	X
93XX	X	X	X
96XX	—	X	X
Analog	X	X	X
Bipolar Memory	X	X	X
Microprocessor	—	X	X

Table 2 MILITARY SUMMARY

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets. Devices are selectively available as custom processed parts with electricals screened to the JAN Slash Sheets.

MIL-STD-883, LEVEL C

If you need a Military temp, range device, but do not require burn in screening performed, our 883C product is ideal. 883C parts are the standard full Mil-Temperature range product to the Signetics data sheet parameters and screened to MIL-STD-883, Class C.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity or running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily avail-

able before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

MILITARY PRODUCTS/PROCESS LEVELS

PROCESS LEVEL AND MARKETING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFFSHORE
JB JM38510XXXXX	2010, Cond. B	Yes	100%	100%	100%	Yes	No
RB SXXXX883B	2010, Cond. B	Yes	100%	100%	100%	No	Yes
RC SXXXX883C	2010, Cond. B	No	100%	100% dc Sample ac	Sample dc only	No	Yes

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

QUALIFIED	QUALIFIES	OPTION 1	OPTION 2
SUB-GROUPS			
A*	Electrical Test		
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*

Group A is performed on each lot or subplot of Signetics devices.

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

MILITARY PRODUCTS/PROCESS LEVELS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
General Mil-M-38510	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A
1. Pre-Certification						
A. Product Assurance Program Plan						
B. Manufacturer's Certification						
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A
4. Traceability	Traceability maintained back to a production lot Para. 3.4.6	—	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A
Screening Per Method 5004 of Mil-Std-883						
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C)	100%	X	X	X	X
8. Temperature Cycling*	1010, Cond. C; (10 cycles, -65°C to +150°C)	100%	X	X	X	X
*For Class B and C devices thermal shock may be substituted, 1011, Cond. A; (15 cycles, 0° to +100°C)						
9. Constant Acceleration	2001, Cond. E; (30kg in YI Plane)	100%	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X
11. Seal (Hermeticity)	1014					
A. Fine	Cond. A or B (5.0 X 10 ⁻⁶ CC/Sec)	100%	X	X	X	X
B. Gross	Cond. C2 Min.	100%	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100% Optional	100% Read & Record	Slash Sheet	Data Sheet	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X	X	N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1		X	X	X	X
B. Static Tests @ +125°C	Sub Group 2		X	X	X	N/A
C. Static Tests @ -55°C	Sub Group 3		X	X	X	N/A

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS

MILITARY PRODUCTS/PROCESS LEVELS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
D. Dynamic Test @25°C	Sub Group 4 (for Linear Product Mainly)		X	X	X	X
E. Functional Test @25°C	Sub Group 7		X	X	X	X
F. Switching Test @25°C	Sub Group 9		X	X	X	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @25°C (A-1). This is controlled by the slash sheets for JB products. For RB 10% is standard	10%	10% 3% Funct'l	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510/ XXXX Slash Sheet #	S X X X X 883B	SXXXX 883C
17. X-Ray	2012		100%	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std 883						
19. Group A	Electrical Tests-Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per pkg. group	X	X	Generic Data Available	
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constant acceleration.	Every 3 months per circuit type	X	X	Generic Data Available	
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available	

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Cont'd)

MILITARY SELECTION GUIDE

DEVICE	DESCRIPTION	PACKAGE		AVAILABILITY			QUAL STATUS
		DIP	CAN	883C	883B	83510/SHEET	
OPERATIONAL AMPLIFIERS							
LF155	Bi-FET Op Amp		H	X	X		
LF156	Bi-FET Op Amp		H	X	X		
LF156A	Bi-FET Op Amp		H		X		
LF198	Sample and Hold Amp		H		X		
LH2101A	Hybrid Dual Op Amp	F		X	X	10105	QPL1
LM101A	High Performance Op Amp	F, FE	H	X	X	10103	QPL1
LM124	Quad Op Amp	F		X	X		
LM158	Dual Op Amp		H	X	X		
MC1556	High Performance	F	H	X	X		
SE532	Dual Op Amp		H		X		
SE538	High Slew Rate Op Amp	F	H	X	X		
SE5512	Dual High Performance Op Amp	F			X		
SE5532	Dual Low Noise Op Amp	FE		X	X		
SE5532A	Dual Low Noise Op Amp	FE		X	X		
SE5534	Low Noise Op Amp	FE	H	X	X		
SE5534A	Low Noise Op Amp	FE	H	X	X		
SE5539	Very High Slew Rate Op Amp	F		X	X		
μA741	General Purpose Op Amp		H			10101	QPL1
μA747	Dual Op Amp	F	H	X	X	10102	QPL1
VIDEO AMPS							
μA733	Differential Video Amplifier	F	H	X	X		
SE511	Dual Differential Amplifier	F			X		
INTERFACE							
DS7820/A	Dual Line Receiver	F		X	X		
DATA CONVERSION							
DAC-08/A	8-Bit D/A Converter	F			X		
MC1508-8	8-Bit D/A Converter	F		X	X		
SE5008	8-Bit D/A Converter	F			X		
SE5009	8-Bit D/A Converter	F			X		
SE5018	8-Bit μP-Compatible D/A Converter	F			X		
SE5019	8-Bit μP-Compatible D/A Converter	F			X		
SE5118	8-Bit DAC Current Output	F		X	X		
SE5119	8-Bit DAC Current Output	F		X	X		
SAMPLE AND HOLD CIRCUITS							
SE5537	Precision Sample and Hold Amplifier		H	X	X		
LF198	Sample and Hold Amplifier		H		X		
PHASE-LOCKED LOOPS							
SE567	Phase-Locked Loop Tone Decoder	F	H	X	X		

MILITARY SELECTION GUIDE

DEVICE	DESCRIPTION	PACKAGE		AVAILABILITY			QUAL STATUS
		DIP	CAN	883C	883B	83510/SHEET	
POWER CONTROLLERS							
SE5560	SMPS Control Circuit	F			X		
SG1524	SMPS Control Circuit	F			X		
SE5551	Dual Polarity Regulator	F			X		
SE5552	Dual Polarity Regulator	F			X		
SE5553	Dual Polarity Regulator	F			X		
SE5554	Dual Polarity Regulator	F			X		
SE5555	Dual Polarity Regulator	F			X		
TIMERS							
SE555	Timer	F, FE	H	X	X	10901	QPL1
SE556-1	Dual Timer	F		X	X	10902	QPL1
SE558	Quad Timer	F			X		
COMPARATORS							
SE521	High-Speed Dual Differential Comparator	F		X	X		
SE522	High-Speed Dual Differential Comparator	F		X	X		
SE527	Voltage Comparator	F	H	X	X		
SE529	Voltage Comparator	F	H	X	X		
LH2111	Hybrid Dual Comparator	F		X	X		
LM111	Voltage Comparator	F	H	X	X		
LM139/A	Quad Comparator	F			X		
LM193/A	Dual Comparator	F			X		
LM119	Dual Voltage Comparator	F	H		X		

MILITARY CROSS REFERENCE

FAIRCHILD	SIGNETICS
μ A111	LM111
μ A139	LM139
μ A733	μ A733
μ AF155/156	LF155/156
μ A101	LM101
μ A101A	LM101A
MC1556	MC1556
μ A1558	MC1558
μ A747	μ A747
MC1555	SE555
μ A556	SE556
μ A723	μ A723

MOTOROLA	SIGNETICS
MLM111	LM111
MC1733	μ A733
LF155/56	LF155/156
MLM101	LM101
MLM101A	LM101A
MC1558	MC1558
MC1747	μ A747
MC3556	SE556
MC1723	μ A723
MC1508	MC1508-8

NATIONAL	SIGNETICS
LM161	SE527
LH2111	LH2111
LM111	LM111
LM119	LM119
LM139	LM139
LM193	LM193/193A
LM733	μ A733
LF155/56	LF155/156
LH2101A	LH2101A
LH2108A	LH2108A
LM101A	LM101
LM101	LM101A
LM124	LM124
LM158	LM158
LM1558	MC1558
LM1581	SE532
LM747	μ A747
LM567	SE567
DM7820	DM7820
DM7830	DM7830
LM555	SE555
LM723	μ A723

PMI	SIGNETICS
SSS1508	MC1508-8
DAC-08	SE5008

RAYTHEON	SIGNETICS
LM111	LM111
LM139	LM139
RM733	μ A733
LF155/56/57	LF155/156
LM101	LM101
LM101A	LM101A
LM124	LM124
RM1556	MC1556
RM1558	MC1558
RM747	μ A747
RM555	SE555
RM723	μ A723

T.I.	SIGNETICS
LM111	LM111
SN52733	μ A733
LF155/56	LF155/156
SN52101A	LM101A
SN55182	DM7820
SN55183	DM7830
SN52555	SE555
SE556	SE556
SN52723	μ A723

Section 18 Appendices

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Section 18 — Appendices

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PACKAGE OUTLINES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
 - a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

PLASTIC ONLY

5. Lead material: Alloy 42 (Nickel/Iron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO Packages-microminiature packages.
 - a. Lead material: Alloy-42.
 - b. Body material: Plastic (Epoxy).

HERMETIC ONLY

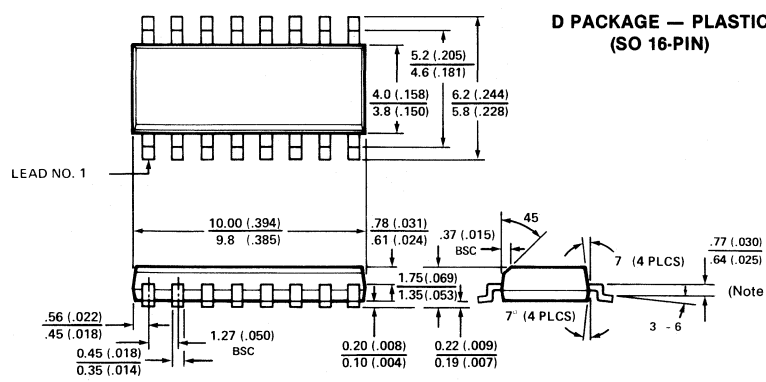
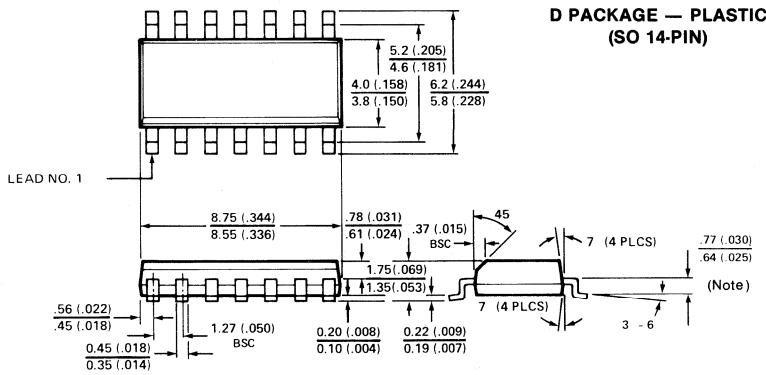
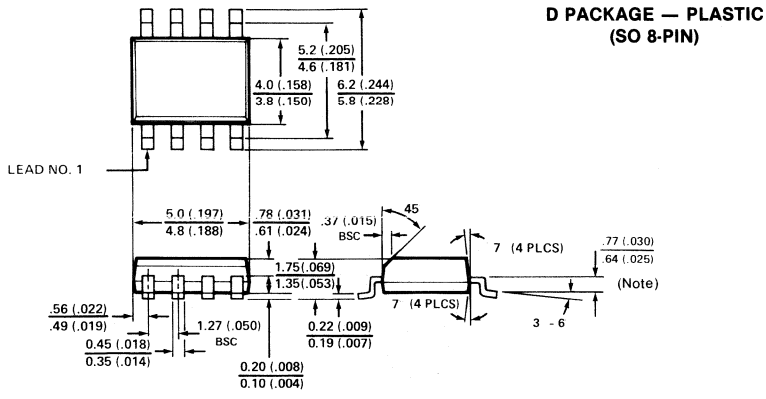
10. Lead material
 - a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
 - b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated or solder dipped.
 - c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
11. Body Material
 - a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.

- b. Ceramic with glass seal at leads.
 - c. BeO ceramic with glass seal at leads.
 - d. Ceramic with ASTM alloy F-30 or equivalent.
12. Lid Material
 - a. Nickel or tin plated nickel, weld seal.
 - b. Ceramic, glass seal.
 - c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
 - d. BeO Ceramic with glass seal.
 13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
 14. Recommended minimum offset before lead bend.
 15. Maximum glass climb .010 inches.
 16. Maximum glass climb or lid skew is .010 inches.
 17. Typical four places.
 18. Dimension also applies to seating plane.

PACKAGE OUTLINES

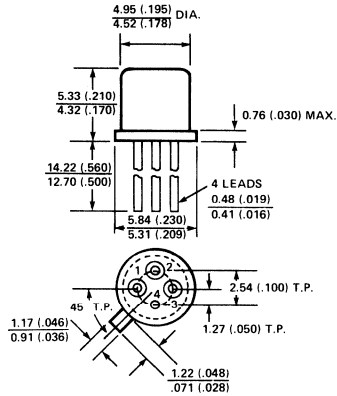
PLASTIC PACKAGES			
PACKAGE CODE		$\theta_{j\alpha}/\theta_{jc} (^{\circ}\text{C}/\text{W})$	DESCRIPTION
SO Packages			
8-Pin	D	110	SO-8
14-Pin	D	100	SO-14
16-Pin	D	100	SO-16
Standard Dual-In-Line			
8-Pin	N	162/65	
14-Pin	N	150/65	TO-116/MO-001
16-Pin	N	137/53	MO-001
18-Pin	N	135/53	
20-Pin	N	135/53	
22-Pin	N	120/53	
24-Pin	N	116/53	MO-015
28-Pin	N	116/53	MO-015
Power Dual-In-Line			
14-Pin	N	95/33	Butterfly
16-Pin	N	95/33	Butterfly
18-Pin	N	90/26	Butterfly
20-Pin	N	90/26	Butterfly
24-Pin	N	60/23	Heatsink
28-Pin	N	56/21	Heatsink
Metal Headers			
3-Pin	H	100/20	TO-5 Header
4-Pin	E	100/20	TO-46 Header
4-Pin	E	150/25	TO-72 Header
8-Pin	H	150/25	TO-5 Header
10-Pin	H	150/25	TO 5/TO-100 Header, Short Can
10-Pin	H	150/25	TO-5/TO-100 Header, Tall Can
Flat Packs			
10-Pin	W	240/50	Flat Ceramic
16-Pin	W	200/50	Flat Ceramic
Cerdip Family			
8-Pin	FE	110/30	Dual-in-Line Ceramic
14-Pin	F	110/30	Dual-in-Line Ceramic
16-Pin	F	100/30	Dual-in-Line Ceramic
18-Pin	F	93/27	Dual-in-Line Ceramic
20-Pin	F	90/25	Dual-in-Line Ceramic
22-Pin	F	75/27	Dual-in-Line Ceramic
24-Pin	F	60/26	Dual-in-Line Ceramic
28-Pin	F	57/27	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
14-Pin	I	95/25	Dip Laminate
16-Pin	I	90/25	Dip Laminate
28-Pin	I	60/25	Dip Laminate

PACKAGE OUTLINES

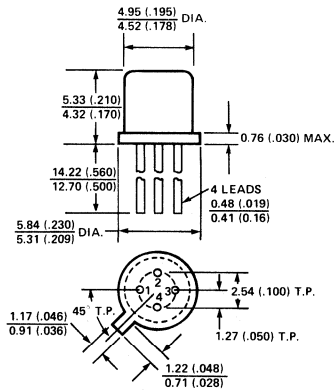


PACKAGE OUTLINES

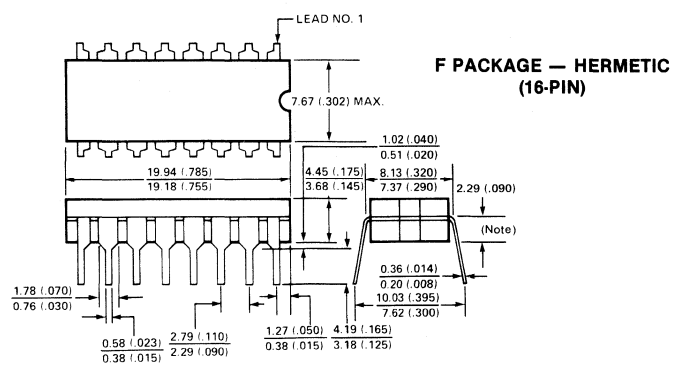
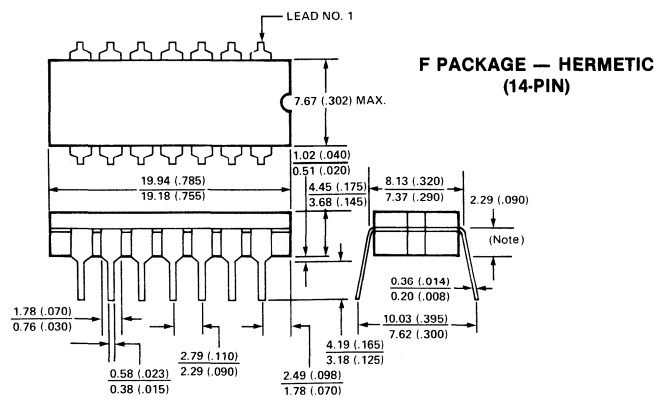
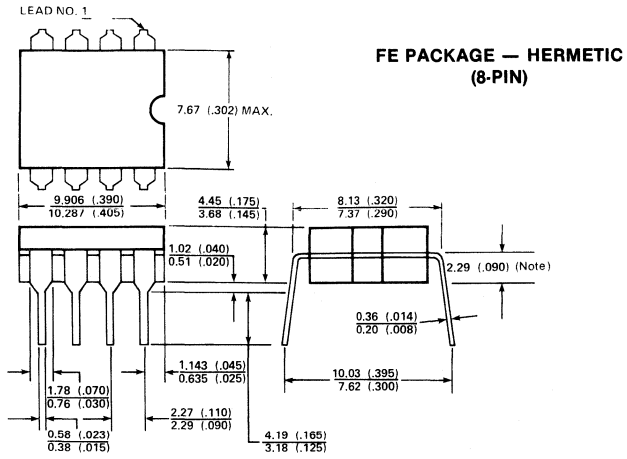
E PACKAGE — HERMETIC (TO-46 HEADER)



E PACKAGE — HERMETIC (TO-72 HEADER)

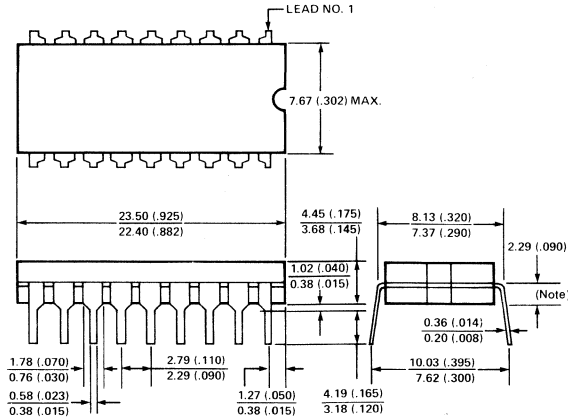


PACKAGE OUTLINES

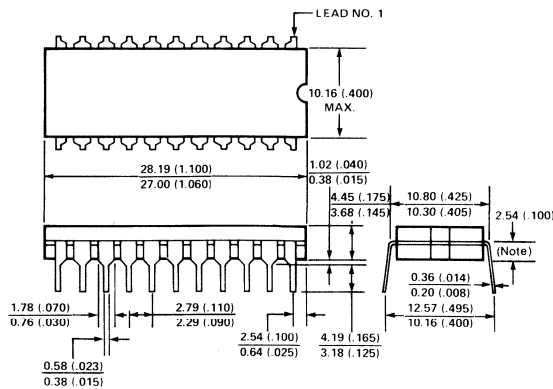


PACKAGE OUTLINES

F PACKAGE — HERMETIC (18-PIN)

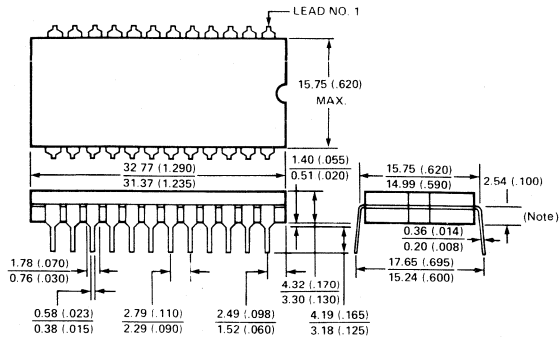


F PACKAGE — HERMETIC (22-PIN)

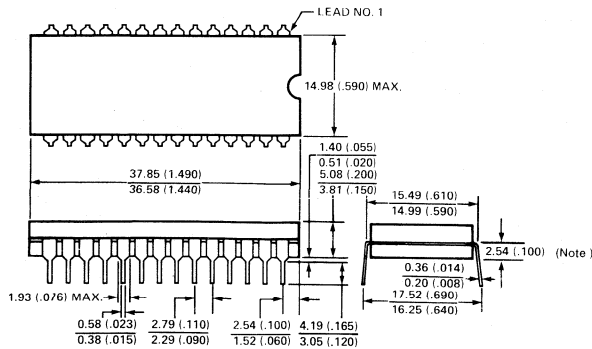


PACKAGE OUTLINES

F PACKAGE — HERMETIC (24-PIN)

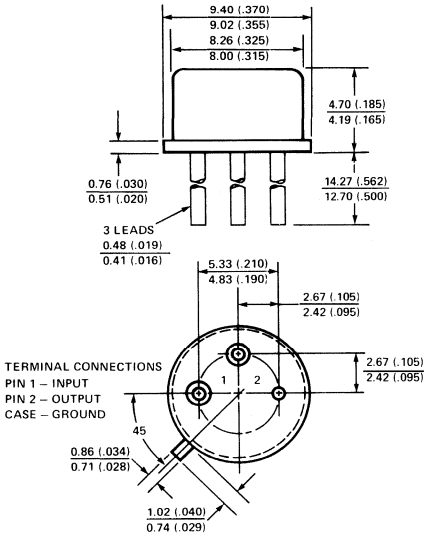


F PACKAGE — HERMETIC (28-PIN)

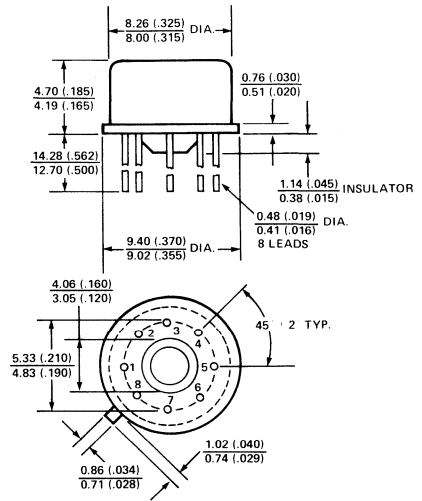


PACKAGE OUTLINES

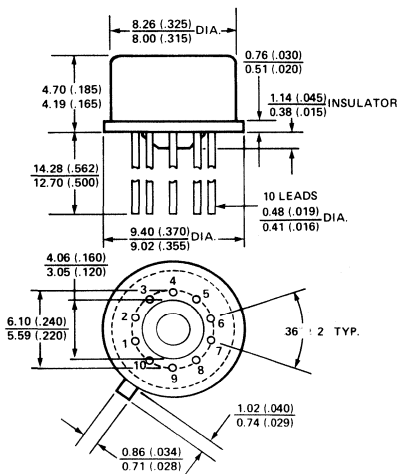
**H PACKAGE — HERMETIC
3-PIN
(TO-5 HEADER)**



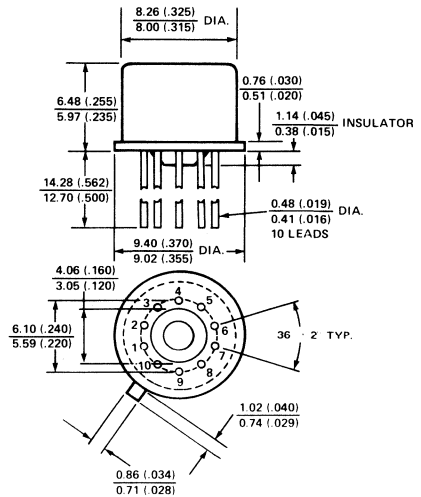
**H PACKAGE — HERMETIC
8-PIN
(TO-5 HEADER)**



**H PACKAGE — HERMETIC
10-PIN
(TO-5/100 HEADER
SHORT CAN)**

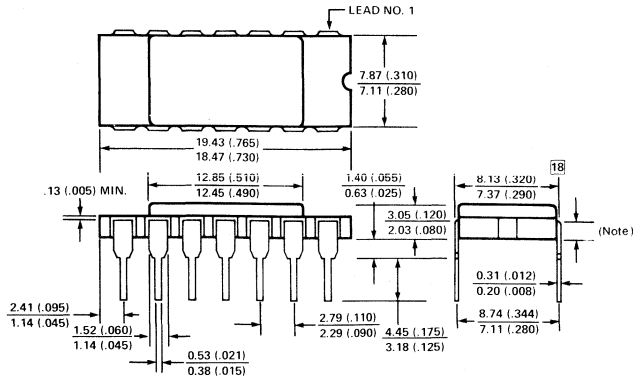


**H PACKAGE HERMETIC
10-PIN
(TO-5/100 HEADER
TALL CAN)**

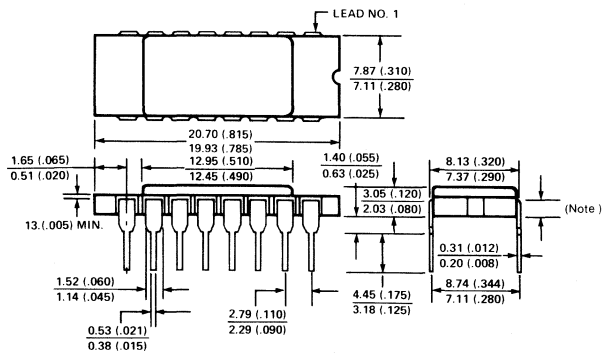


PACKAGE OUTLINES

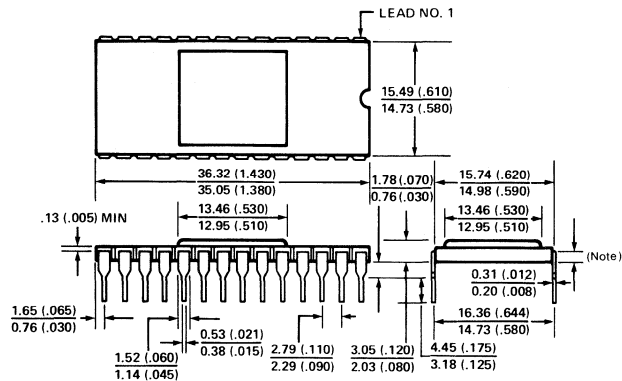
**I PACKAGE — HERMETIC
(14-PIN)**



**I PACKAGE — HERMETIC
(16-PIN)**

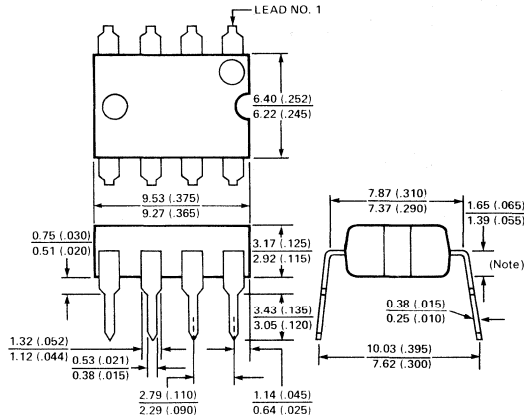


**I PACKAGE — HERMETIC
(28-PIN)**

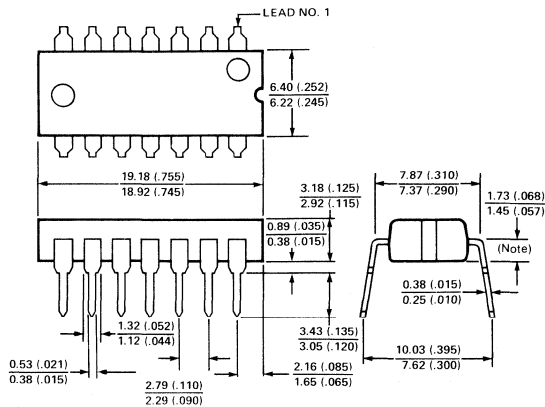


PACKAGE OUTLINES

N PACKAGE — PLASTIC (8-PIN)

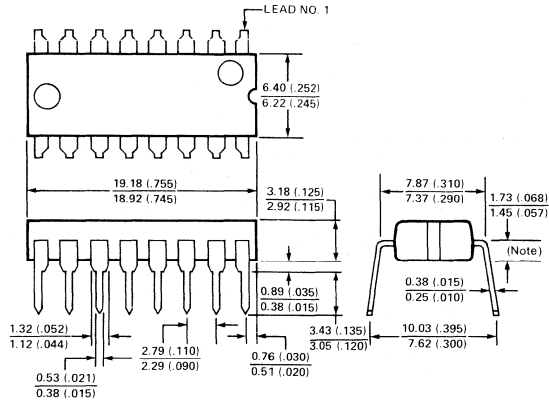


N PACKAGE — PLASTIC (14-PIN)

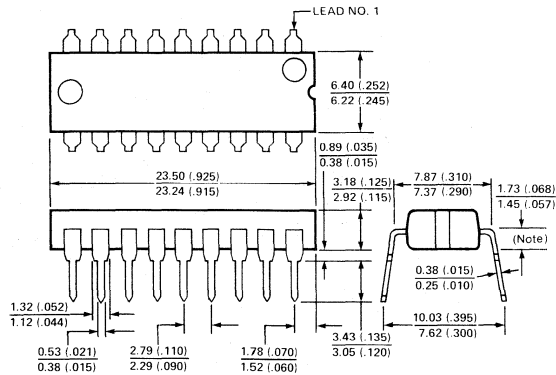


PACKAGE OUTLINES

N PACKAGE — PLASTIC (16-PIN)

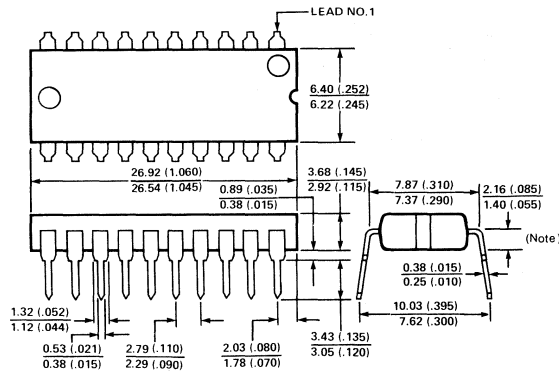


N PACKAGE — PLASTIC (18-PIN)

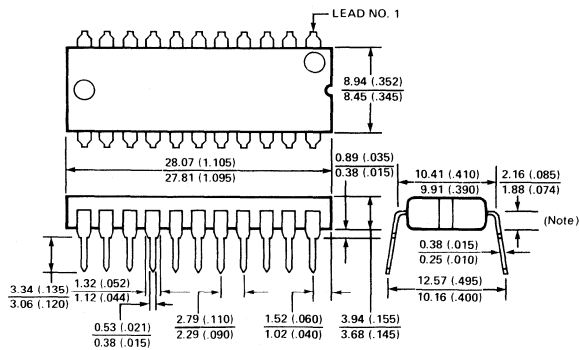


PACKAGE OUTLINES

N PACKAGE — PLASTIC (20-PIN)

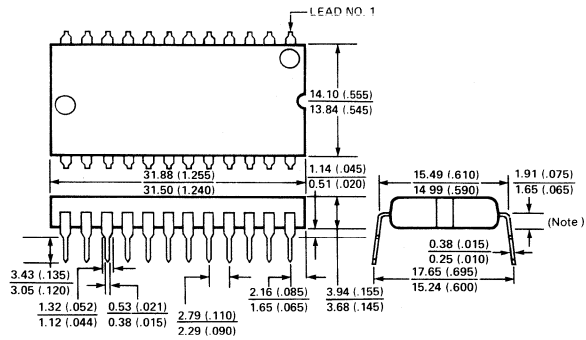


N PACKAGE — PLASTIC (22-PIN)

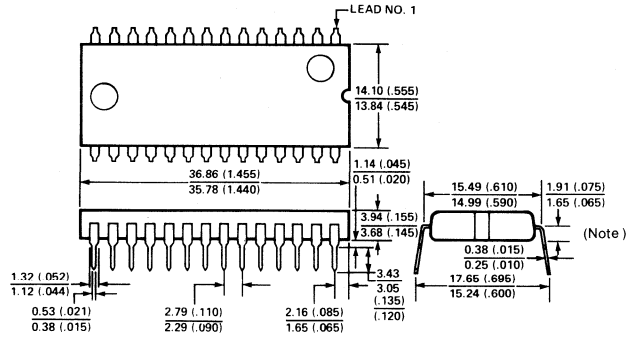


PACKAGE OUTLINES

**N PACKAGE — PLASTIC
(24-PIN)**

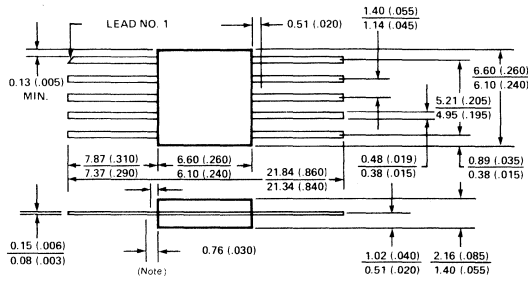


**N PACKAGE — PLASTIC
(28-PIN)**

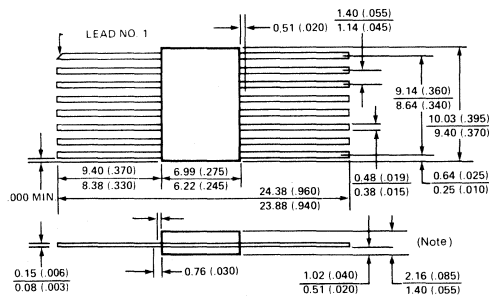


PACKAGE OUTLINES

**W PACKAGE — HERMETIC
(10-PIN)**



**W PACKAGE — HERMETIC
(16-PIN)**



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Venezuela: IND. VENEZOLANAS PHILIPS S.A., Elcoma Dept., A. Ppal de los Ruices, Edif. Centro Colgate, CARACAS, Tel. 36 05 11.

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Integrated circuits

Part 7

August 1982

Signetics Bipolar memories

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Bipolar Memory Data Manual 1982

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PREFACE

Rapid improvement in both the cost and performance of semiconductor memories has led to a dramatic increase in their usage in today's highly sophisticated electronic systems. Signetics has worked diligently over the last 20 years to develop the various technologies necessary to satisfy the broad range of users' semiconductor requirements. As a result, Signetics is able to offer a very broad, high performance bipolar memory product line.

Signetics offers a complete line of bipolar Schottky PROMs, Integrated Fuse Logic, and RAMs for many high-speed applications. These products are available with organizations ranging from 64 to 2K bits for the RAM family, 256 to 32K bits for the PROM family and $18 \times 32 \times 10$ for the IFL family. All Signetics' bipolar products are fabricated with double level metallization for maximum packaging density and low cost. Signetics will continue to advance bipolar memory "state of the art" in future years, through the introduction of new special purpose PROMs and state-of-the-art Integrated Fuse Logic.

The 1982 Signetics Memory Data Manual contains data on currently available PROM and RAM products and some products which are planned for the immediate future. For information on the Integrated Fuseable Logic family, refer to the Signetics IFL Manual. In addition, a product selection guide is included to aid the user in quickly selecting the optimum product for his particular system application.

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ORDERING INFORMATION

ORDERING INFORMATION

Signetics Bipolar Memory integrated circuit products may be ordered by contacting either the local Signetics sales office, Signetics representatives and/or Signetics authorized distributors. A complete listing is located in the back of this manual.

The table shown provides part number

definition for Signetics memory products. The Signetics part number system allows complete definition for ordering a device. The part number itself and the product description is defined on each data sheet. The suffix is a single letter defining a package type (as shown in the table on this page). Additional or special process-

ing is defined by adding the processing indicator when required.

The military qualification, Full MIL Signetics or Full JAN slash sheet status, can be determined by referring to the military section of this manual. Verification of the military status can be made by contacting your local Signetics sales office.

Table 1 PART NUMBER DESCRIPTION

The diagram illustrates the structure of a Signetics part number. It shows three examples: 82S181, 82HS137A, and 82S191. Each example is broken down into its constituent parts: PREFIX (N or S), PART NUMBER (82, HS, or S), and SUFFIX (F, N, or I). The suffix 'N' is further broken down into 'N' and 'B', which are linked to the '883B' processing indicator. Arrows indicate the mapping from the part number components to the tables below.

USED TO DEFINE OPERATING TEMPERATURE RANGE	
PREFIX	DEVICE TEMPERATURE RANGE
N	0°C to +75°C
S	-55°C to +125°C

USED TO DEFINE PART ITSELF	
----------------------------	--

USED TO DEFINE PACKAGE TYPE	
PACKAGE CODE	PACKAGE DESCRIPTION
F	16, 18, 20, 22, 24, 28-Lead DIL CERDIP
I	18, 24, 28-Lead DIL CERAMIC
G	20, 28-Lead Square Leadless
R	16, 18, 24, 28-Lead CERAMIC-Beryllia Flat Pack
N	16, 18, 20, 22, 24, 28-Lead DIL PLASTIC
W	16-Lead CERPAC

PROCESSING INDICATOR		
MILITARY		
883C		Full MIL-STD-883 Class C Processing
883B		Full MIL-STD-883 Class B Processing including 168 hrs. Burn-In
Commercial		
A	SUPR II A	Tightened AQLs
B	SUPR II B	Tightened AQLs with Operating High Temp. Burn-In

PRODUCT STATUS DEFINITIONS

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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10415B	1024-Bit ECL RAM (1024 × 1)	6-1
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10470A	4096-Bit ECL RAM (4096 × 1)	6-7
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BIPOlar MEMORY SELECTION GUIDE

BIPOlar MEMORY SELECTION GUIDE

DEVICE	ORG	OUTPUT CKT ¹	OUTPUT LOGIC ²	ACCESS TIME ⁴	TEMP ³	PKG	PINS	MAX I _{cc} ⁴
CAMs								
10155	8 × 2	OE	—	13	C	F, N	18	140
RAMs								
3101A	16 × 4	OC	B	35	M, C	F, N	16	105
54/74S189	16 × 4	TS	B	35	M, C	F, N	16	110
82S21	32 × 2	OC	T	50	C	F, N	16	130
82S16	256 × 1	TS	T	50	M, C	F, N	16	115
82S17	256 × 1	OC	T	50	M, C	F, N	16	115
74S301	256 × 1	OC	B	50	M, C	F, N	16	115
82LS16	256 × 1	TS	T	40	M, C	F, N	16	70
82LS17	256 × 1	OC	T	40	M, C	F, N	16	70
74LS301	256 × 1	OC	B	40	M, C	F, N	16	70
82S09	64 × 9	OC	T	45	M, C	I, N	28	190
82S19	64 × 9	OC	B	35	M, C	I, N	28	190
82S210	256 × 9	TS	B	60	M, C	F, N	24	185
82S212	256 × 9	TS	B	45	M, C	F, N	22	185
8X350	256 × 8	TS	B	N/A	M, C	F, N	22	185
10415	1024 × 1	OE	B	20	C	F	16	150
10415A	1024 × 1	OE	B	15	C	F	16	150
10415B	1024 × 1	OE	B	10	C	F	16	150
100415	1024 × 1	OE	B	20	C	F	16	150
100415A	1024 × 1	OE	B	15	C	F	16	150
100415B	1024 × 1	OE	B	10	C	F	16	150
10422	256 × 4	OE	B	20	C	F	24	195
10422A	256 × 4	OE	B	15	C	F	24	195
10422B	256 × 4	OE	B	10	C	F	24	195
100422	256 × 4	OE	B	20	C	F	24	195
100422A	256 × 4	OE	B	15	C	F	24	195
100422B	256 × 4	OE	B	10	C	F	24	195
10470*	4096 × 1	OE	B	30	C	F	18	150
10470A*	4096 × 1	OE	B	20	C	F	18	150
100470*	4096 × 1	OE	B	30	C	F	18	150
100470A*	4096 × 1	OE	B	20	C	F	18	150
10474*	1024 × 4	OE	B	35	C	F	24	195
10474A*	1024 × 4	OE	B	25	C	F	24	195
100474*	1024 × 4	OE	B	35	C	F	24	195
100474A*	1024 × 4	OE	B	25	C	F	24	195
FPLAs								
82S100	16 × 48 × 8	TS	—	50	M, C	F, N	28	170
82S101	16 × 48 × 8	OC	—	50	M, C	F, N	28	170
82S152	18 × 32 × 10	OC	I/O	40	M, C	F, N	20	155
82S153	18 × 32 × 10	TS	I/O	40	M, C	F, N	20	155
FPGAs								
82S150*	18 × 12	OC	I/O	20	M, C	F, N	20	155
82S151*	18 × 12	TS	I/O	20	M, C	F, N	20	155
82S102	16 × 9	OC	—	35	M, C	F, N	28	170
82S103	16 × 9	TS	—	35	M, C	F, N	28	170
FPLSs								
82S104	16 × 48 × 8	OC	R	60	M, C	F, N	28	180
82S105	16 × 48 × 8	TS	R	60	M, C	F, N	28	180
82S154*	16 × 32 × 12	OC	I/O, R	65	M, C	F, N	20	155
82S155*	16 × 32 × 12	TS	I/O, R	65	M, C	F, N	20	155
82S156*	16 × 32 × 12	OC	I/O, R	65	M, C	F, N	20	155
82S157*	16 × 32 × 12	TS	I/O, R	65	M, C	F, N	20	155
82S158	16 × 32 × 12	OC	I/O, R	65	M, C	F, N	20	155
82S159	16 × 32 × 12	TS	I/O, R	65	M, C	F, N	20	155

BIPOLAR MEMORY SELECTION GUIDE

BIPOLAR MEMORY SELECTION GUIDE (Continued)

DEVICE	ORG	OUTPUT CKT ¹	OUTPUT LOGIC ²	ACCESS TIME ⁴	TEMP ³	PKG	PINS	MAX I _{CC} ⁴
PROMs								
82S23	32 × 8	OC	—	50	M, C	F, N	16	77
82S123	32 × 8	TS	—	50	M, C	F, N	16	77
82S126	256 × 4	OC	—	50	M, C	F, N	16	120
82S129	256 × 4	TS	—	50	M, C	F, N	16	120
10149	256 × 4	OE	—	20	C	F	16	160
100149	256 × 4	OE	—	20	C	F	16	180
82S130	512 × 4	OC	—	50	M, C	F, N	16	140
82S131	512 × 4	TS	—	50	M, C	F, N	16	140
82S115	512 × 8	TS	—	60	M, C	F, N	24	175
82S140	512 × 8	OC	—	60	M, C	F, N	24	175
82S141	512 × 8	TS	—	60	M, C	F, N	24	175
82S137	1024 × 4	TS	—	60	M, C	F, N	18	140
82HS137	1024 × 4	TS	—	45	M, C	F, N	18	140
82HS137A	1024 × 4	TS	—	35	C	F, N	18	140
82S147	512 × 8	TS	—	60	M, C	F, N	20	155
82HS147	512 × 8	TS	—	45	M, C	F, N	20	155
82LS181	1024 × 8	TS	—	120	M, C	F, N	24	80
82S180	1024 × 8	OC	—	70	M, C	F, N	24	175
82S181	1024 × 8	TS	—	70	M, C	F, N	24	175
82HS181	1024 × 8	TS	—	55	M, C	F, N	24	175
82HS181A	1024 × 8	TS	—	45	C	F, N	24	175
82S183	1024 × 8	TS	—	60	M, C	F, N	24	175
82S2708	1024 × 8	TS	—	70	M	F	24	175
82S185	2048 × 4	TS	—	100	M, C	I, N	18	120
82HS185	2048 × 4	TS	—	50	M, C	F, N	18	155
82HS185A	2048 × 4	TS	—	45	C	F, N	18	155
82S191	2048 × 8	TS	—	80	M, C	F, N	24	175
82HS191	2048 × 8	TS	—	60	M, C	F, N	24	175
82HS195*	4096 × 4	TS	—	35	M, C	F, N	20	155
82S321*	4096 × 8	TS	—	80	C	F, N	24	175

*To be announced.

NOTES

1. Output circuit:

OE = Open emitter
 OC = Open collector
 TS = 3-state

2. Output logic:

T = Transparent — input data appears on output during Write
 B = Blanked — output is blanked during Write
 R = Output logic
 I/O = Input/output option

3. Temperature range:

C = Commercial (0°C to +75°C)
 M = Military (-55°C to +125°C)

4. Commercial (0°C to +75°C)

BIPOLAR MEMORY CROSS REFERENCE

BIPOLAR MEMORY CROSS REFERENCE

AMD	SIGNETICS
Am27S18C	N82S23
AM27S19C	N82S123
AM27S20C	N82S126
AM27S21C	N82S129
AM27S12C	N82S130
AM27S13C	N82S131
AM27S33C	N82S137
	N82HS137
AM27S29C	N82S147
	N82HS147
AM27S31C	N82S141
AM27S15C	N82S115
AM27S180C	N82S180
AM27S181C	N82S181
	N82HS181
AM27S185C	N82S185
	N82HS185
AM27S191C	N82S191
	N82HS191
AM27S41C	N82HS195
2702/3101A	N3101A
54S289	N82S25
2700	N82S16
27LS01	N82LS16
2701	N82S17

NATIONAL	SIGNETICS
DM74S188	N82S23
DM74S288	N82S123
DM74S387	N82S126
DM74S287	N82S129
DM74S570, A	N82S130
DM74S571, A	N82S131
DM74S573, A	N82S137
	N82HS137
DM74S472	N82S147
	N82HS147
DM74S574, A	N82S141
DM87S180	N82S180
DM87S181	N82S181
	N82HS181
DM87S185	N82S185
	N82HS185
DM87S191	N82S191
	N82HS191
74S189	74S189
74S289	N82S25
74S200	N82S16
74S206	N82LS16
DM10422	10422
DM100422	100422
DM10415	10415
DM10470	10470
DM100470	100470

INTEL	SIGNETICS
3601	N82S126
3621	N82S129
3602	N82S130
3622	N82S131
3625	N82S137
	N82HS137
3624	N82S141
3628	N82S181
	N82HS181
3636	N82S191
3636A	N82HS191
3632	N82S321
3632-1	
3101A	N3101A
3101	N82S25
3106	N82S16
3107	N82S17

HARRIS	SIGNETICS
HM7602-5	N82S23
HM7603-5	N82S123
HM7610-5	N82S126
HM7611-5	N82S129
HM7620-5	N82S130
HM7621-5	N82S131
HM7643-5	N82S137
	N82HS137
HM7649-5	N82S147
	N82HS147
HM7641-5	N82S141
HM7647R-5	N82S115
HM7680-5	N82S180
HM7681-5	N82S181
	N82HS181
HM7681P-5	N82PS181
HM7681R-5	N82S183
HM7608-5	N82S2708
HM7685-5	N82S185
	N82HS185
HM76161-5	N82S191
	N82HS191
HM76165-2/8	N82HS195

FAIRCHILD	SIGNETICS
9341C	N82S126
10416	10149
93427C	N82S129
100416	100149
93436C	N82S130
93446C	N82S131
93453C	82S137
	N82HS137
9344C	N82S141
93450C	N82S180
93451C	N82S181
	N82HS181
93L451C	N82LS181
93461C	N82S2708
93515C	N82S185
	N82HS185
93511C	N82S191
	N82HS191
93513C	N82HS195

MMI	SIGNETICS
6330-1	N82S23
6331-1	N82S123
6000-1	N82S126
6301-1	N82S129
6305-1	N82S130
6306-1	N82S131
6353-1	N82S137
	N82HS137
6349-1	N82S147
	N82HS147
6341-1	N82S141
6380-1	N82S180
6381-1	N82S181
	N82HS181
6560	N3101A
6561	74S189
6560	N82S25
6555	N82S09
6531	N82S16
6530	N82S17

INTERSIL	SIGNETICS
IM5600C	N82S23
IM5610C	N82S123
IM5603C	N82S126
IM5623C	N82S129
IM5604C	N82S130
IM5624C	N82S131
5501	N82S25
5523A	N82S16
5533A	N82S17

1

BIPOLAR MEMORY CROSS REFERENCE

BIPOLAR MEMORY CROSS REFERENCE (Continued)

MOTOROLA	SIGNETICS	T.I.	SIGNETICS	RAYTHEON	SIGNETICS
MCM10149	*10149	TBP18SA030J, N	N82S23	29661C	N82S129
MCM7620	N82S130	TBP24SA10J, N	N82S123	29610C	N82S130
MCM7621	N82S131	TBP24SA10J, N	N82S126	29611C	N82S131
MCM7643C	N82S137	TBP14S10J, N	N82S129	29641C	N82S137
	N82HS137	TBP24S41J, N	N82S137		N82HS137
MCM7641C	N82S141		N82HS137	29625C	N82S141
MCM7681C	N82S181	TBP28S42	N82S147	29631AC	N82S181
	N82HS181		N82HS147		N82HS181
MCM82708C	N82S2708	TBP28S46J, N	N82S141	29633AC	N82PS181
MCM7685C	N82S185	TBP28SA86J, N	N82S180	29635C	N82S2708
	N82HS185	TBP28S86J, N	N82S181	29651AC	N82S185
4064	N82S25		N82HS181		N82HS185
4256	N82S16	TBP28P85	N82PS181	29681AC	N82S191
10422	10422	TBP28P86	N82LS181		N82HS191
10470	10470	TBP28S2708J, N	N82S2708		
		TBP24S81J, N	N82S185		
			N82HS185		
		TBP28S166J, N	N82S191		
			N82HS191		
		74S289	N3101A		
		74S289	N82S25*		
		74S301	N74S301		
		74S200	N82S16		

Section 2
RAMs,
Special Purpose

16-BIT ECL CAM (8 × 2)

10155

DESCRIPTION

The 10155 is a 16-bit ECL Content Addressable Memory (CAM) organized as an array of 8 words by 2 bits. Each cell of the array consists of a D-type latch and an exclusive-OR comparator, along with control logic for reading, writing and masking.

The modes of operation possible with the 10155 are associate, masked associate, read, write, and hybrid. Lines Y_0 - Y_7 are used for linear word select in the read/write mode, and are used as outputs for match/mismatch information in the associate mode.

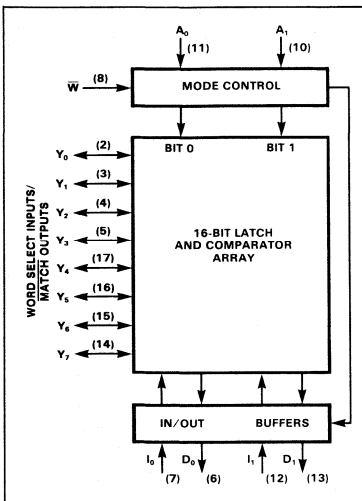
In associate operation, I_0 and I_1 contain information to be compared. If the latches at a particular Y location are in a state matching the input data, that Y line goes low.

The Y outputs are open emitters, allowing expansion in multiples of 2 bits by tying additional 10155's to the Y bus lines. To inhibit comparison of a particular bit, the corresponding A_0 or A_1 line is held low.

In the read mode, the state of the selected cells appears on outputs D_0 and D_1 . In the write mode, these outputs are transparent, following the state of I_0 and I_1 .

In Hybrid mode, one of the I_0 or I_1 data inputs may be associated with the Q_{n0} or Q_{n1} cells respectively. If a match exists, the corresponding Y_n line(s) will go low, and can be used to address the other half of the memory for writing new data. Thus, it is possible to write I_1 in Q_{n1} where I_0 matches Q_{n0} or vice versa.

BLOCK DIAGRAM



FEATURES

- 12ns associate time (max.)
- Linear address select
- Single bit masking
- 50 Ω output drive
- ECL 10K compatible
- Open emitter match lines for easy bit expansion
- 50k Ω input pulldown resistors (except on Y lines)

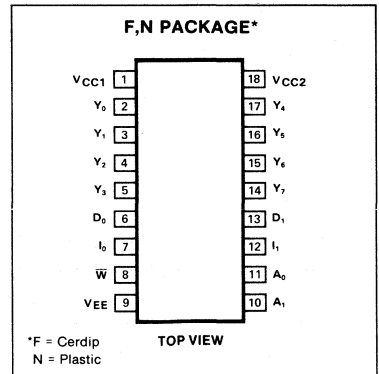
APPLICATION

- Content addressable memory systems

RECOMMENDED OPERATING VOLTAGES

- $V_{CC1} = V_{CC2} = 0V$
- $V_{EE} = -5.2V \pm 5\%$

PIN CONFIGURATION



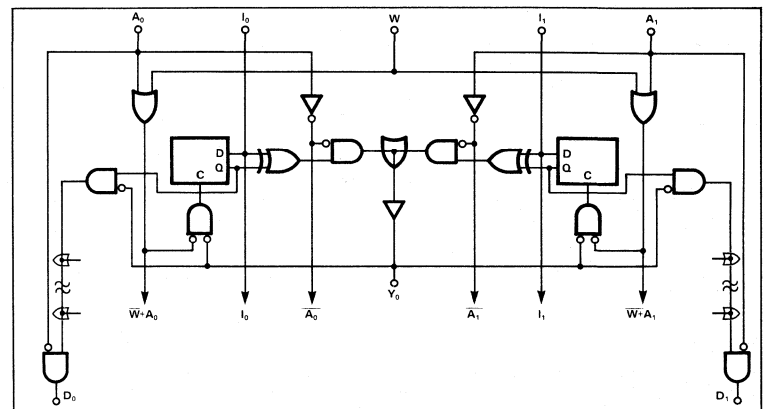
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TRUTH TABLE (POSITIVE LOGIC)

MODE	A_0	A_1	I_0	I_1	\bar{W}	D_0	D_1	Q_{n0}	Q_{n1}	Y_n
Associate ¹	1	1	1/0	1/0	X	0	0	Q_{n0}	Q_{n1}	$Q_{n0} \oplus I_0 + Q_{n1} \oplus I_1$
Associate ^{1,2} (masked)	1	0	1/0	X	1	0	D_1	Q_{n0}	Q_{n1}	$Q_{n0} \oplus I_0$
Associate ^{1,2} (masked)	0	1	X	1/0	1	D_0	0	Q_{n0}	Q_{n1}	$Q_{n1} \oplus I_1$
Read ³	0	0	X	X	1	D_0^2	D_1^2	Q_{n0}	Q_{n1}	0 (Selected address)
Write ^{3,4}	0	0	1/0	1/0	0	I_0	I_1	I_0	I_1	0 (Selected address)
Hybrid ⁵	1	0	1/0	1/0	0	0	I_1	Q_{n0}	$I_1 \cdot \bar{Y}_n$	$Q_{n0} \oplus I_0$
Hybrid ⁵	0	1	1/0	1/0	0	I_1	0	$I_0 \cdot \bar{Y}_n$	Q_{n1}	$Q_{n1} \oplus I_1$

- X = Don't care
 Q_{n0} = Contents of address n, Bit 0 (n = 0 to 7)
 Q_{n1} = Contents of address n, Bit 1
- NOTES
1. 1 (high) = Mismatch, 0 (low) = Match
 2. Read mode: $D_0 = Q_{00} \cdot Y_0 + Q_{10} \cdot Y_1 + \dots + Q_{70} \cdot Y_7$
 $D_1 = Q_{01} \cdot Y_0 + Q_{11} \cdot Y_1 + \dots + Q_{71} \cdot Y_7$
 3. In normal operation a single Y address is selected for read or write
 4. Write is transparent
 5. Simultaneous Associate and Write at all "Match" addresses.

LOGIC DIAGRAM (TYPICAL BIT)



16-BIT ECL CAM (8 × 2)

10155

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2} = 0V$

PARAMETER	RATING	UNIT
V _{EE} Supply voltage	-8	Vdc
V _{IN} Input voltage	0 to V _{EE}	Vdc
I _O Output source current	40	mAdc
Temperature Range		°C
T _A Operating	-30 to +85	
T _J Operating junction	125	
T _{STG} Storage	-55 to +125	

DC ELECTRICAL CHARACTERISTICS¹ $V_{CC1} = V_{CC2} = 0V, V_{EE} = -5.2V, R_L = 50\Omega$ to -2V

PARAMETER	TEST CONDITIONS	-30 °C			+25 °C			+85 °C			UNIT
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input voltage V _{IL} Low V _{IH} High V _{ILA} Low threshold V _{IHA} High threshold		-1.890			-1.850			-1.825			V
				-0.890			-0.810			-0.700	
				-1.500			-1.475			-1.440	
			-1.205			-1.105			-1.035		
Output voltage V _{OL} Low V _{OH} High	V _{IH} = Max, V _{IL} = Min	-1.89		-1.675	-1.65		-1.85	-1.825		-1.615	V
		-1.06		-0.89	-0.96		-0.81	-0.89		-0.70	
VOLA Low threshold VOHA High threshold	V _{IHA} = Min, V _{ILA} = Max			-1.655			-1.63			-1.595	
		-1.08			-0.98			-0.91			
Input current I _{IL} Low I _{IH} High	A, I, W = V _{IL} Min				0.5						µA
	A = V _{IH} Max I, W = V _{IH} Max Y = V _{IH} Max						220				
							200				
I _{EE} Supply current	V _{IH} Max						140				mA

AC ELECTRICAL CHARACTERISTICS² -30°C ≤ T_A ≤ +85°C, V_{CC1} = V_{CC2} = +2V, V_{EE} = -3.2V, R_L = 50Ω to ground

PARAMETER	FROM	TO	TEST CONDITIONS	LIMITS			UNIT
				Min ³	Typ	Max	
Associate time T _{A1} T _{A2}	I±	Y±				12	ns
	A+	Y+				12	
Disable time T _{D1} T _{D2} T _{D3}	A-	Y-				12	ns
	A+	D-				7	
	Y+	D-				13	
Setup and hold time T _{H1} Hold time T _{S2} Setup time T _{H2} Hold time T _{S3} Setup time T _{H3} Hold time T _{S4} Setup time	\bar{W} +	A+				1	ns
	A-	Y-				15	
	\bar{W} +	Y±				3	
	Y+	\bar{W} -				3	
	\bar{W} +	I±				3	
	I±	\bar{W} +				5	
T _W Write pulse width						10	ns
Access time T _{A3} Write T _{A4} Write T _{A5} Read T _{A6} Read	\bar{W} -	D±	T _{S4} ≥ T _W			17	ns
	I+,-	D+,-				13	
	Y-	D+				10	
	A-	D+					

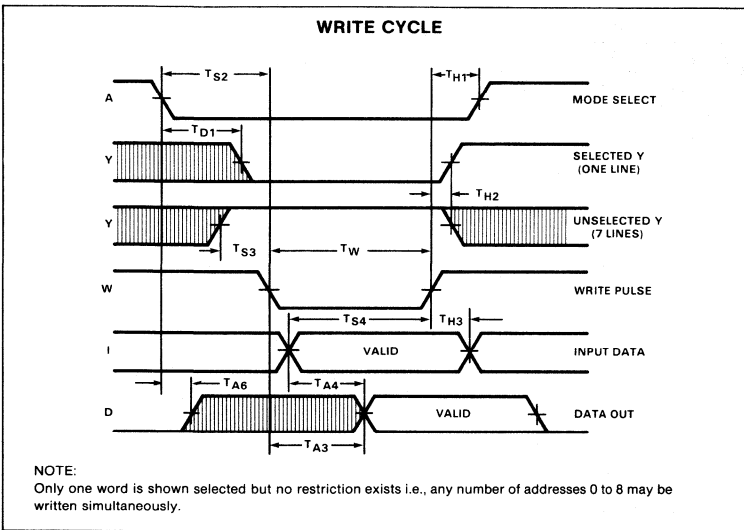
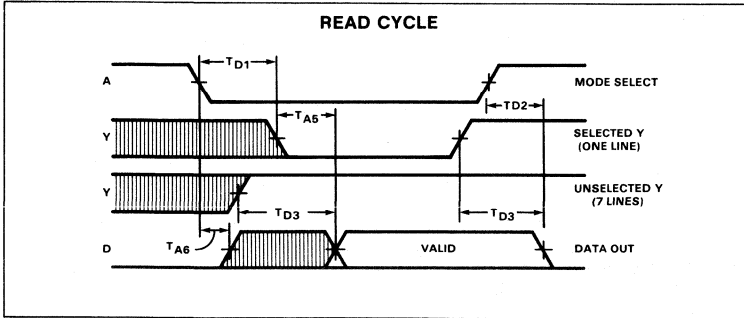
NOTES

- Each ECL 10K series device has been designed to meet the dc and ac specifications after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.
- Refer to dc characteristics.
- Minimum allowed.

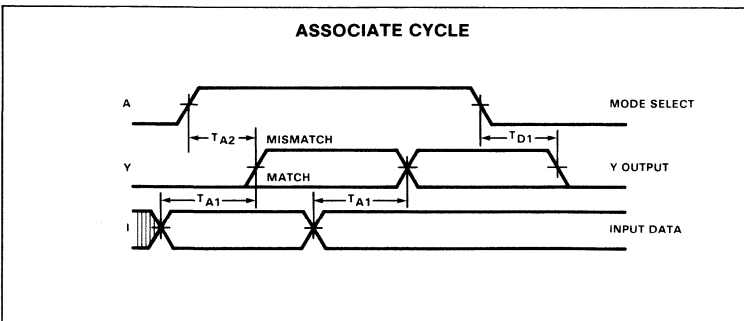
16-BIT ECL CAM (8x2)

10155

VOLTAGE WAVEFORMS



NOTE:
Only one word is shown selected but no restriction exists i.e., any number of addresses 0 to 8 may be written simultaneously.

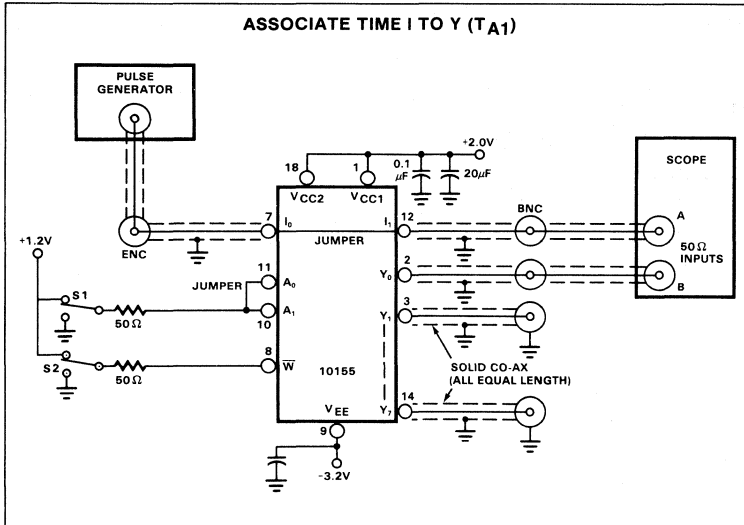


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16-BIT ECL CAM (8x2)

10155

MEASUREMENT CIRCUIT



64-BIT BIPOLAR WRITE-WHILE-READ RAM (32 × 2)

82S21 (O.C.)

DESCRIPTION

The 82S21 is ideally suited for high speed buffers and as the memory element in high speed accumulators.

Words are selected through a 5-input decoder when the chip enable input, CE is at logic high. \overline{WS}_0 and \overline{WS}_1 are the write select inputs for the bit 0 and bit 1 of the word selected. \overline{WE} is the write control input. When \overline{WS}_N and \overline{WE} are both at logic low data on the DI_0 and DI_1 data lines are written into the addressed word. The read function is enabled when either \overline{WS}_N or \overline{WE} is at logic high.

An internal latch provides the Write-While-Read capability. When the latch control line (strobe) is logic high and data is being read from the 82S21, the latch is effectively bypassed. The data at the output will be that of the addressed word. When strobe goes from a logic high to logic low, the outputs are latched and will remain latched regardless of the state of any other address or control line. When strobe goes from low to high, the outputs unlatch and will assume the contents of the present address word.

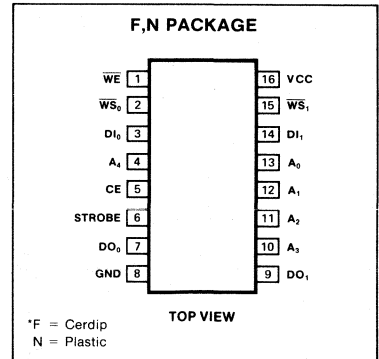
FEATURES

- Address access time: 50ns max
- Write cycle time:
 - Transparent mode: 45ns max
 - Latched mode: 60ns max
- Power dissipation: 7.5mW/bit typ
- 32mA output sink capability
- On-chip output latches
- Bit masking control lines
- Write-While-Read function
- Non-inverting open collector outputs
- TTL compatible

APPLICATIONS

- Scratch pad memory
- Buffer memory
- Accumulator register
- Control store

PIN CONFIGURATION



2

TRUTH TABLE

CE	WE	WS ₀	WS ₁	STROBE	MODE	OUTPUTS
X	X	X	X	0	Output hold Disabled	DO _N = (A _M) at last CE = high DO _N = high
0	X	X	X	0		
1	1	X	X	1 or ↓	Read (transparent/latched)	DO _N = (A _M)
1	0	1	1	1 or ↓	Read (transparent/latched)	
1	0	0	0	0	Write data	DO _N = (A _M) at last strobe = ↓
1	0	0	0	1	Write data	DO _N = DI _N
1	0	0	1	X	Write data into bit 0 only	If strobe = low: DO _N = (A _M) at last strobe = ↓
1	0	1	0	X	Write data into bit 1 only	If strobe = high: DO _N = DI _N or (A _M) as per WS _N

() = Contents of
↓ = High to low transition

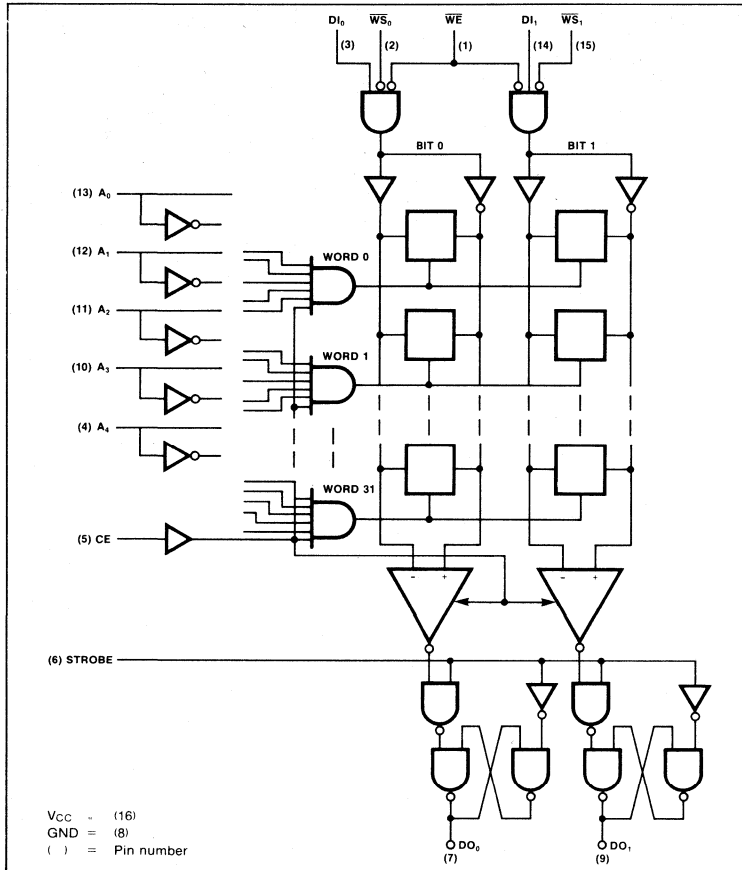
ABSOLUTE MAXIMUM RATINGS

PARAMETER ¹	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _{OH} Output voltage	+5.5	Vdc
I _{IN} Input current	±30	mA
I _{OUT} Output current	+100	mA
Temperature range		°C
T _A Operating	0 to +75	
T _{STG} Storage	-65 to +150	

64-BIT BIPOLAR WRITE-WHILE-READ RAM (32 × 2)

82S21 (O.C.)

LOGIC DIAGRAM



DC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER ¹	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IL} Input voltage Low ¹ V_{IH} Input voltage High ¹ V_{IC} Clamp ^{1,2}	$V_{CC} = 4.75\text{V}$ $V_{CC} = 5.25\text{V}$ $V_{CC} = 4.75\text{V}$, $I_{IN} = -18\text{mA}$	2		0.85 -1.2	V
V_{OL} Output voltage Low ^{1,3}	$V_{CC} = 4.75\text{V}$, $I_{OL} = 32\text{mA}$			0.45	V
I_{IL} Input current Low I_{IH} Input current High	$V_{IN} = 0.45\text{V}$ $V_{IN} = 5.5\text{V}$			-1.6 25	mA μA
I_{OLK} Output current Leakage ⁴	$V_{CC} = 5.25\text{V}$ $V_{OUT} = 5.25\text{V}$			40	μA
I_{CC} V_{CC} supply current ⁵	$V_{CC} = 5.25\text{V}$			130	mA
C_{IN} Capacitance Input C_{OUT} Capacitance Output	$V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$		5 8		pF

64-BIT BIPOLAR WRITE-WHILE-READ RAM (32 × 2)

82S21 (O.C.)

AC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$, $R_1 = 150\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$

PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
				Min	Typ	Max	
Access time T_{AA} Address T_{CE} Chip enable	Output Output	Address Chip enable	Latched or transparent read			50 50	ns
Disable time T_{CD} Chip enable	Output	Chip enable	Latched or transparent read			50	ns
Setup and hold time T_{WSA} Setup time T_{WHA} Hold time	Write	Address	Latched or transparent write	15			ns
T_{WSD} Setup time T_{WHD} Hold time				5			
T_{WSC} Setup time T_{WHC} Hold time	Write	Data in	Latched or transparent write	25			
T_{WSC} Setup time T_{WHC} Hold time				5			
T_{CES} Setup time T_{CEH} Hold time	Strobe	Chip enable	Latched read	50			
T_{ADH} Hold time				5			
Pulse width T_{SW} Strobe T_{WP} Write inputs	Output	Address	Latched read Latched or transparent write	30			ns
Latch time T_{SLR} Read strobe T_{SLW} Write strobe T_{LRW} WWR strobe				25			
T_{DL} Strobe	Output	Strobe	Latched read			25	ns
T_{WD} Valid time				Output	Write	Latched or transparent write	

NOTES

1. All voltage values are with respect to network ground terminal.
2. Test each input one at a time.
3. Measured with a logic low stored. Output sink current is supplied

through a resistor to V_{CC} .

4. Measured with V_{IL} applied to CE, and V_{IH} to strobe.
5. I_{CC} is measured with all inputs at 4.5V, and the outputs open.

MEMORY TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable high (with Address valid) and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes low and Data Output is in high state.

T_{AA} Delay between beginning of valid Address (with Chip Enable high) and when Data Output becomes valid.

T_{WSC} Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.

T_{WHC} Required delay between end of Write Enable pulse and end of Chip Enable.

T_{WSA} Required delay between beginning of valid Address and beginning of Write Enable pulse.

T_{WHA} Required delay between end of Write Enable pulse and end of valid Address.

T_{WSD} Required delay between begin-

T_{WHD} Required delay between end of Write Enable pulse and end of valid Input Data.

T_{WP} Width of Write Enable pulse.

T_{WD} Delay between beginning of Write Enable pulse and when Data Output reflects the contents of the Data Input.

T_{CES} Minimum delay between leading edge of Chip Enable and trailing edge of Strobe, for latching valid output data.

T_{CEH} Required delay between trailing edge of Strobe and end of Chip Enable, for latching valid output data.

T_{SLR} Minimum delay between Address valid time and trailing edge of Strobe, for latching valid output data.

T_{SW} Minimum width of Strobe pulse required to update contents of output data latches.

T_{ADH} Required delay between trailing edge of Strobe and end of valid

ning of valid Data Input and end of Write Enable pulse.

Address.

T_{DL} Delay between leading edge of Strobe and when output data latches are released.

T_{LRW} Minimum delay required between trailing edge of Strobe and leading edges of Write Enable or Write Select for latching old output data (being read) while new data is being written (at the same address).

T_{SLW} Minimum delay between leading edge of Write Enable or Write Select and trailing edge of Strobe for latching data being written in output data latches.

T_{DL}

T_{LRW}

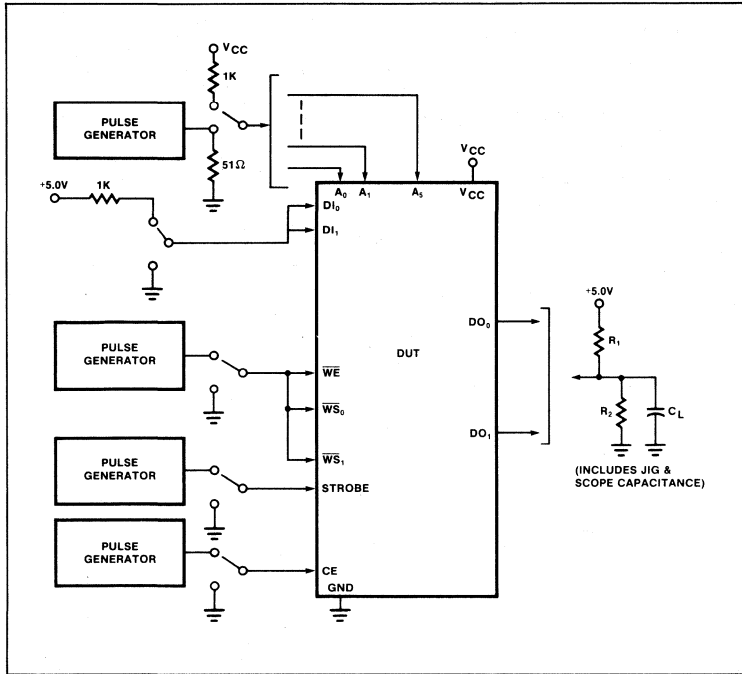
T_{SLW}



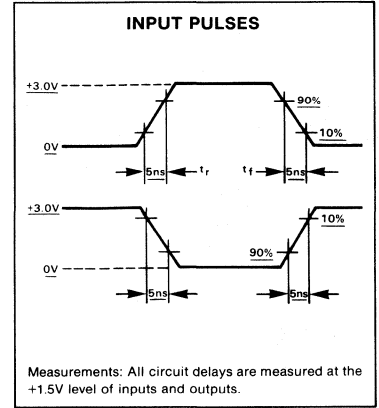
64-BIT BIPOLAR WRITE-WHILE-READ RAM (32 × 2)

82S21 (O.C.)

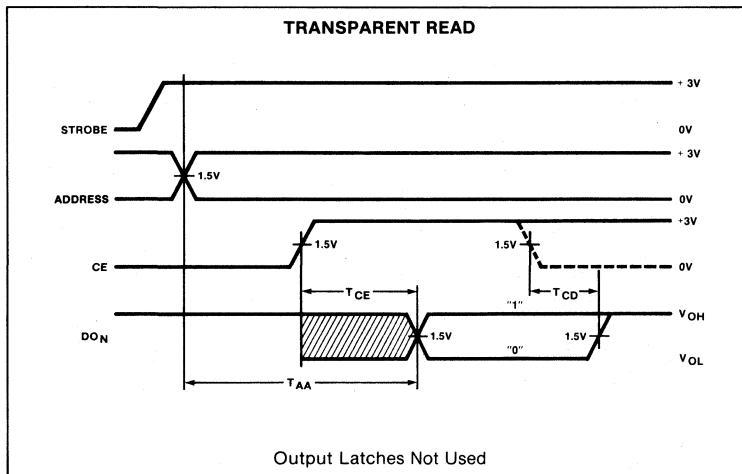
TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAMS

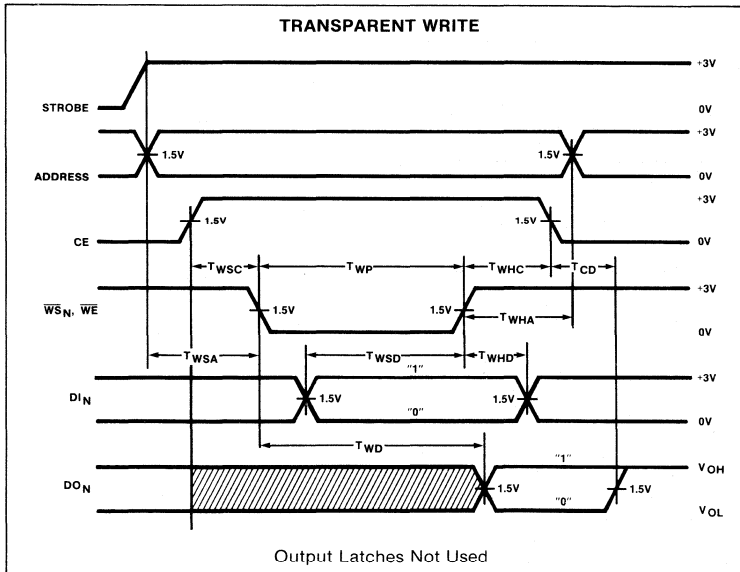
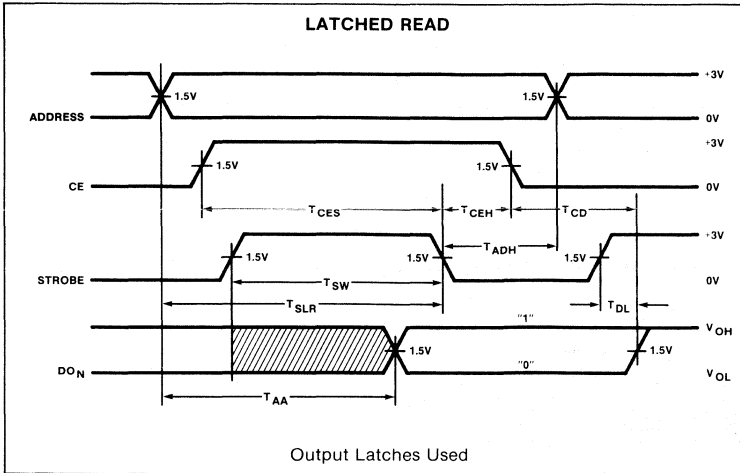


64-BIT BIPOLAR WRITE-WHILE-READ RAM (32 × 2)

82S21 (O.C.)

2

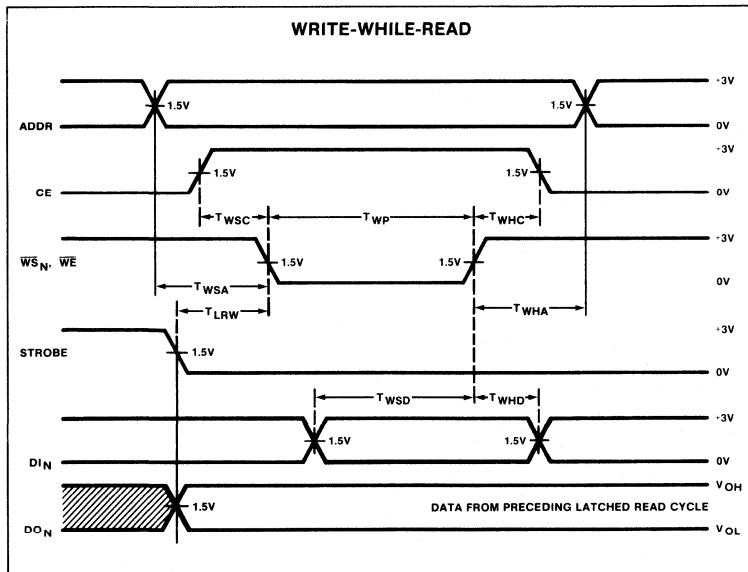
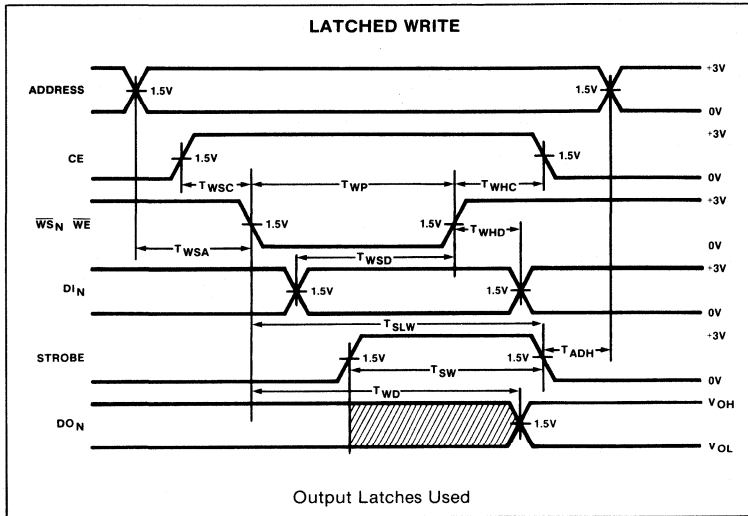
TIMING DIAGRAMS (Cont'd)



64-BIT BIPOLAR WRITE-WHILE-READ RAM (32 × 2)

82S21 (O.C.)

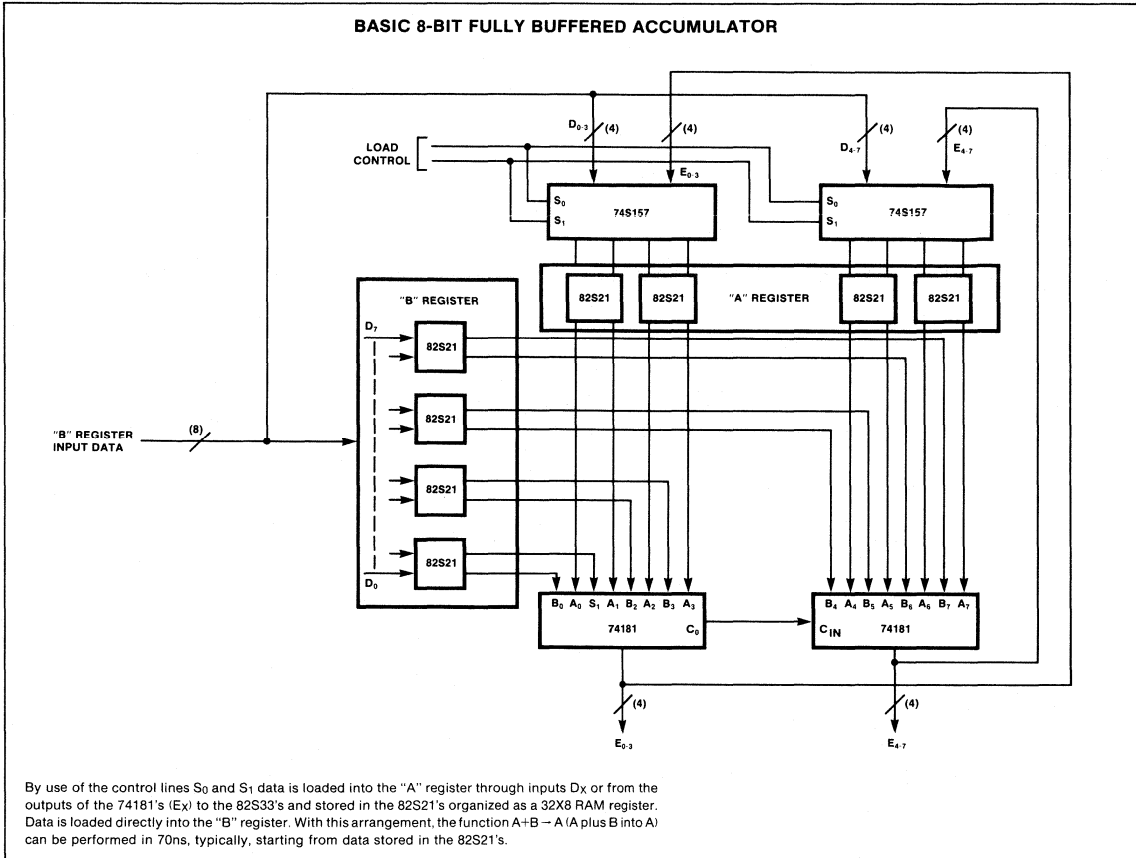
TIMING DIAGRAMS (Cont'd)



64-BIT BIPOLAR WRITE-WHILE-READ RAM (32x2)

82S21 (O.C.)

TYPICAL APPLICATION



2

Section 3 RAMs, 64-Bit

64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4) 82S25 (O.C.), 3101A (O.C.), 54/74S189 (T.S.)

DESCRIPTION

This family of Read/Write Random Access Memories is ideal for use in scratch pad and high-speed buffer memory applications.

These products are fully decoded memory arrays with separate input and output lines. They feature pnp inputs and 1 chip enable line for ease of memory expansion.

During Write, the outputs of each product assume the logic state defined in the truth table.

The family is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N74S189N, N82S25N, and for the military temperature range (-55°C to +125°C) specify S54S189 F or W, S82S25 F or W.

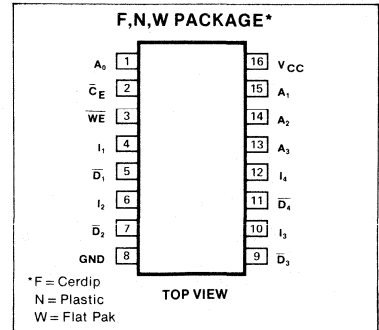
FEATURES

- Output access time:
 N82S25: 50ns max
 S82S25: 60ns max
 N3101A: 35ns max
 N74S189: 35ns max
 S54S189: 50ns max
- Power dissipation: 6.25mW/bit, typ
- Input loading:
 N grade: -100µA max
 S grade: -150µA max
- On-chip address decoding
- Output options:
 82S25: Open collector
 3101A: Open collector
 54/74S189: Tri-state
- Schottky processed
- TTL compatible

APPLICATIONS

- Scratch pad memory
- Buffer memory
- Push down stacks
- Control store

PIN CONFIGURATION

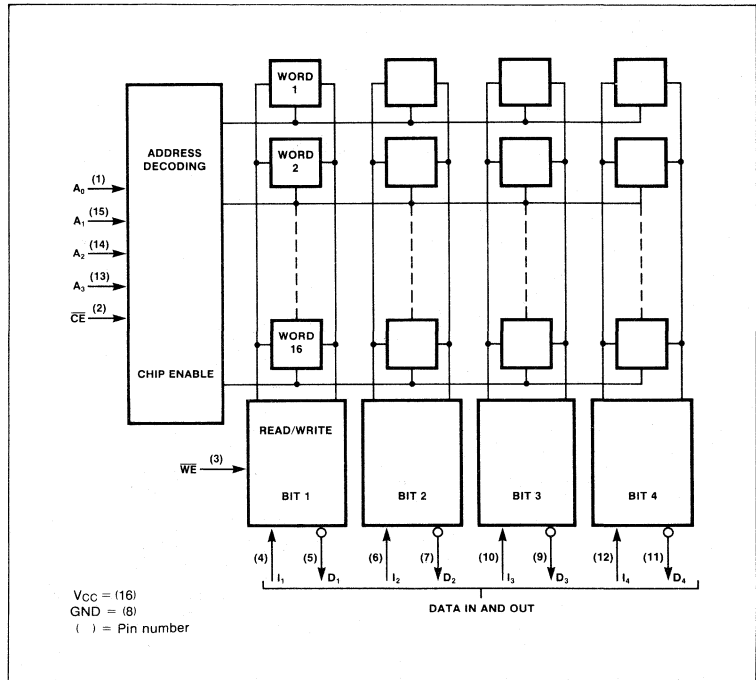


3

TRUTH TABLE

	CE	WE	D IN	82S25	3101A	54/74S189
				DATA OUT		
Read	0	1	X	Stored data	Stored data	Stored data
Write "0"	0	0	0	1	1	Hi-Z
Write "1"	0	0	1	1	1	Hi-Z
Disable	1	X	X	1	1	Hi-Z

BLOCK DIAGRAM



64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4) 82S25 (O.C.), 3101A (O.C.), 54/74S189 (T.S.)

AC ELECTRICAL CHARACTERISTICS

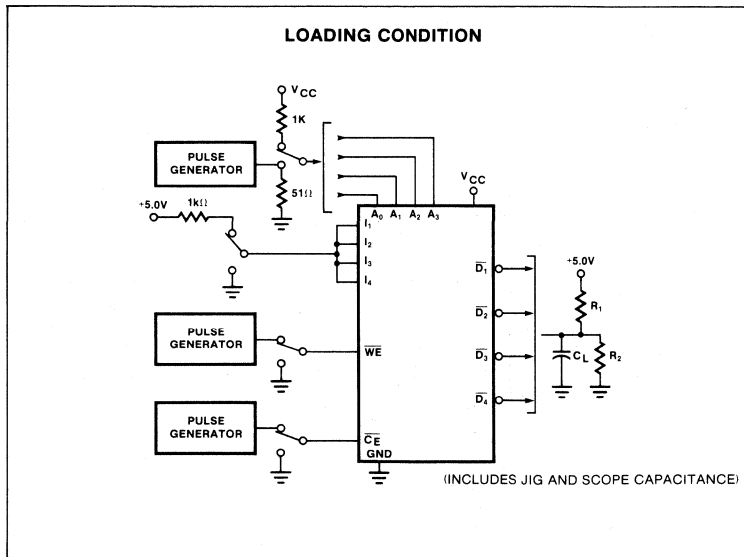
$R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, See ac test load
 N grade: $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$
 S grade: $-55^\circ C \leq T_A \leq +125^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER	TO	FROM	N82S25			S82S25			N3101A, N74S189			S54S189			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T _{AA} Access time					50			60			35			50	ns
T _{CE} Chip enable					35			35			17			25	
T _{CD} Disable time	Output	Chip enable			35			35			17			40	ns
T _{WD} Response time	Output	Write enable			25			30			25			50	ns
T _{WR} Write recovery time					50			60			35			40	ns
T _{WSA} Setup time	Write enable	Address	5		10			0			0			ns	
T _{WHA} Hold time			5		10			0		10					
T _{WSD} Setup time	Write enable	Data in	30		30			25			30			ns	
T _{WHD} Hold time			5		10			0		10					
T _{WSC} Setup time	Write enable	\overline{CE}	0		0			0			0			ns	
T _{WHC} Hold time			5		5			0		0					
T _{WP} Pulse width			30		30			25			30			ns	

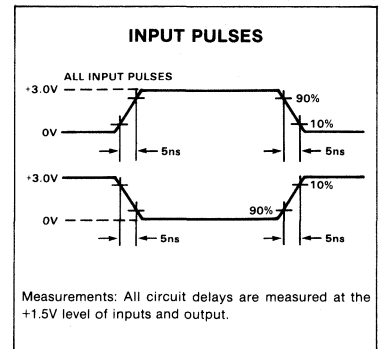
NOTES

1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. Output sink current is supplied through a resistor to V_{CC}.
3. All sense outputs in low state.
4. To guarantee a Write into the slowest bit.
5. Positive current is defined as into the terminal referenced.
6. Positive logic definition: high = +5.0V, low = GND.
7. Test each input one at a time.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



64-BIT BIPOLAR SCRATCH PAD MEMORY (16x4) 82S25 (O.C.), 3101A (O.C.), 54/74S189 (T.S.)

ABSOLUTE MAXIMUM RATINGS

PARAMETER ¹		RATING	UNIT
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
V _{OH}	Output voltage High	+5.5	Vdc
T _A	Temperature range Operating N grade S grade	0 to +75 -55 to +125	°C
T _{STG}	Storage	-65 to +150	

3

DC ELECTRICAL CHARACTERISTICS N grade: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
S grade: 55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER ⁷	TEST CONDITIONS ⁶	N GRADE			S GRADE			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low ¹ High ¹ Clamp ^{1,7}			.85			.80	V
V _{OL} V _{OH}	Output voltage Low ^{2,3,1} High (54/74S189) ¹			0.45			0.5	V
I _{IL} I _{IH}	Input current Low High			-100 10			-150 25	μA
I _{OLK} I _{OS} I _{O(OFF)}	Output current Leakage Short circuit (54/74S189) Hi-Z (54/74S189)			100 -100 ±50		-30	100 -100 ±50	μA mA μA
I _{CC}	Supply current ³ 82S25 3101A 54/74S189			105 105 110			120 120 110	mA
C _{IN} C _{OUT}	Capacitance Input Output			5 8			5 8	pF

Section 4
RAMs,
256-Bit

256-BIT BIPOLAR RAM (256 × 1)

82S16 (T.S.)/82S17 (O.C.)

DESCRIPTION

The 82S16 and 82S17 are Read/Write memory arrays which feature either open collector or 3-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

Both devices have fast Read access and Write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

Both devices are available in the commercial temperature range (0°C to +75°C) and

the military temperature range (-55°C to +125°C). They are specified as: N82S16F or N or N82S17F or N for the commercial temperature range, and S82S16F, G, or R or S82S17F, G, or R for the military temperature range. Military products are available as fully processed to Mil-Std 883 Level B or Level C; specify either 883B or 883C.

See page 4-9 for Truth Table, Timing Diagrams, Test Circuit and Waveform.

FEATURES

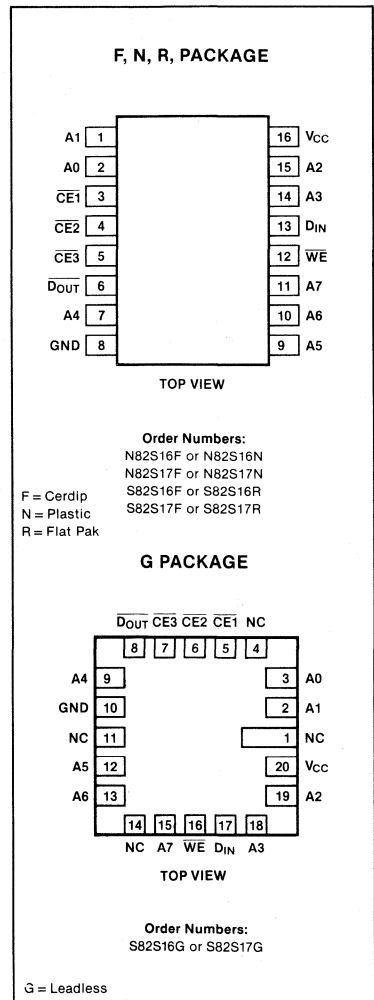
- **Address access time:**
N82S16/17: 50ns max
S82S16/17: 70ns max
- **Write cycle time:**
N82S16/17: 55ns max
S82S16/17: 70ns max
- **Power dissipation: 1.5mW/bit typ**
- **Input loading:**
N82S16/17: -100mA max
S82S16/17: -250mA max
- **Output follows complement of data input during Write**

- **On-chip address decoding**
- **Output option:**
82S16 3-state
82S17 Open collector
- **Schottky clamped**
- **TTL compatible**

APPLICATIONS

- Buffer memory
- Writable control store
- Memory mapping
- Push down stack
- Scratch pad

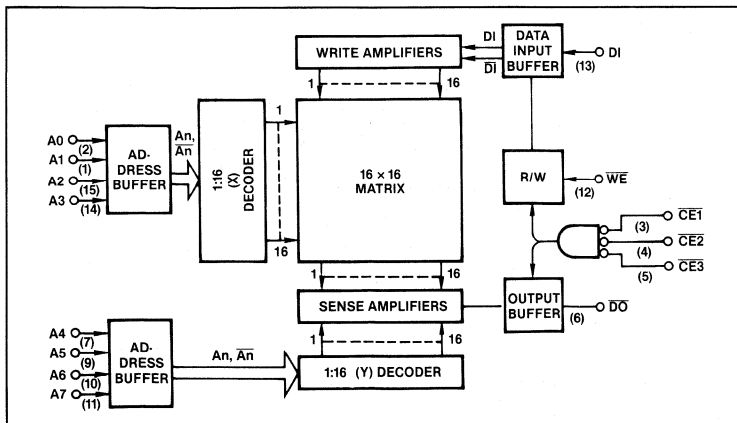
PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+ 7	Vdc
V _{IN} Input voltage	+ 5.5	Vdc
V _{OUT} Output voltage High (open collector)	+ 5.5	Vdc
T _A Temperature Range Operating	0 to +70	°C
N grade	-55 to +125	
S grade	-65 to +150	
T _{STG} Storage	-65 to +150	°C

BLOCK DIAGRAM



256-BIT BIPOLAR RAM (256 × 1)

82S16 (T.S.)/82S17 (O.C.)

DC ELECTRICAL CHARACTERISTICS N82S16/17: 0 °C ≤ T_A ≤ + 75 °C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S16/17: - 55 °C ≤ T_A ≤ + 125 °C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS	N82S16/17			S82S16/17			UNIT
		Min	Typ ¹	Max	Min	Typ ¹	Max	
V _{IH} V _{IL} V _{IC}	Input voltage ² High Low Clamp ³ V _{CC} = max V _{CC} = min V _{CC} = min, I _{IN} = - 12mA	2.0	- 1.0	0.85 - 1.5	2.0	- 1.0	0.8 - 1.5	V
V _{OH} V _{OL}	Output voltage ² High (82S16) ⁴ Low ⁵ V _{CC} = min I _{OH} = - 3.2mA I _{OL} = 16mA	2.6	0.35	0.45	2.4	0.35	0.5	V
I _{IH} I _{IL}	Input current ³ High Low V _{CC} = max V _{IN} = 5.5V V _{IN} = 0.45V		1 - 10	25 - 100		1 - 10	25 - 250	μA
I _{OLK} I _{O(OFF)} I _{OS}	Output current Leakage (82S17) ⁶ Hi-Z state (82S16) ⁶ Short circuit (82S16) ⁷ V _{OUT} = 5.5V V _{OUT} = 5.5V V _{OUT} = 0.45V V _{CC} = max, V _O = 0V		1 1 - 1	40 40 - 40		1 1 - 1	40 50 - 50	μA
I _{CC}	V _{CC} supply current ⁸ V _{CC} = max		80	115		80	120	mA
C _{IN} C _{OUT}	Capacitance Input Output V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS R₁ = 270Ω, R₂ = 6000Ω, C_L = 30pF
 N82S16/17: 0 °C ≤ T_A ≤ + 75 °C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S16/17: - 55 °C ≤ T_A ≤ + 125 °C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S16/17			S82S16/17			UNIT
			Min	Typ ¹	Max	Min	Typ ¹	Max	
T _{AA} T _{CE}	Access time Address Chip enable Output Output	Address Chip enable		40 30	50 40		40 30	70 40	ns
T _{CD} T _{WD}	Disable time Valid time Output Output	Chip enable Write enable		30 30	40 40		15 30	40 55	ns ns
T _{WSA} T _{WHA} T _{WSD} T _{WHD} T _{WSC} T _{WHC}	Setup and hold time Setup time Hold time Write enable Setup time Hold time Write enable Setup time Hold time Write enable	Address Data in CĒ	15 5 40 5 10 5	5 0 30 0 0 0		20 10 50 10 10 10	5 0 30 0 0 0		ns
T _{Wp}	Pulse width Write enable ⁹		30	15		40	15		ns

NOTES

- All typical values are at V_{CC} = 5V, T_A + 25 °C.
- All voltage values are with respect to network ground terminal.
- Test each input one at a time.
- Measured with a logic low stored and V_{IL} applied to CĒ1, CĒ2 and CĒ3.
- Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
- Measured with V_{IH} applied to CĒ1, CĒ2 and CĒ3.
- Duration of the short-circuit should not exceed 1 second.
- I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
- Minimum required to guarantee a Write into the slowest bit.

256-BIT BIPOLAR RAM (256 × 1)

82LS16 (T.S.)/82LS17 (O.C.)

DESCRIPTION

The 82LS16 and 82LS17 are Read/Write memory arrays which feature either open collector or 3-state output options for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors which reduce input loading.

During Write operation, the logical state of the output of both devices follows the complement of the data input being written. This feature allows faster execution of Write/Read cycles, enhancing the performance of systems utilizing indirect addressing modes, and/or requiring immediate verification following a Write cycle.

Both devices have fast Read access and Write cycle times, as well as low power requirements and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, where power limitations are of major concern.

Both devices are available in the commercial temperature range (0°C to +75°C) and the military temperature range (-55°C to +125°C). They are specified as: N82LS16F or N or N82LS17F or N for the commercial temperature range, and S82LS16F, G, or W or S82LS17F, G, or W for the military temperature range. Military products are available as fully processed to Mil-Std 883 Level B or Level C; specify either 883B or 883C.

See page 4-9 for Truth Table, Timing Diagrams, Test Circuit and Waveform.

FEATURES

- **Address access time:**
N82LS16/17: 40ns max
S82LS16/17: 60ns max
- **Write cycle time:**
N82LS16/17: 40ns max
S82LS16/17: 65ns max
- **Power dissipation: 0.98mW/bit typ**
- **Input loading:**
N82LS16/17: -100 μ A max
S82LS16/17: -250 μ A max

- **Output follows complement of data input during Write**
- **On-chip address decoding**
- **Output option:**
82LS16 3-state
82LS17 Open collector
- **Schottky clamped**
- **TTL compatible**

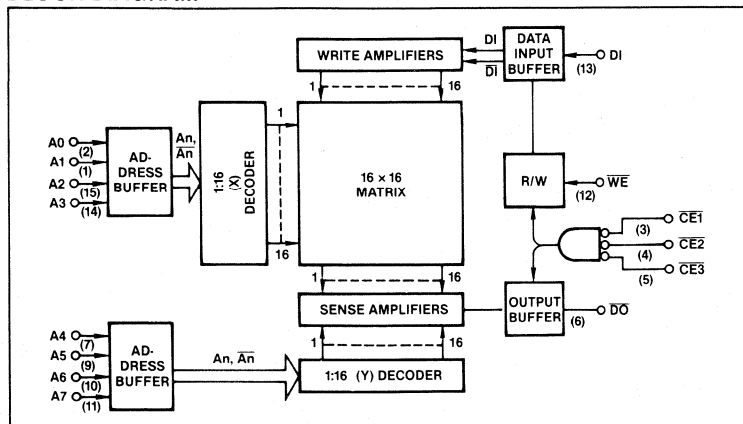
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

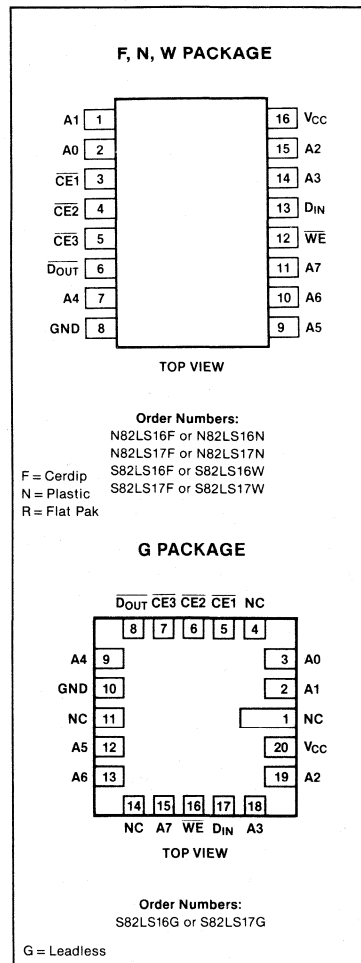
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+ 7	Vdc
V _{IN} Input voltage	+ 5.5	Vdc
V _{OUT} Output voltage		Vdc
V _{OUT} High (open collector)	+ 5.5	
T _A Temperature Range		°C
Operating	0 to +70	
N grade	-55 to +125	
S grade	-65 to +150	
T _{STG} Storage		°C

BLOCK DIAGRAM



PIN CONFIGURATIONS



256-BIT BIPOLAR RAM (256 × 1)

82LS16 (T.S.)/82LS17 (O.C.)

DC ELECTRICAL CHARACTERISTICS N82LS16/17: 0 °C ≤ T_A ≤ + 75 °C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82LS16/17: - 55 °C ≤ T_A ≤ + 125 °C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS	N82LS16/17			S82LS16/17			UNIT		
		Min	Typ ¹	Max	Min	Typ ¹	Max			
V _{IH} V _{IL} V _{IC}	Input voltage ² High Low Clamp ³	V _{CC} = max V _{CC} = min V _{CC} = min, I _{IN} = - 12mA		2.0		0.85	2.0		0.8	V
V _{OH} V _{OL}	Output voltage ² High (82LS16) ⁴ Low ⁵	V _{CC} = min I _{OH} = - 3.2mA I _{OL} = 16mA		2.6		0.45	2.4		0.5	V
I _{IH} I _{IL}	Input current ³ High Low	V _{CC} = max V _{IN} = 5.5V V _{IN} = 0.45V			1	25		1	25	μA
I _{OLK} I _{O(OFF)}	Output current Leakage (82LS17) ⁵ Hi-Z state (82LS16) ⁶	V _{OUT} = 5.5V V _{OUT} = 5.5V V _{OUT} = 0.45V			1	40		1	40	μA
I _{OS}	Short circuit (82LS16) ⁷	V _{CC} = max, V _O = 0V		- 20		- 70	- 20		- 70	
I _{CC}	V _{CC} supply current ⁸	V _{CC} = max			50	70		50	100	mA
C _{IN} C _{OUT}	Capacitance Input Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V			5			5		pF

AH ELECTRICAL CHARACTERISTICS R₁ = 270Ω, R₂ = 600Ω, C_L = 30pF
 N82LS16/17: 0 °C ≤ T_A ≤ + 75 °C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82LS16/17: - 55 °C ≤ T_A ≤ + 125 °C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82LS16/17			S82LS16/17			UNIT	
			Min	Typ ¹	Max	Min	Typ ¹	Max		
T _{AA} T _{CE}	Access time Address Chip enable	Output Output	Address Chip enable		30 15	40 25		30 15	70 40	ns
T _{CD} T _{WD}	Disable time Valid time	Output Output	Chip enable Write enable		15 30	25 40		15 30	40 55	ns ns
T _{WSA} T _{WHA}	Setup and hold time Setup time Hold time	Write enable	Address		0 0	- 5 - 5		10 10	- 5 - 5	ns
T _{WSD} T _{WHD}	Setup time Hold time	Write enable	Data in		25 0	15 - 5		40 10	15 - 5	
T _{WSC} T _{WHC}	Setup time Hold time	Write enable	\overline{CE}		0 0	- 5 - 5		10 10	- 5 - 5	
T _{WP}	Pulse width Write enable ⁹				25	15		40	15	ns

NOTES

1. All typical values are at V_{CC} = 5V, T_A + 25 °C.
2. All voltage values are with respect to network ground terminal.
3. Test each input one at a time.
4. Measured with a logic low stored and V_{IL} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
5. Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
6. Measured with V_{IH} applied to $\overline{CE1}$, $\overline{CE2}$ and $\overline{CE3}$.
7. Duration of the short-circuit should not exceed 1 second.
8. I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V and the output open.
9. Minimum required to guarantee a Write into the slowest bit.

256-BIT TTL RAM (256 × 1)

54/74S301 (O.C.)

DESCRIPTION

The 54/74S301 is a Read/Write memory array which features an open collector output for optimization of word expansion in bused organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors, which reduce input loading.

The additional feature of output blanking during Write (\bar{D}_O terminal "H") permits \bar{D}_O and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast Read access and Write cycle times, and thus are ideally suited in high speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

The 54/74S301 is available in both the commercial temperature range (0°C to

+75°C) and the military temperature range (-55°C to +125°C). They are specified as: N74S301F or N for the commercial temperature range, S54S301F, G, or R for the military temperature range. Military products are available as fully processed to Mil Std 883 Level B or Level C; specify either 883B or 883C.

See page 4-9 for Truth Table, Timing Diagrams, Test Circuit and Waveform.

FEATURES

- **Address access time:**
N74S301: 50ns max
S54S301: 70ns max
- **Write cycle time:**
N74S301: 50ns max
S54S301: 60ns max

- **Power dissipation:** 1.5mW/bit typ
- **Input loading:**
N74S301: -100µA max
S54S301: -250µA max
- **Output blanking during Write**
- **On-chip address decoding**
- **Schottky clamped**
- **TTL compatible**

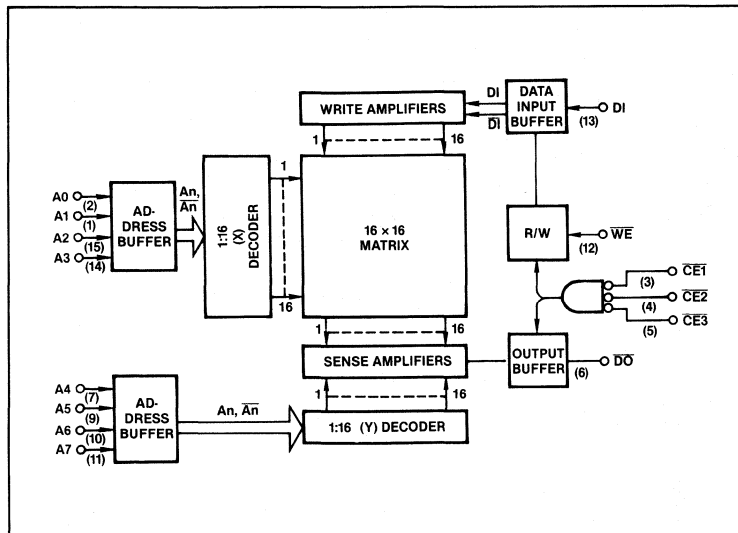
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

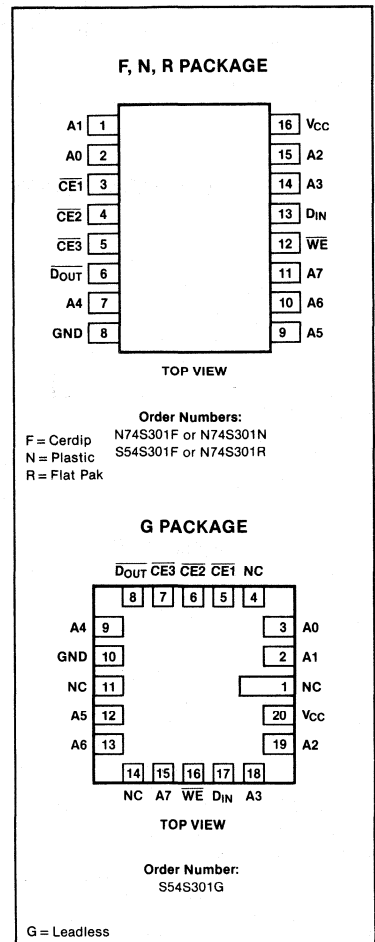
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC}	Supply voltage	+ 7	Vdc
V _{IN}	Input voltage	+ 5.5	Vdc
V _{OUT}	Output voltage High (open collector)	+ 5.5	Vdc
T _A	Temperature Range Operating N grade S grade	0 to + 70 - 55 to + 125	°C
T _{STG}	Storage	- 65 to + 150	°C

BLOCK DIAGRAM



PIN CONFIGURATIONS



256-BIT TTL RAM (256 × 1)

54/74S301 (O.C.)

DC ELECTRICAL CHARACTERISTICS N74S301: 0 °C ≤ T_A ≤ + 70 °C, 4.75V ≤ V_{CC} ≤ 5.25V
 S54S301: - 55 °C ≤ T_A ≤ + 125 °C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS	N74S301			S54S301			UNIT
		Min	Typ ¹	Max	Min	Typ ¹	Max	
V _{IL} V _{IH} V _{IC}	Input voltage ² Low High Clamp ³ V _{CC} = min V _{CC} = max V _{CC} = min, I _{IN} = - 18mA	2.0	- 1.0	- 1.2	2.0	- 1.0	- 1.2	V
V _{OL}	Output voltage Low ⁵ V _{CC} = min I _{OL} = 16mA		0.35	0.45		0.35	0.50	V
I _{IL} I _{IH}	Input current ² Low High V _{CC} = max V _{IL} = 0.45V V _{IH} = 2.7V			- 100 25			- 250 25	μA μA
I _{OLK}	Output current Leakage ⁵ V _{IH} = 2V, V _O = 5.5V			40			50	μA
I _{CC}	V _{CC} supply current ⁸ V _{CC} = max V _{CC} = max, T _A = + 125 °C		80	130		80	130 99	mA
C _{IN} C _{OUT}	Capacitance Input Output V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS R1 = 270Ω, R2 = 1KΩ, C_L = 15pF
 N74S301: 0 °C ≤ T_A ≤ + 75 °C, 4.75V ≤ V_{CC} ≤ 5.25V
 S54S301: - 55 °C ≤ T_A ≤ + 125 °C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N74S301			S54S301			UNIT
			Min	Typ ¹	Max	Min	Typ ¹	Max	
T _{AA} T _{CE}	Access time Address Chip enable Output Output	Address Chip enable		40 30	50 40		40 30	70 40	ns
T _{CD} T _{WD}	Disable time Valid time Output Output	Chip enable Write enable		30 30	40 40			45 55	ns ns
T _{WSA} T _{WHA}	Setup and hold time Setup time Hold time Write enable	Address	20 5	5 0		20 10	5 0		ns
T _{WSD} T _{WHD}	Setup time Hold time Write enable	Data in	40 5	30 0		50 10	30 0		
T _{WSC} T _{WHC}	Setup time Hold time Write enable	CE	10 5	0 0		10 10	0 0		
T _{WP}	Pulse width Write enable ⁹		30	15		40	15		ns

NOTES

- All typical values are at V_{CC} = 5V, T_A = 25 °C.
- All voltage values are with respect to network ground terminal.
- Test each input one at a time.
- Measured with a logic low stored and V_{IL} applied to CE1, CE2 and CE3.
- Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
- Measured with V_{IH} applied to CE1, CE2 and CE3.
- Duration of the short-circuit should not exceed 1 second.
- I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
- Minimum required to guarantee a Write into the slowest bit.

256-BIT TTL RAM (256 × 1)

54/74LS301 (O.C.)

DESCRIPTION

The 54/74LS301 is a Read/Write memory array which features an open collector output for optimization of word expansion in bus organizations. Memory expansion is further enhanced by full on-chip address decoding, 3 chip enable inputs and PNP input transistors, which reduce input loading.

The additional feature of output blanking during Write (\bar{D}_O terminal "H") permits \bar{D}_O and D_{IN} terminals to share a common I/O line to reduce system interconnections. These devices have fast Read access and Write cycle times, and thus are ideally suited in high-speed memory applications such as cache, buffers, scratch pads, writable control stores, etc.

The 54/74LS301 is available in both the commercial temperature range (0°C to

+ 75°C) and the military temperature range (-55°C to +125°C). They are specified as: N74LS301F or N for the commercial temperature range, and S54LS301F, G, or W for the military temperature range. Military products are available as fully processed to Mil-Std 883 Level B or Level C; specify either 883B or 883C.

See page 4-9 for Truth Table, Timing Diagrams, Test Circuit and Waveform.

FEATURES

- **Address access time:**
N74LS301: 40ns max
S54LS301: 70ns max
- **Write cycle time:**
N74LS301: 25ns max
S54LS301: 60ns max

- **Power dissipation: 0.98mW/bit typ**
- **Input loading:**
N74LS301: -100 μ A max
S54LS301: -250 μ A max
- **Output blanking during Write**
- **On-chip address decoding**
- **Schottky clamped**
- **TTL compatible**

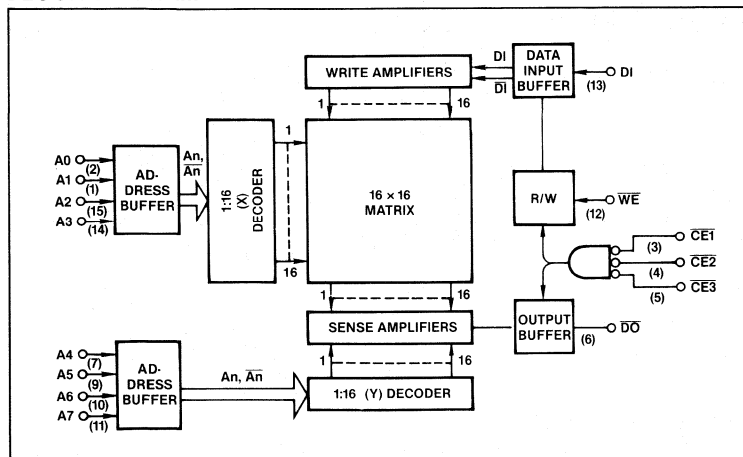
APPLICATIONS

- **Buffer memory**
- **Writable control store**
- **Memory mapping**
- **Push down stack**
- **Scratch pad**

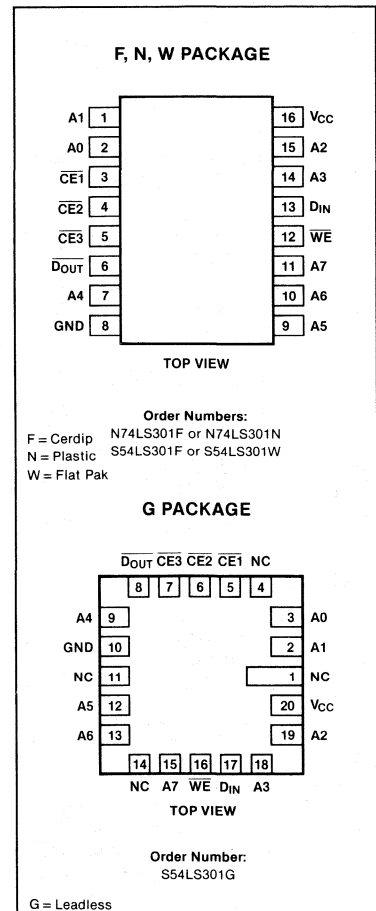
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+ 7	Vdc
V _{IN} Input voltage	+ 5.5	Vdc
V _{OUT} Output voltage		Vdc
V _{OUT} High (open collector)	+ 5.5	
T _A Temperature Range		°C
Operating	0 to + 70	
N grade	- 55 to + 125	
S grade	- 65 to + 150	
T _{STG} Storage		°C

BLOCK DIAGRAM



PIN CONFIGURATIONS



256-BIT TTL RAM (256 × 1)

54/74LS301 (O.C.)

DC ELECTRICAL CHARACTERISTICS N74LS301: 0 °C ≤ T_A ≤ +75 °C, 4.75V ≤ V_{CC} ≤ 5.25V
 S54LS301: -55 °C ≤ T_A ≤ +125 °C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS	N74LS301			S54LS301			UNIT
		Min	Typ ¹	Max	Min	Typ ¹	Max	
V _{IL} V _{IH} V _{IC}	Input voltage ² Low High Clamp ³	V _{CC} = min V _{CC} = max V _{CC} = min, I _{IN} = -18mA	2.0		0.85 -1.2	2.0	0.8 -1.2	V
V _{OL}	Output voltage Low ⁵	V _{CC} = min I _{OL} = 16mA		0.45			0.50	V
I _{IL} I _{IH}	Input current ² Low High	V _{CC} = max V _{IL} = 0.45V V _{IH} = 2.7V		-100 25			-250 25	μA
I _{OLK}	Output current Leakage ⁵	V _{IH} = 2V, V _O = 5.5V		40			50	μA
I _{CC}	V _{CC} supply current ⁸	V _{CC} = max		50 70		50 100		mA
C _{IN} C _{OUT}	Capacitance Input Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		5 8		pF

AC ELECTRICAL CHARACTERISTICS R₁ = 270Ω, R₂ = 1KΩ, C_L = 15pF
 N74LS301: 0 °C ≤ T_A ≤ +75 °C, 4.75V ≤ V_{CC} ≤ 5.25V
 S54LS301: -55 °C ≤ T_A ≤ +125 °C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N74LS301			S54LS301			UNIT
			Min	Typ ¹	Max	Min	Typ ¹	Max	
T _{AA} T _{CE}	Access time Address Chip enable	Output Output	Address Chip enable	30 15	40 25		30 15	70 40	ns
T _{CD} T _{WD}	Disable time Valid time	Output Output	Chip enable Write enable	15 30	25 40		15 30	40 55	ns ns
T _{WSA} T _{WHA}	Setup and hold time Setup time Hold time	Write enable	Address	0 0	-5 -5		10 10	-5 -5	ns
T _{WSD} T _{WHD}	Setup time Hold time	Write enable	Data in	25 0	15 -5		40 10	15 -5	
T _{WSC} T _{WHC}	Setup time Hold time	Write enable	$\overline{\text{CE}}$	0 0	-5 -5		10 10	-5 -5	
T _{WP}	Pulse width Write enable ⁹			25	15		40	15	ns

NOTES

- All typical values are at V_{CC} = 5V, T_A +25 °C.
- All voltage values are with respect to network ground terminal.
- Test each input one at a time.
- Measured with a logic low stored and V_{IL} applied to $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$ and $\overline{\text{CE}}_3$.
- Measured with a logic high stored. Output sink current is supplied through a resistor to V_{CC}.
- Measured with V_{IH} applied to $\overline{\text{CE}}_1$, $\overline{\text{CE}}_2$ and $\overline{\text{CE}}_3$.
- Duration of the short-circuit should not exceed 1 second.
- I_{CC} is measured with the Write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
- Minimum required to guarantee a Write into the slowest bit.

Section 5 RAMs, Byte-Organized

576-BIT BIPOLAR RAM (64 × 9)

82S09/82S19 (O.C.)

DESCRIPTION

The organization of this device allows byte storage of data, including parity. Where parity is not monitored, the ninth bit can be used as a tag or status indicator for each word stored. Ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which cost and performance requirements dictate a wide data path in favor of word depth.

The 82S09/19 features open collector outputs, chip enable input, and a very low current pnp input structure to enhance memory expansion.

During Write operation, the 82S19 output goes to a "1".

The 82S09/19 is available in the commercial and military temperature ranges. For the commercial temperature ranges (0°C to +75°C) specify N82S09/19, F or N and for the military temperature range (-55°C to +125°C) specify S82S09/19 I, R or F.

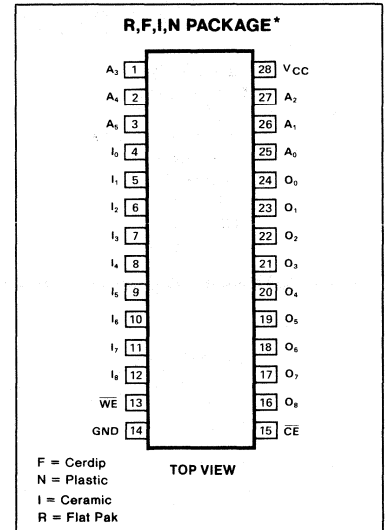
FEATURES

- Address access time:
 - N82S09: 45ns max
 - S82S09: 80ns max
 - N82S19: 35ns max
 - S82S19: 60ns max
- Write cycle time:
 - N82S09/19: 45ns max
 - S82S09: 80ns max
 - S82S19: 70ns max
- Power dissipation: 1.3mW/bit typ
- Input loading:
 - N82S09/19: -100µA max
 - S82S09/19: -150µA max
- On-chip address decoding
- Schottky clamped
- Fully TTL compatible
- 82S09 Output is Non-Blanked During Write
- 82S19 Output is Blanked During Write

APPLICATIONS

- Buffer memory
- Control register
- FIFO memory
- Push down stack
- Scratch pad

PIN CONFIGURATION

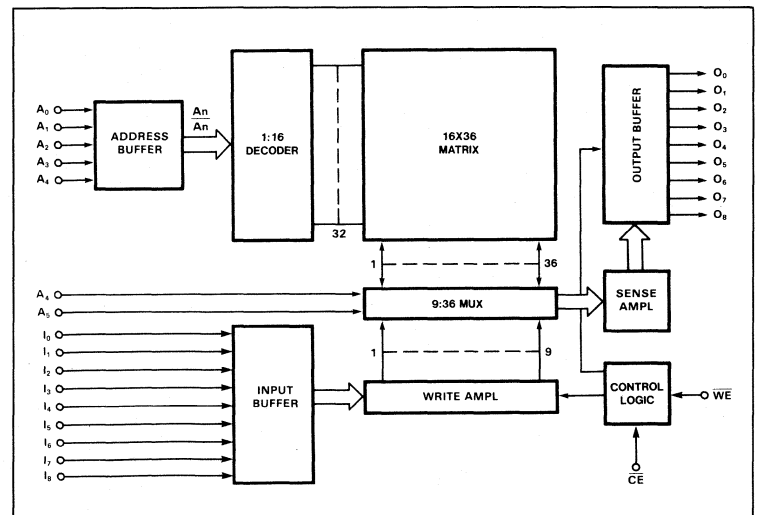


TRUTH TABLE

MODE	CE	WE	I _N	O _N	
				82S09	82S19
Read	0	1	X	Complement of data stored	
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	1
Disabled	1	X	X	1	1

X = Don't care

BLOCK DIAGRAM



576-BIT BIPOLAR RAM (64×9)

82S09/82S19 (O.C.)

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V _{OH}	High	+5.5	
T _A	Temperature range		°C
	Operating		
	N82S09/19	0 to +75	
	S82S09/19	-55 to +125	
T _{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS^{1,7} N82S09/19: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S09/19: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER ¹	TEST CONDITIONS	N82S09/19			S82S09/19			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{IL}	Input voltage Low			.85			.80	V
V _{IH}	Input voltage High				2.2			
V _{IC}	Clamp ²			-1.5			-1.5	
V _{OL}	Output voltage Low ³			0.5			0.5	V
I _{IL}	Input current Low			-100			-150	μA
I _{IH}	Input current High			25			40	μA
I _{OLK}	Output current Leakage ⁴			40			60	μA
I _{CC}	V _{CC} supply current ⁵			190			200	mA
C _{IN}	Capacitance Input		5			5		pF
C _{OUT}	Capacitance Output		8			8		pF

Refer to notes on next page.

576-BIT BIPOLAR RAM (64 × 9)

82S09/82S19 (O.C.)

AC ELECTRICAL CHARACTERISTICS⁷

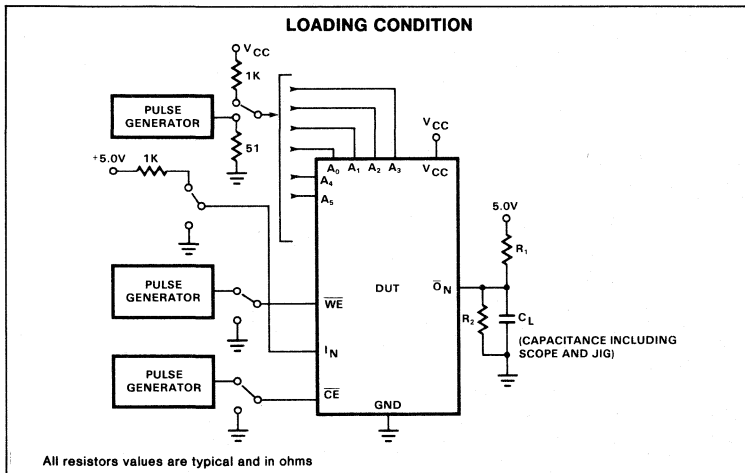
$R_1 = 600\Omega$, $R_2 = 900\Omega$, $C_L = 30\text{pF}$, for 82S09
 $R_1 = 510\Omega$, $R_2 = 750\Omega$, $C_L = 30\text{pF}$, for 82S19
 N82S19: $0^\circ \leq T_A \leq +75^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82S19: $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TO	FROM	N82S09			S82S09			N82S19			S82S19			UNIT
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T_{AA} T_{CE}	Access time Address Chip enable				45			80		35			60	ns	
T_{CD} T_{WD} T_{WR}	Disable time Valid time Write recovery time	Output Output Output			30			50		25			35	ns	
T_{WSA} T_{WHA}	Setup and hold time Setup time Hold time	Write enable	Address	5		10		5		10			ns		
T_{WSD} T_{WHD}	Setup time Hold time	Write enable	Data in	35		5		30		45			ns		
T_{WSC} T_{WHC}	Setup time Hold time	Write enable	\overline{CE}	5		10		5		10			ns		
T_{WP}	Pulse width Write enable ⁶			35		50		35		50			ns		

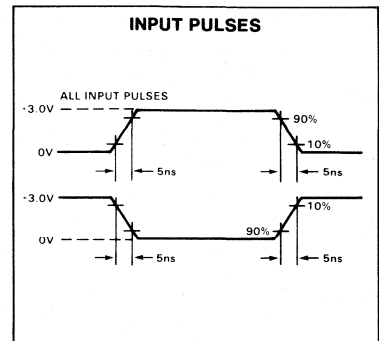
NOTES

- All voltage values are with respect to network ground terminal.
- Test each input one at a time.
- Measured with the logic low stored. Output sink current is supplied through a resistor to V_{CC} .
- Measured with V_{IH} applied to \overline{CE} .
- I_{CC} is measured with the write enable and chip enable input grounded, all other inputs at 4.5V, and the outputs open.
- Minimum required to guarantee a Write into the slowest bit.
- The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.

TEST LOAD CIRCUIT



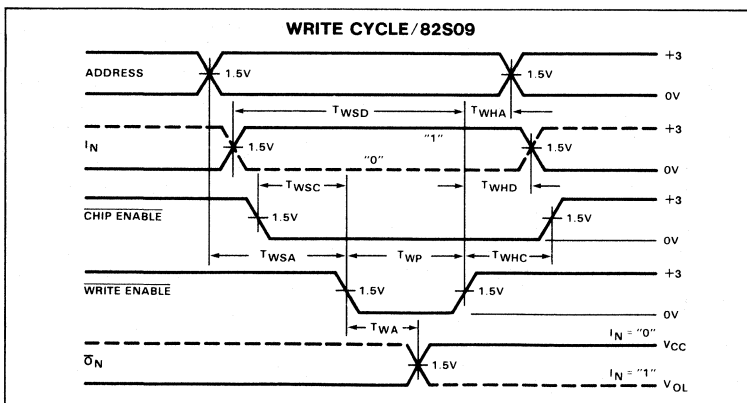
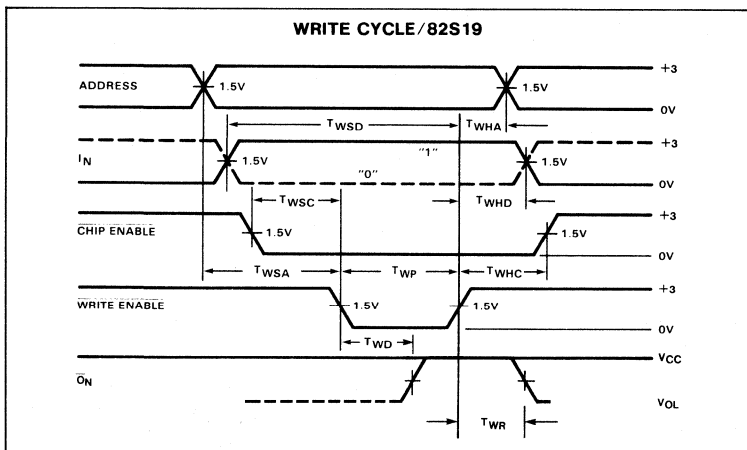
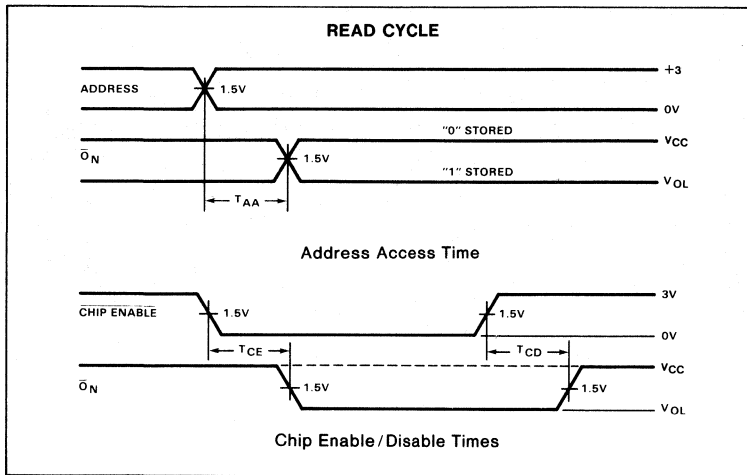
VOLTAGE WAVEFORM



576-BIT BIPOLAR RAM (64x9)

82S09/82S19 (O.C.)

TIMING DIAGRAMS



MEMORY TIMING DEFINITIONS

- T_{CE}** Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
- T_{CD}** Delay between when Chip Enable becomes high and Data Output is in off state.
- T_{AA}** Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.
- T_{WSC}** Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
- T_{WHD}** Required delay between end of Write Enable pulse and end of valid Input Data.
- T_{WP}** Width of Write Enable pulse.
- T_{WSA}** Required delay between beginning of valid Address and beginning of Write Enable pulse.
- T_{WSD}** Required delay between beginning of valid Data Input and end of Write Enable pulse.
- T_{WD}** Delay between beginning of Write Enable pulse and when Data Output goes high (blanks).
- T_{WHA}** Required delay between end of Write Enable pulse and end of valid Address.
- T_{WHC}** Required delay between end of Write Enable pulse and end of valid Address.
- T_{WR}** Delay between end of Write Enable pulse and when Data Output becomes valid. (Assuming address still valid.)
- T_{WA}** Delay between beginning of Write Enable pulse and when data output reflects complement of data input.

2304-BIT BIPOLAR RAM (256 × 9)

82S210 (T.S.)

DESCRIPTION

The 82S210 data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

\overline{WE} causes the present address state to be held in the address latches, independent of any other control signals. A positive pulse on both \overline{L} lines will cause a new address state to be strobed into the latches.

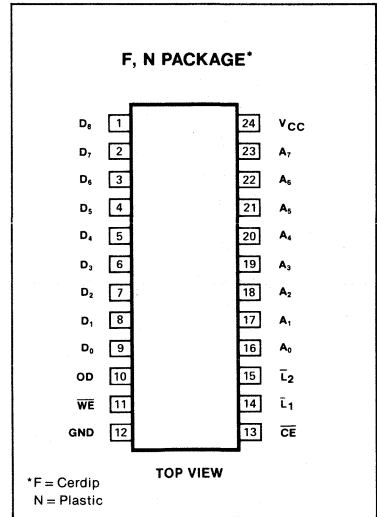
The 82S210 is available in both the commercial and military temperature range. For the commercial temperature range

(0°C to 75°C) specify N82S210F or N and for the military temperature range (-55°C to +125°C) specify S82S210F.

FEATURES

- Access time:
 - Address
 - N82S210: 60ns max
 - S82S210: 90ns max
 - Strobe
 - N82S210: 70ns max
 - S82S210: 100ns max
- On-chip address latches
- Tri-state outputs
- Schottky clamped TTL
- 9th Bit for Parity or Tag

PIN CONFIGURATION

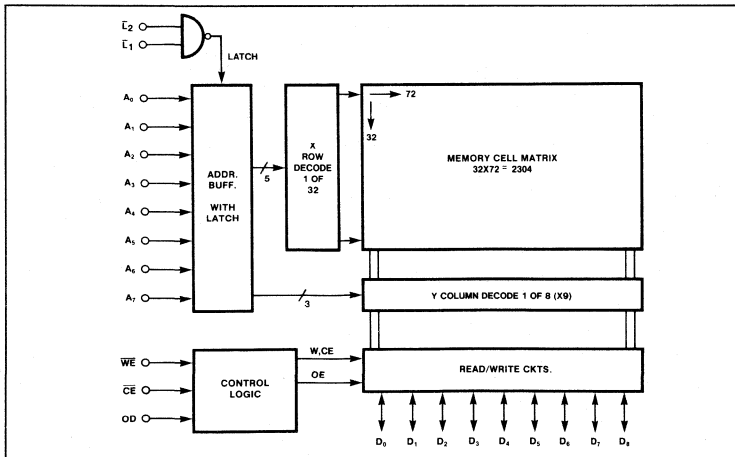


TRUTH TABLE

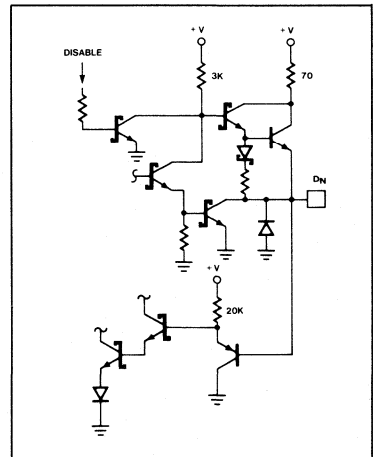
MODE	\overline{WE}	\overline{CE}	OD	\overline{L}_1	\overline{L}_2	\overline{DN} IN/OUT
Disable output	X	X	1	X	X	High Z
Disable R/W	X	1	X	X	X	High Z
Write	0	0	1	X	X	Data in
Read	1	0	0	X	X	Data out
Transparent address	X	X	X	1	1	—
Hold address	X	X	X	0	X	—
Hold address	X	X	X	X	0	—

X = Don't care

BLOCK DIAGRAM



TYPICAL I/O STRUCTURE



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
V _O	Off-state output voltage	+5.5	Vdc
T _A	Temperature range		°C
T _A	Operating	Commercial	0 to +75
		Military	-55 to +125
T _{STG}	Storage	-65 to +150	

2304-BIT BIPOLAR RAM (256 × 9)

82S210 (T.S.)

DC ELECTRICAL CHARACTERISTICS N82S210: 0°C ≤ T_A ≤ 75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S210: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	N82S210			S82S210			UNIT
		Min	Typ	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage ² Low High Clamp ³	V _{CC} = Min V _{CC} = Max V _{CC} = Min, I _{IN} = -12mA			.85	2.2	.80	V
V _{OL} V _{OH}	Output voltage ² Low High	CE, OD = Low, WE = High I _{OUT} = 9.6mA I _{OUT} = -2mA			0.5	2.4	0.5	V
I _{IL} I _{IH}	Input current Low High	V _{IN} = 0.45V V _{IN} + 5.5V			-100 25		-150 40	μA
I _{O (OFF)} I _{OS}	Output current Hi-Z state Short circuit ^{3, 4}	CE = High, V _{OUT} = 5.5V CE = High, V _{OUT} = 0.5V CE = OD = Low, WE = High, V _{OUT} = 0V, Stored High			-20	40 -100 -70	60 -150 -80	
I _{CC}	Supply current		135	185			200	mA
C _{IN} C _{OUT}	Capacitance Input Output	CE = High or OD = High V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V			5 8		5 8	pF

AC ELECTRICAL CHARACTERISTICS¹ R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82S210: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S210: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TO	FROM	N82S210			S82S210			UNIT
			Min	Typ	Max	Min	Typ	Max	
T _{AA}	Address access time	D _N	A _N			60		90	ns
T _{OE} T _{CE}	Output enable time Output enable time	D _N	OD CE	5		35 35		50 50	ns ns
T _{OD} T _{CD}	Output disable time Output disable time	D _N	OD CE			35 35		50 50	ns ns
T _{WP}	Write pulse width		WE	40			60		ns
T _{SA} T _{HA}	Address setup time Address hold time	WE	A _N WE	10 10			15 15		ns ns
T _{SD} T _{HD}	Data setup time Data hold time	WE D _N	D _N WE	35 10			55 15		ns ns
T _{SC} T _{HC}	Chip enable setup time Chip enable hold time	WE CE	CE WE	5 5			10 10		ns ns
T _{SO} T _{HO}	OD setup time OD hold time (To guarantee Hi-Z state during entire write cycle)	CE OD	OD CE	5 5			5 5		ns ns

NOTES

1. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warmup.
2. All voltages are with respect to network ground terminal.
3. Measured on one pin at a time.
4. Duration of test should not exceed one second.

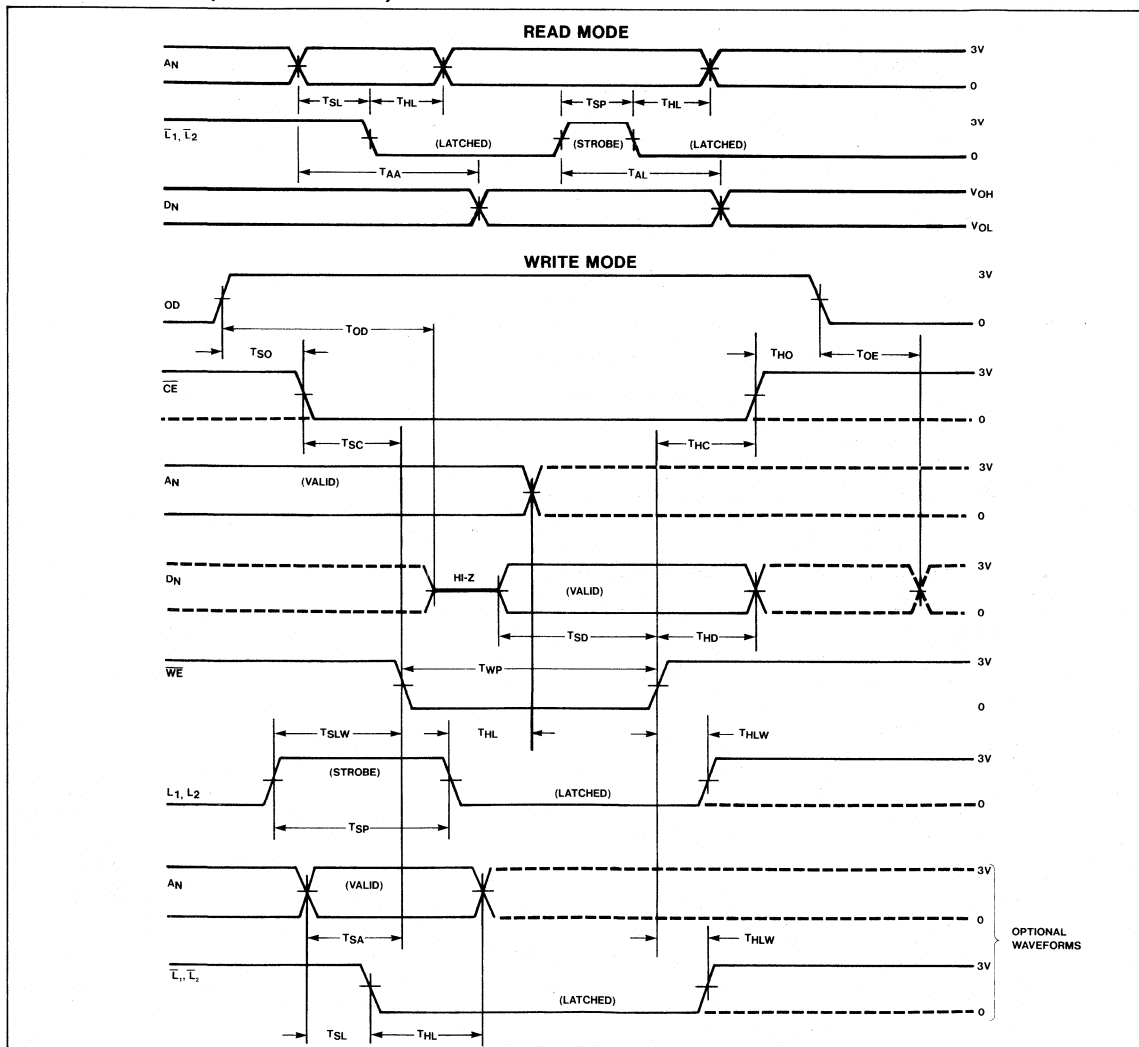
2304-BIT BIPOLAR RAM (256 × 9)

82S210 (T.S.)

AC CHARACTERISTICS (Continued)

PARAMETER	TO	FROM	N82S210			S82S210			UNIT
			Min	Typ	Max	Min	Typ	Max	
T_{SP} Strobe pulse width		\overline{L}	20			30			ns
T_{SL} Latch setup time	\overline{L}	$\overline{A_N}$	5			10			ns
T_{HL} Latch hold time	$\overline{A_N}$	\overline{L}	10			15			ns
T_{SLW} Strobe setup time	\overline{WE}	\overline{L}	15			20			ns
T_{HLW} Latch hold after write	\overline{L}	\overline{WE}	10			15			ns
T_{AL} Strobe access time	$\overline{D_N}$	\overline{L}			70			100	ns

TIMING DIAGRAMS (LATCHED MODE)

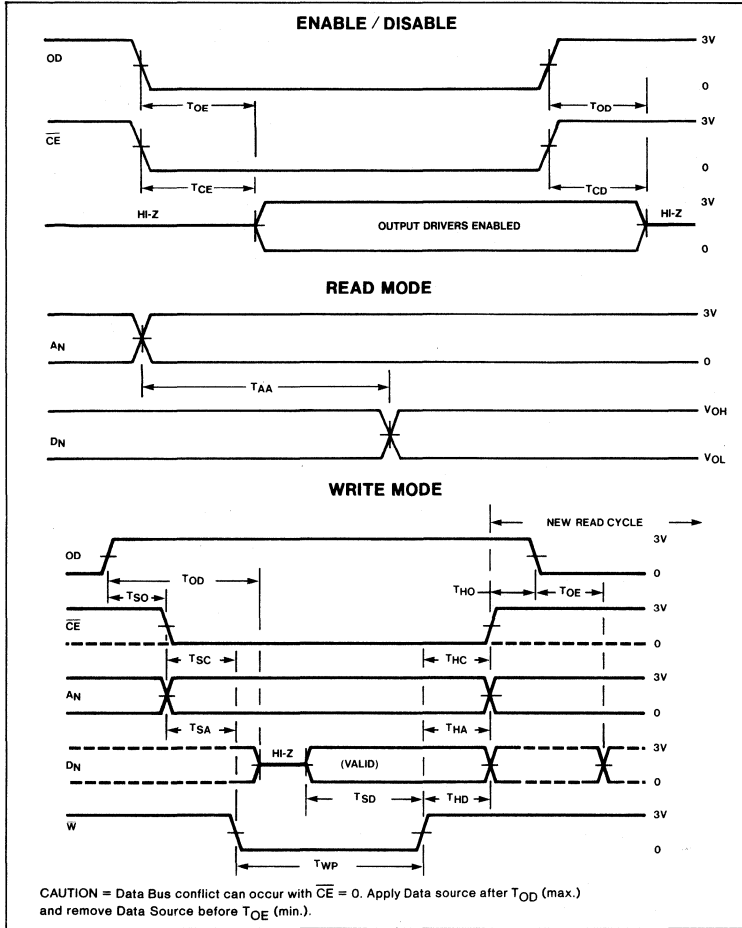


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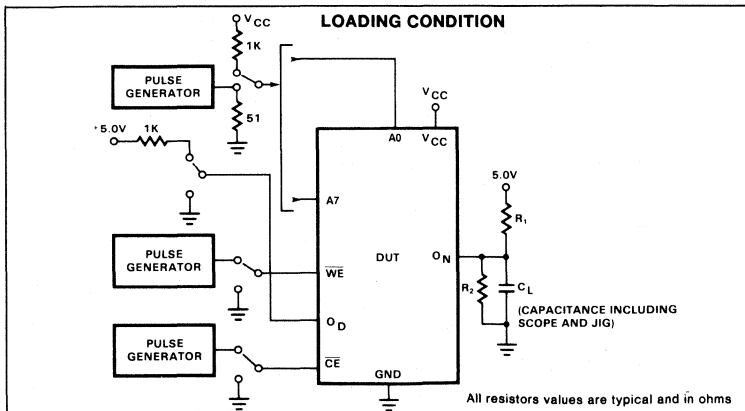
2304-BIT BIPOLAR RAM (256 × 9)

82S210 (T.S.)

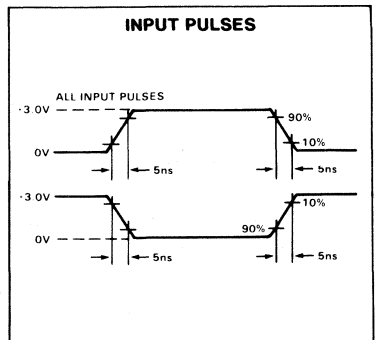
TIMING DIAGRAMS (TRANSPARENT MODE $\overline{L1} = \overline{L2} = 1$)



TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



2304-BIT BIPOLAR RAM (256 × 9)

82S212 (T.S.)

DESCRIPTION

The organization of the 82S212 allows the byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used as a tag for each word stored. The 82S212 is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which space and performance requirements dictate a wide data path in favor of word depth.

The 82S212 data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

The 82S212 is available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to 75°C) specify N82S212F or N and for the military temperature range (-55°C to +125°C) specify S82S212F.

FEATURES

- **Address access time:**
N82S212: 45ns max
S82S212: 70ns max
- **Power dissipation:** 0.3mW/bit
- **Tri-state outputs**
- **Schottky clamped TTL**

APPLICATIONS

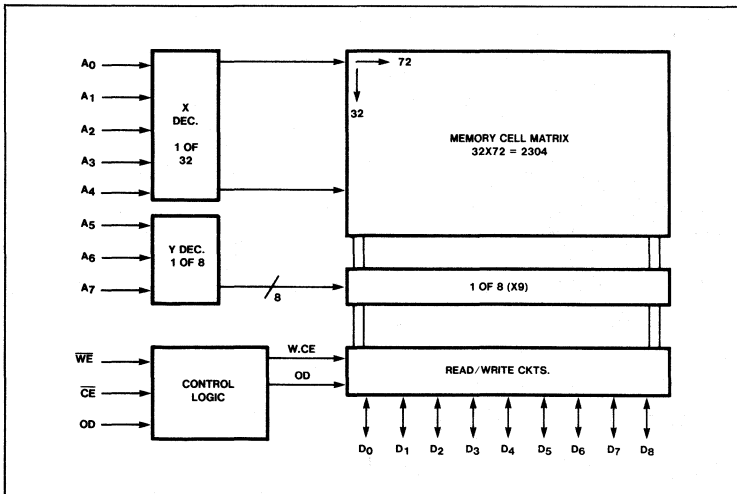
- **Cache memory**
- **Buffer storage**
- **Writable control store**

TRUTH TABLE

MODE	WE	CE	OD	DN IN/OUT
Disable output	X	X	1	High Z
Disable R/W	X	1	X	High Z
Write	0	0	1	Data in
Read	1	0	0	Data out

X = Don't care

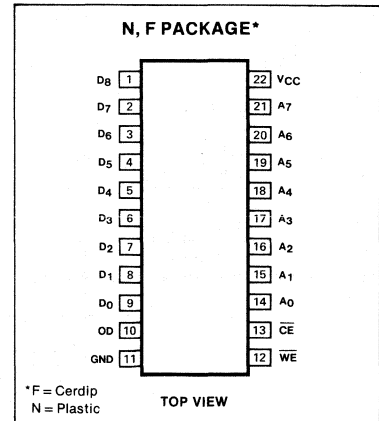
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

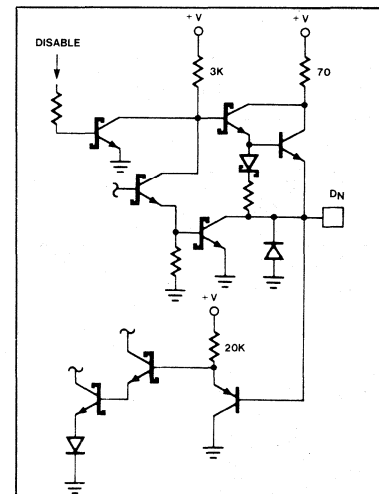
PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	+7
V _{IN}	Input voltage	+5.5
V _O	Off-state output voltage	+5.5
T _A	Operating Temperature range	°C
	Commercial	0 to +75
	Military	-55 to +125
T _{STG}	Storage	-65 to +150

PIN CONFIGURATION



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TYPICAL I/O STRUCTURE



2304-BIT BIPOLAR RAM (256 × 9)

82S212 (T.S.)

DC ELECTRICAL CHARACTERISTICS¹ N82S212: 0 °C ≤ T_A ≤ + 75 °C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S212: - 55 °C ≤ T_A ≤ + 125 °C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER ¹	TEST CONDITIONS	N82S212			S82S212			UNIT			
		Min	Typ	Max	Min	Typ	Max				
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp ²	V _{CC} = Min V _{CC} = Max V _{CC} = Min, I _{IN} = - 12mA			2.0		.85 - 1.5	2.2		.80 - 1.5	V
V _{OL}	Output voltage Low ³	V _{CC} = Min, I _{OL} = 8.0mA					0.5			0.5	V
I _{IL} I _{IH}	Input current Low High	V _{IN} = 0.45V V _{IN} = 5.5V					- 100 25			- 150 40	μA
I _{O (OFF)} I _{OS}	Output current Hi-Z state Short circuit ^{4, 5}	CE = High or OD = High, V _{OUT} = 5.5V CE = High or OD = High, V _{OUT} = 0.5V CE = OD = Low, V _{OUT} = 0V			- 20		40 - 100 - 70	- 15		60 - 100 - 80	μA mA
I _{CC}	V _{CC} supply current ⁵	V _{CC} = Max				135	185			200	mA
C _{IN} C _{OUT}	Capacitance Input Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V				5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS¹ R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82S212: 0 °C ≤ T_A ≤ + 75 °C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S212: - 55 °C ≤ T_A ≤ + 125 °C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TO	FROM	N82S212			S82S212			UNIT	
			Min	Typ ³	Max	Min	Typ ³	Max		
T _{AA}	Access time Address	Output	Address			45			70	ns
T _{OE} T _{CE}	Enable time Output Output	Output Output	OD Chip enable	5		25 25			50 50	ns
T _{OD} T _{CD}	Disable time Output Output	Output Output	OD Chip enable			25 25			50 50	ns
T _{WP}	Pulse width Write			25			45			ns
T _{WSC} T _{WHD}	Setup time Hold time	Write Chip enable	Chip enable Write	5 5			10 10			
T _{WSD} T _{WHD}	Setup time Hold time	Write Data	Data Write	25 5			45 5			
T _{WSA} T _{WHA}	Setup time Hold time	Write Address	Address Write	5 5			10 15			
T _{SO} T _{HO}	Setup time (from disabled state) Hold time	Chip enable OD	OD Chip enable	5 5			5 5			

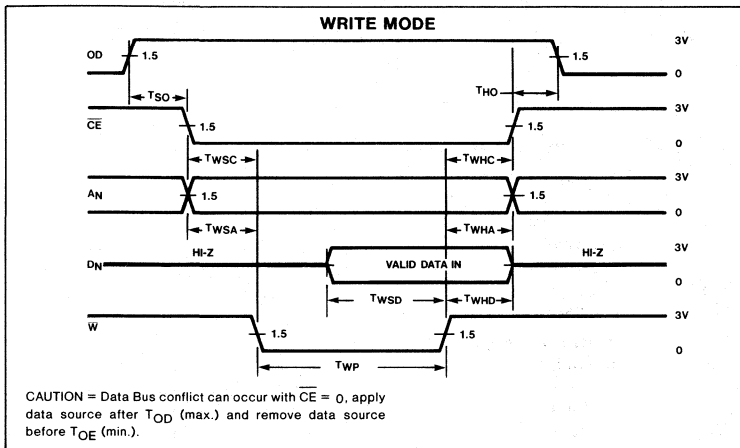
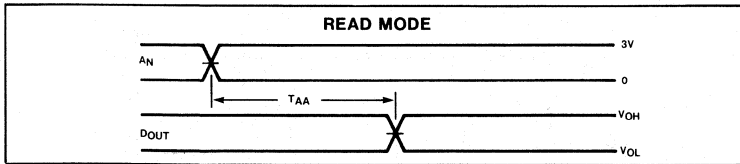
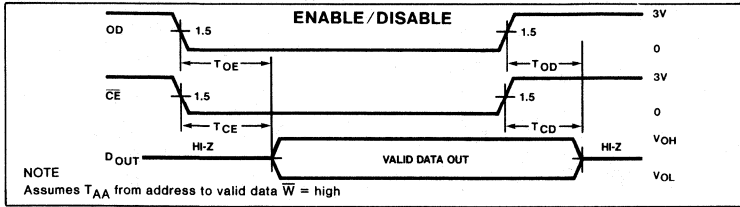
NOTES

- The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2 minute warmup.
- All voltages are with respect to network ground terminal.
- All typical values are at V_{CC} = 5V, T_A = 25 °C.
- Measured on one pin at a time.
- Duration of I_{OS} test should not exceed one second.

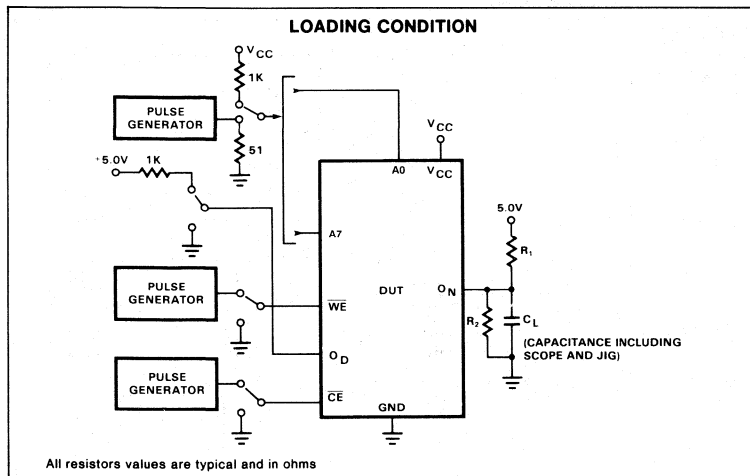
2304-BIT BIPOLAR RAM (256 × 9)

82S212 (T.S.)

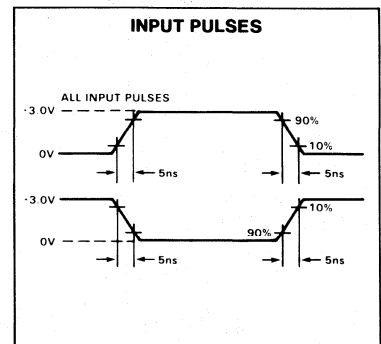
TIMING DIAGRAMS



TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



5

2048-BIT BIPOLAR RAM (256 × 8)

8X350 (T.S.)

DESCRIPTION

The 8X350 bipolar RAM is designed principally as a working storage element in an 8X300 based system. Internal circuitry is provided for direct use in 8X300 applications. When used with the 8X300, the RAM address and data buses are tied together and connected to the IV bus of the system.

The data inputs and outputs share a common I/O bus with 3-state outputs.

The 8X350 is available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N8X350-F, and for the military temperature range (-55°C to +125°C) specify S8X350-F.

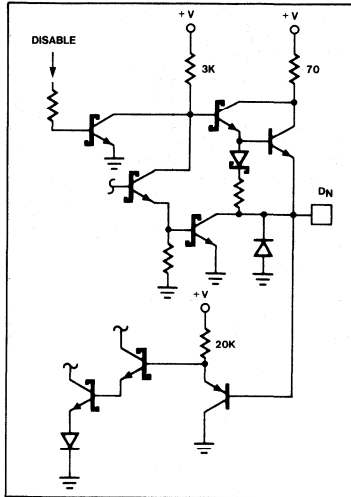
FEATURES

- On-chip address latches
- 3-state outputs
- Schottky clamped TTL
- Internal control logic for 8X300 system
- Directly interfaces with the 8X300 bipolar microprocessor with no external logic
- May be used on left or right bank

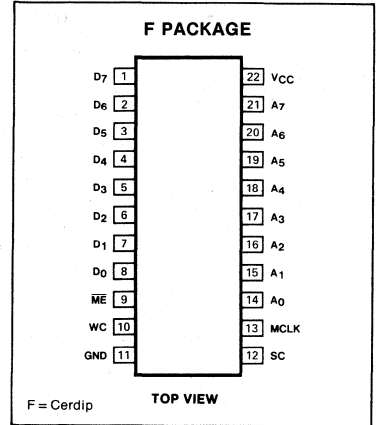
APPLICATIONS

- 8X300 or 8X305 working storage

TYPICAL I/O STRUCTURE



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

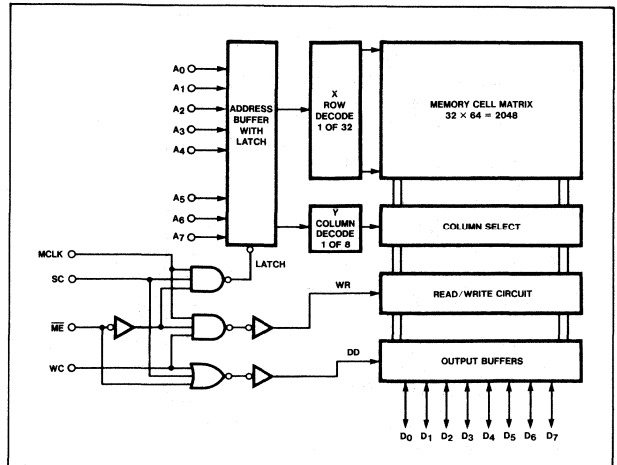
PARAMETER	RATING	UNIT	
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V _{OH}	High	+5.5	
V _O	Off-state	+5.5	
T _A	Temperature range		°C
	Operating	0 to +75	
	Commercial		
	Military	-55 to +125	
T _{STG}	Storage	-65 to +150	

TRUTH TABLE

Note X = Don't care

MODE	ME	SC	WC	MCLK	BUSSED DATA/ADDRESS LINES
Hold address					
Disable data out	1	X	X	X	High Z data out
Input new address	0	1	0	1	Address High Z
Hold address					
Disable data out	0	1	0	0	High Z data out
Hold address					
Write data	0	0	1	1	Data in
Hold address					
Disable data out	0	0	1	0	High Z data out
Hold address					
Read data	0	0	0	X	Data out
Undefined state ¹²	0	1	1	1	—
Hold address ¹²					
Disable data out	0	1	1	0	High Z data out

BLOCK DIAGRAM



2048-BIT BIPOLAR RAM (256 × 8)

8X350 (T.S.)

DC ELECTRICAL CHARACTERISTICS² N8X350: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S8X350: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TEST CONDITIONS	N8X350			S8X350			UNIT	
		Min	Typ	Max	Min	Typ	Max		
V _{IL} V _{IH} V _{IC}	Input voltage Low ¹ High ¹ Clamp ^{1,3}	V _{CC} = Min V _{CC} = Max V _{CC} = Min, I _{IN} = -12mA			2.0		.85 -1.2	2.0 -1.2	V
V _{OL} V _{OH}	Output voltage Low ^{1,4} High ^{1,5}	V _{CC} = Min I _{OL} = 9.6mA I _{OH} = -2mA			2.4		0.5 2.4	.5	V
I _{IL} I _{IH}	Input current Low High	V _{IN} = 0.45V V _{IN} = 5.5V					-100 25	-150 50	μA
I _{O(OFF)} I _{OS}	Output current High Z state Short circuit ^{3,6}	M _E = High, V _{OUT} = 5.5 V M _E = High, V _{OUT} = 0.5 V SC = WC, M _E = Low, V _{OUT} = 0V, Stored High			-20		40 -100	60 -100	μA μA
I _{CC}	V _{CC} supply current ⁷	V _{CC} = Max					185	200	mA
C _{IN} C _{OUT}	Capacitance Input Output	M _E = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V				5 8		5 8	pF

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AC ELECTRICAL CHARACTERISTICS^{2,9} N8X350: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 S8X350: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

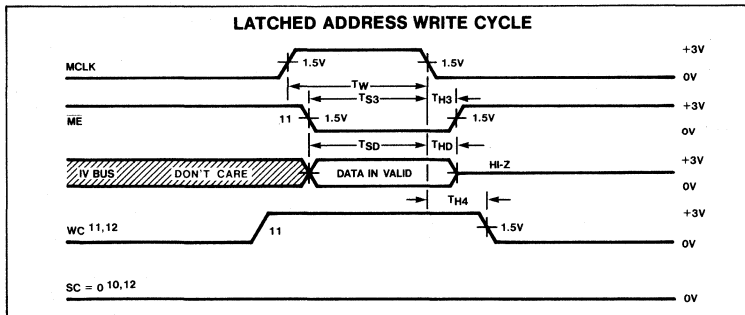
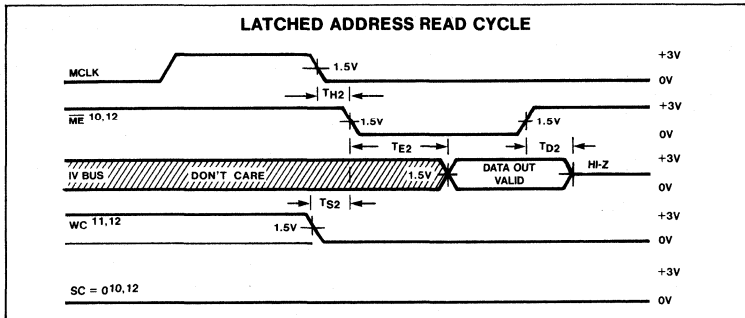
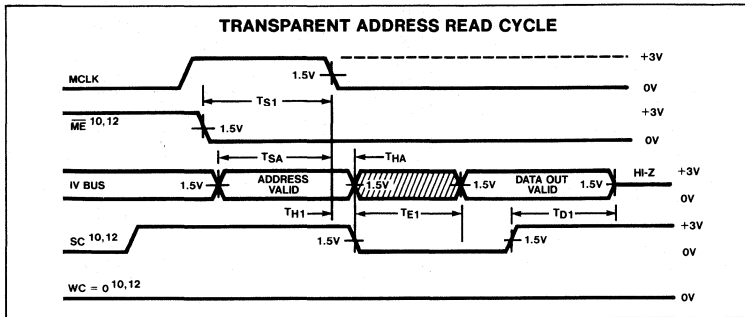
PARAMETER	TO	FROM	N8X350			S8X350			UNIT
			Min	Typ	Max	Min	Typ	Max	
T _{E1} T _{E2}	Enable time Output Output	Data out Data out	SC- M _E -			35 35		40 40	ns
T _{D1} T _{D2}	Disable time Output Output	Data out Data out	SC+ M _E +			35 35		40 40	ns
T _W	Pulse width Master clock ⁸			40			50		ns
T _{SA} T _{HA} T _{SD} T _{HD} T _{S3} T _{H3} T _{S1} T _{H2} T _{S2} T _{H1} T _{H4}	Setup and hold time Setup time Hold time Setup time Hold time Setup time Hold time Setup time Hold time Setup time Hold time Setup time Hold time	MCLK- Address MCLK- Data in MCLK- M _E - M _E + MCLK- M _E - M _E - MCLK- M _E - M _E - SC-, WC- SC- WC-	Address MCLK- Data in MCLK- M _E - MCLK- M _E - MCLK- M _E - MCLK- M _E - MCLK- M _E - MCLK- M _E - MCLK- M _E -	30 5 35 5 40 5 30 5 5 0 5 5 5 5			40 10 45 10 50 5 40 5 5 5 5 5 5		ns

Notes on following page.

2048-BIT BIPOLAR RAM (256 × 8)

8X350 (T.S.)

TIMING DIAGRAMS



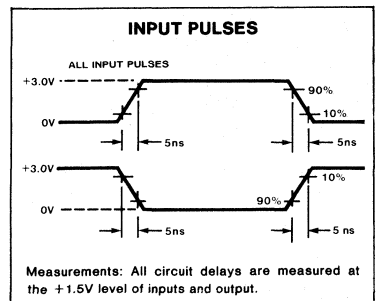
NOTES

1. All voltage values are with respect to network ground terminal.
2. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
Typical thermal resistance values of the package at maximum temperature are:
 θ_{JA} junction to ambient at 400fpm air flow - 50°C/watt
 θ_{JA} junction to ambient - still air - 90°C/watt
 θ_{JA} junction to case - 20°C/watt
3. Test each pin one at a time.
4. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC} .
5. Measured with a logic high stored.
6. Duration of the short circuit should not exceed 1 second.
7. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V and the output open.
8. Minimum required to guarantee a Write into the slowest bit.
9. Applied to the 8X300 based system with the data and address pins tied to the IV Bus.
10. $SC + \overline{ME} = 1$ to avoid bus conflict.
11. $WC + \overline{ME} = 1$ to avoid bus conflict.
12. The SC and WC outputs from the 8X300 are never at 1 simultaneously.

TIMING DEFINITIONS

- TS1** Required delay between beginning of Master Enable low and falling edge of Master Clock.
- TSA** Required delay between beginning of valid address and falling edge of Master Clock.
- THA** Required delay between falling edge of Master Clock and end of valid Address.
- TH1** Required delay between falling edge of Master Clock and when Select Command becomes low.
- TE1** Delay between beginning of Select Command low and beginning of valid data output on the IV Bus.
- TD1** Delay between when select Command becomes high and end of valid data output on the IV Bus.
- TH2** Required delay between falling edge of Master Clock and when Master Enable becomes low.
- TE2** Delay between when Master Enable becomes low and beginning of valid data output on the IV Bus.
- TD2** Delay between when Master Enable becomes high and end of valid data output on the IV Bus.
- TS2** Required delay between when Select Command or Write Command becomes low and when Master Enable becomes low.
- Tw** Minimum width of the Master Clock pulse.
- TS3** Required delay between when Master Enable becomes low and falling edge of Master Clock.
- TH3** Required delay between falling edge of Master Clock and when Master Enable becomes high.
- TSD** Required delay between beginning of valid data input on the IV Bus and falling edge of Master Clock.
- THD** Required delay between falling edge of Master Clock and end of valid data input on the IV Bus.
- TH4** Required delay between falling edge of Master Clock and when Write Command becomes low.

VOLTAGE WAVEFORM



Section 6
RAMs,
ECL

1024-BIT ECL RAM (1024 × 1)

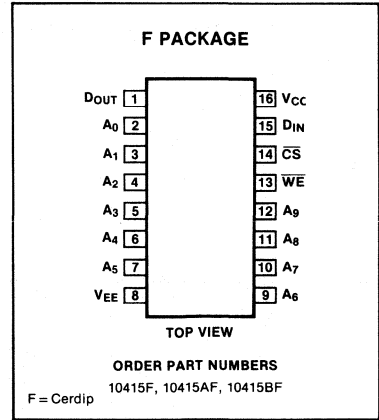
10415/10415A/10415B

DESCRIPTION

The 10415 device is a 1024-word by 1-bit, fully encoded ECL Read/Write Random Access Memory designed for high speed scratch pad, control, and buffer storage applications. The device also includes full address decoding on-chip, separate data in and noninverting data out lines, an active LOW chip select.

- **Address access times:**
 - 10415: 20ns max
 - 10415A: 15ns max
 - 10415B: 10ns max
- **Low power dissipation of 0.7mW/bit typical**
- **Blanked outputs**

PIN CONFIGURATION



FEATURES

- **Organization:** 1024 words x 1 bit
- **Fully compatible with 10K ECL families**
- **Operating temperature:** 0°C to +75°C

APPLICATIONS

- **Buffer memory**
- **Scratch pad memory**
- **Writeable microcode store**

ABSOLUTE MAXIMUM RATINGS

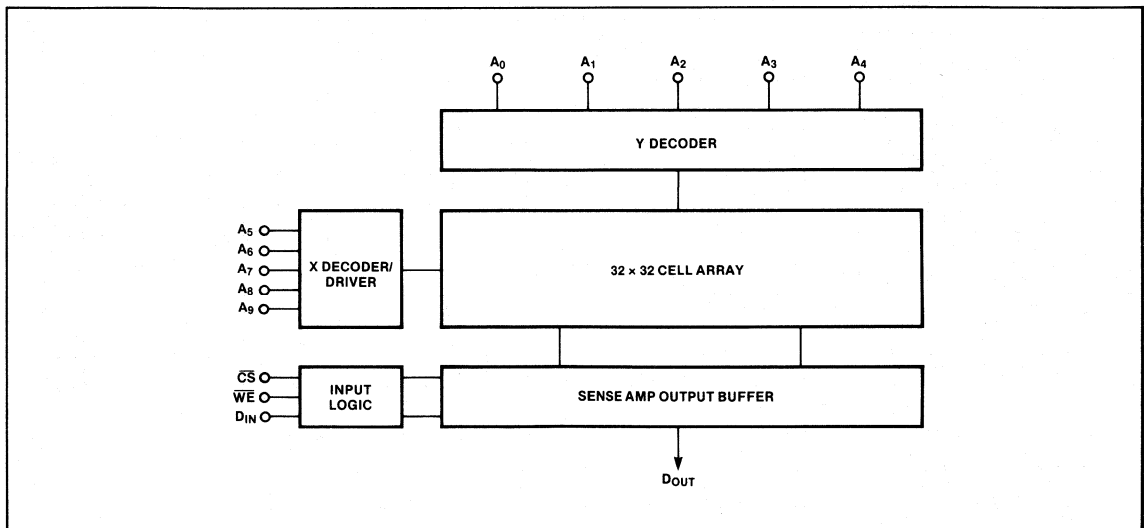
PARAMETER	RATING	UNIT
V _{EE} Supply voltage	- 7	Vdc
V _O Output voltage	+ 0.5 to V _{EE}	Vdc
I _O Output current	- 30	mA
T _A Operating	0 to +75	°C
T _{stg} Storage	- 55 to + 150	°C

TRUTH TABLE

INPUTS			OUTPUT	MODE
CS	WE	DI		
H	X	X	L	Disable
L	H	X	D _{OUT}	Read
L	L	H	L	Write 1
L	L	L	L	Write 0

H = HIGH voltage level
L = LOW voltage level
X = Don't care

BLOCK DIAGRAM



1024-BIT ECL RAM (1024 × 1)

10415/10415A/10415B

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.25V \pm 5\%$, Output load 50Ω to $-2V$, $0^\circ C \leq T_A \leq 75^\circ C$

PARAMETER	TEST CONDITIONS	0°C		+25°C		+75°C		UNIT
		Min	Max	Min	Max	Min	Max	
Input voltage V_{IH} HIGH V_{IL} LOW V_{IHA} Threshold HIGH V_{ILA} Threshold LOW								V
		-1.870	-0.840	-1.850	-0.810	-1.830	-0.720	
		-1.145		-1.105		-1.045		
			-1.490		-1.475		-1.450	
Output voltage V_{OH} HIGH V_{OL} LOW V_{OHA} Threshold HIGH V_{OLA} Threshold LOW	$V_{IH} = \text{MAX}$	-1.0	-0.840	-0.960	-0.810	-0.900	-0.720	V
	$V_{IL} = \text{MIN}$	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	
	V_{IHA}	-1.020		-0.980		-0.900		
	V_{ILA}		-1.645		-1.630		-1.605	
Input current I_{IH} HIGH I_{IL} LOW I_{IL} CS	$V_{IH} = \text{MAX}$		220		220		220	μA
	$V_{IL} = \text{MIN}$	-6		-6		-6		
	$V_{IL} = \text{MIN}$	10		10		10		
I_{EE} Supply current	$V_{IL} = \text{MIN}$		150		150		150	mA
Capacitance C_{IN} Input C_{OUT} Output					5			μF
					5			

NOTES

1. Voltages are defined with respect to ground, pin 16.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow >400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $0^\circ C \leq T_A \leq +75^\circ C$, $R_L = 50\Omega$ to $-2V$

PARAMETER	10415			10415A			10415B			UNIT
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T_{AA} Address access time			20			15			10	ns
T_{BD} Chip select recovery time			5			5			5	ns
T_{BS} Chip select access time			5			5			5	ns
T_{WD} Write disable time ¹			6			6			6	ns
T_{WP} Write pulse width	12			10			8			ns
T_{WR} Write recovery time ¹		4.5	10		4.5	10		4.5	10	ns
T_{WHA} Address hold time ¹	3	0		3	0		3	0		ns
T_{WHC} Chip select hold time ¹	2	0		2	0		2	0		ns
T_{WHD} Data hold time ¹	2	0		2	0		2	0		ns
T_{WSA} Address setup time ¹	1	0		1	0		1	0		ns
T_{WSC} Chip select setup time ¹	2	0		2	0		2	0		ns
T_{WSD} Data setup time ¹	2	0		2	0		2	0		ns
t_f Output fall time ²	0.5	2		0.5	2		0.5	2		ns
t_r Output rise time ²	0.5	2		0.5	2		0.5	2		ns

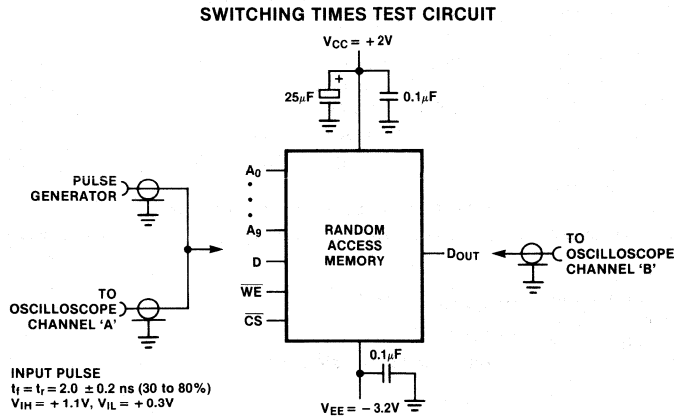
NOTES

1. To guarantee a write into the slowest bit.
2. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudo-random testing pattern.
3. AC limits apply after thermal equilibrium has been established.
4. Unit is in a test socket or mounted on a printed circuit board with transverse air flow >400 ft/min.
5. Setup and hold times are guaranteed for $T_W \geq T_W \text{ MIN}$.
6. All propagation measurements to output are measured from 50% of the input pulse to a valid output level ($V_{IH} \text{ MIN}$ or $V_{IL} \text{ MAX}$).
7. Typical values are at $V_{EE} = -5.2V$, $T_A = 25^\circ C$ and maximum loading.

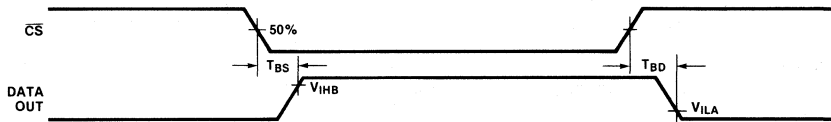
1024-BIT ECL RAM (1024 × 1)

10415/10415A/10415B

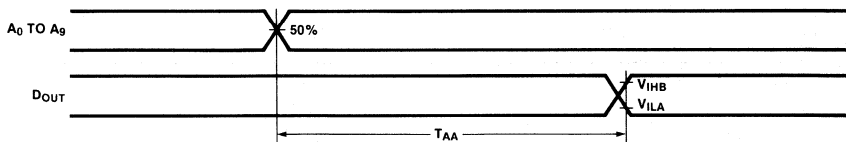
SWITCHING TIMES TEST CIRCUIT AND TIMING DIAGRAMS



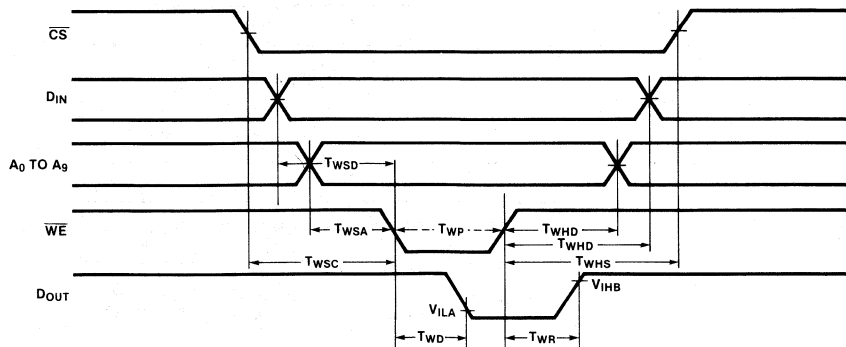
READ MODE PROPAGATION DELAY FROM CHIP SELECT



READ MODE PROPAGATION DELAY FROM ADDRESS



WRITE MODE



1024-BIT ECL RAM (256 × 4)

10422/10422A/10422B

DESCRIPTION

The 10422 device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high speed scratch pad, control, and buffer storage applications. The 10422 is available in a slim line 24-pin dual-in-line, flat or leadless package. This circuit may be reconfigured as 512 × 2 or 1024 × 1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The Open Emitter outputs have a 50Ω drive capability. The input pull-down resistor to V_{CC} is 50,000Ω typical for the block selects.

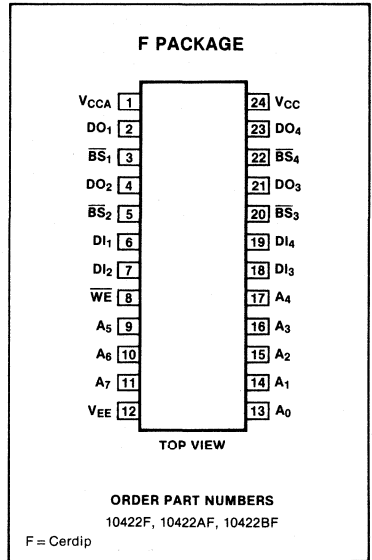
FEATURES

- 256 words × 4 bits organization
- Fully compatible with 10K series ECL families
- Address access times:
 - 10422: 20ns max
 - 10422A: 15ns max
 - 10422B: 10ns max
- Low power dissipation of 0.8mW/bit
- Operating temperature: 0°C to +75°C (ambient)
- Block select allows variable organization

APPLICATIONS

- High speed scratch pad
- Control and buffer storage

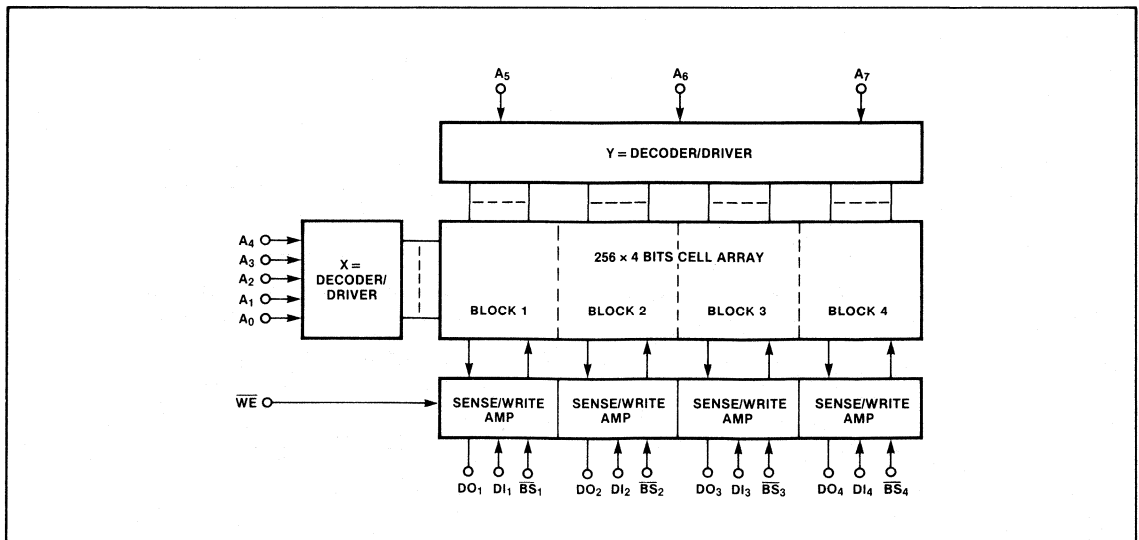
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{EE} Supply voltage	- 7	Vdc
V _{IN} Input voltage	0 to V _{EE}	Vdc
I _O Output source current temperature range	- 30	mAdc
T _A Operating	0 to + 75	°C
T _J Operating junction	125	°C
T _{stg} Storage	- 55 to + 150	°C

BLOCK DIAGRAM



1024-BIT ECL RAM (256 × 4)

10422/10422A/10422B

DC ELECTRICAL CHARACTERISTICS $V_{EE} = -5.2V \pm 5\%$, Output load 50Ω to -2V, $0^\circ C \leq T_A \leq +75^\circ C$

PARAMETER	TEST CONDITIONS	0°C		+25°C		+75°C		UNIT
		Min	Max	Min	Max	Min	Max	
Input voltage V_{IH} HIGH V_{IL} LOW V_{IHA} Threshold HIGH V_{ILA} Threshold LOW								V
		-1.870	-0.840	-1.850	-0.810	-1.830	-0.720	
		-1.145		-1.105		-1.045		
			-1.490		-1.475		-1.450	
Output voltage V_{OH} HIGH V_{OL} LOW V_{OHA} Threshold HIGH V_{OLA} Threshold LOW	$V_{IH} = \text{MAX}$	-1.0	-0.840	-0.960	-0.810	-0.900	-0.720	V
	$V_{IL} = \text{MIN}$	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	
	V_{IHA}	-1.020		-0.980		-0.900		
	V_{ILA}		-1.645		-1.630		-1.605	
Input current I_{IH} HIGH I_{IL} LOW I_{IL} \overline{BS}	$V_{IH} = \text{MAX}$		220		220		220	μA
	$V_{IL} = \text{MIN}$	-6		-6		-6		
	$V_{IL} = \text{MIN}$	10		10		10		
I_{EE} Supply current	$V_{IL} = \text{MIN}$		195		195		195	mA
Capacitance C_{IN} Input C_{OUT} Output							8	pF
							8	

NOTES

1. Voltages are defined with respect to ground, pins 1 and 24.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to -2V, $0^\circ C \leq T_A \leq +75^\circ C$

PARAMETER	10422			10422A			10422B			UNIT
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T_{AA} Address access time			20			15			10	ns
T_{BD} Block select recovery time			5			5			5	ns
T_{BS} Block select access time			5			5			5	ns
T_{WD} Write disable time ¹			5			5			5	ns
T_{WP} Write pulse width	12			10			8			ns
T_{WR} Write recovery time ¹		4.5	9		4.5	9		4.5	9	ns
T_{WHA} Address hold time ¹	5	0		5	0		5	0		ns
T_{WHC} Block select hold time ¹	4	0		4	0		4	0		ns
T_{WHD} Data hold time ¹	4	0		4	0		4	0		ns
T_{WSA} Address setup time ¹	2	0		2	0		2	0		ns
T_{WSC} Block select setup time ¹	3	0		3	0		3	0		ns
T_{WSD} Data setup time ¹	3	0		3	0		3	0		ns
t_f Output fall time ²		2			2			2		ns
t_r Output rise time ²		2			2			2		ns

NOTES

1. To guarantee a write into the slowest bit.
2. Measured between 20% and 80% points.
3. AC limits apply after thermal equilibrium has been established.
4. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
5. Setup and hold times are guaranteed for $T_W \geq T_{W \text{ MIN}}$.
6. After propagation measurements to output are measured from 50% of the input pulse to a valid output level ($V_{IH \text{ MIN}}$ or $V_{IL \text{ MAX}}$).
7. Typical values are at $V_{EE} = -5.2V$, $T_A = 25^\circ C$ and maximum loading.



1024-BIT ECL RAM (256 × 4)

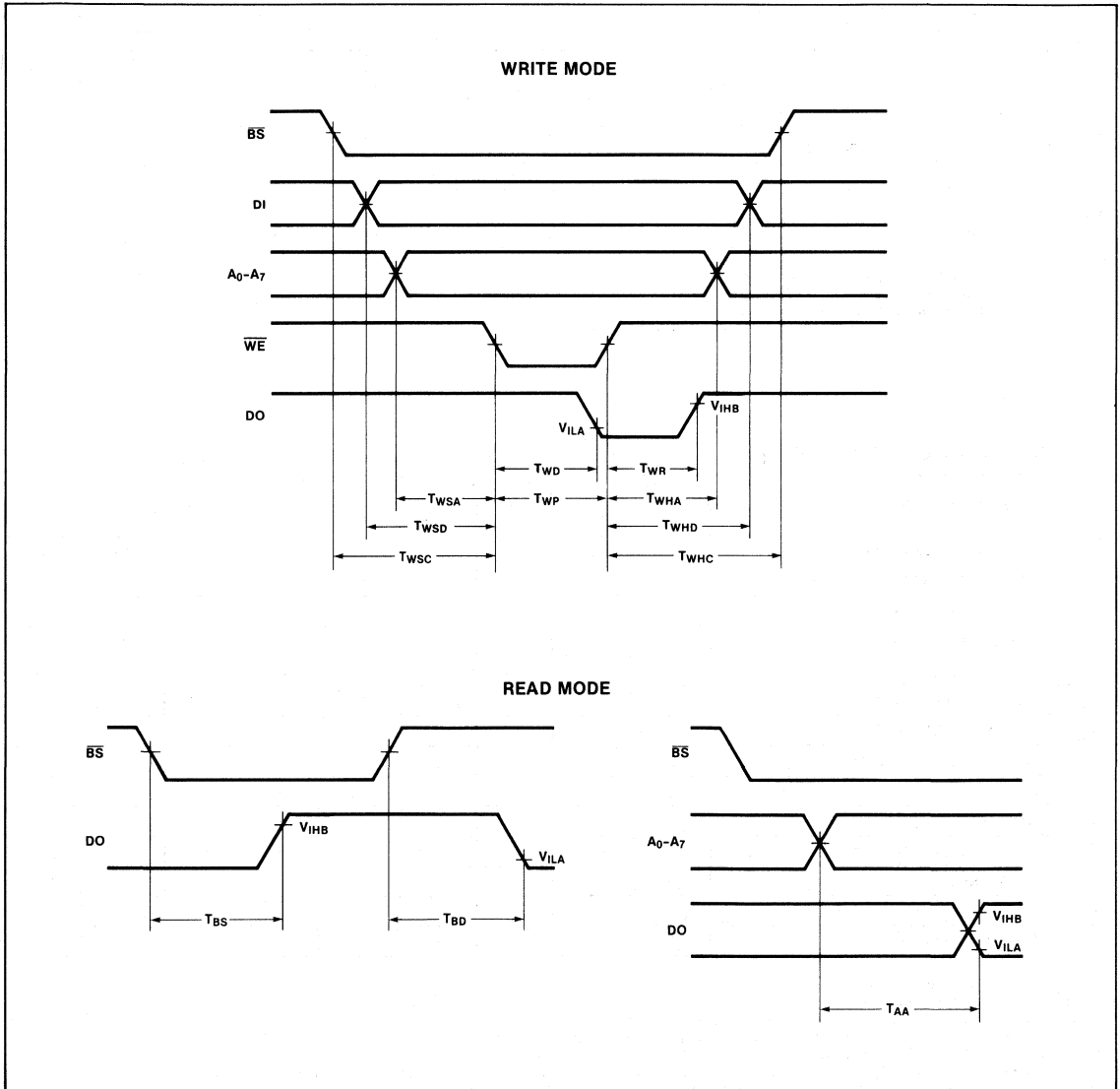
10422/10422A/10422B

TRUTH TABLE (Positive Logic)

INPUTS			OUTPUT	MODE
\overline{BS}_N	\overline{WE}	DI_N	DO_N	
H	X	X	L	Disable
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 N = Blocks 1-4

TIMING DIAGRAMS



4096-BIT ECL RAM (4096 × 1)

10470/10470A

DESCRIPTION

The 10470/10470A device is a 4096 words by 1 bit fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines, and an active LOW Chip Select input.

The 10470/10470A is compatible with the 10K ECL families and includes on-chip voltage compensation for improved noise margin.

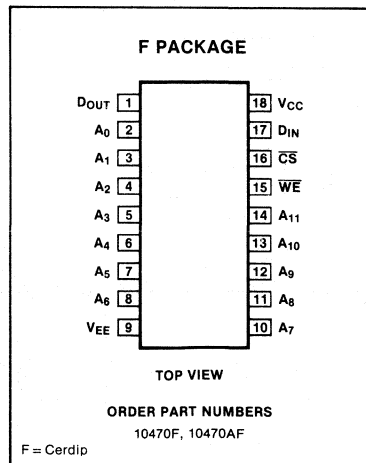
The device is specified with two different read cycle times:

- 10470 : 35ns max
- 10470A: 25ns max

FEATURES

- **Organization:** 4096 words by 1 bit
- **Fully compatible with 10K ECL families**
- **Operating temperature:** 0°C to +75°C
- **Address access times:**
 - 10470: 35ns max
 - 10470A: 25ns max
- **Low supply current of 150mA max**

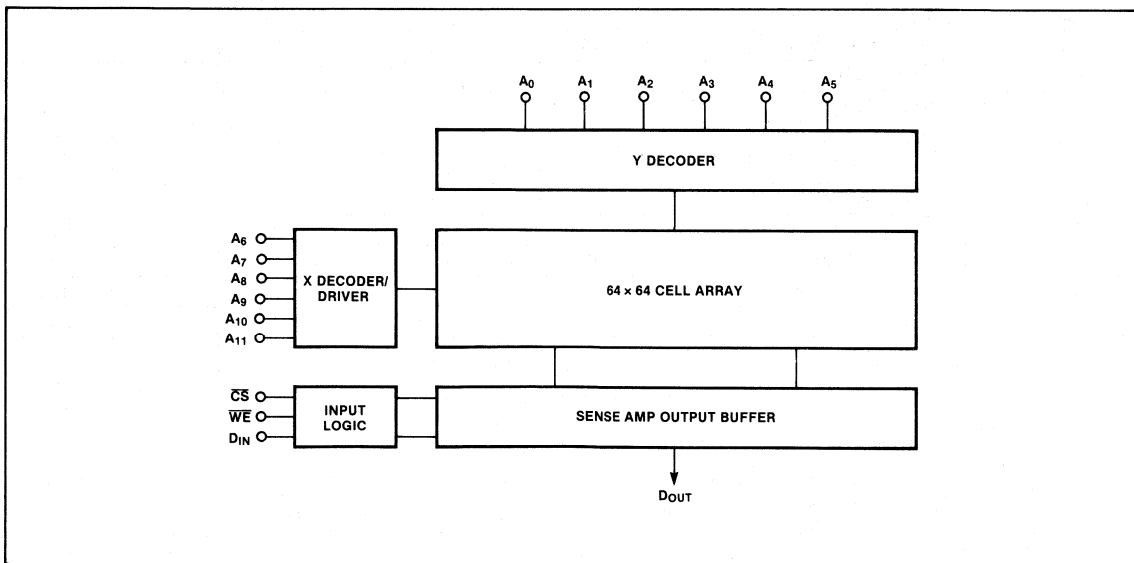
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{EE} Supply voltage	-7	Vdc
V _{IN} Input voltage	+0.5 to V _{EE}	Vdc
I _O Output current	-30	mA
T _A Operating	0 to +75	°C
T _{stg} Storage	-55 to +150	°C

BLOCK DIAGRAM



4096-BIT ECL RAM (4096 × 1)

10470/10470A

DC ELECTRICAL CHARACTERISTICS $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $0^\circ C \leq T_A \leq +75^\circ C$

PARAMETER	TEST CONDITIONS	0°C		+25°C		+75°C		UNIT	
		Min	Max	Min	Max	Min	Max		
V_{IH} V_{IL} V_{IHA} V_{ILA}	Input voltage HIGH LOW Threshold HIGH Threshold LOW		-0.840		-0.810		-0.720	V	
		-1.870		-1.850		-1.830			
		-1.145		-1.105		-1.045			
			-1.490		-1.475		-1.450		
V_{OH} V_{OL} V_{OHA} V_{OLA}	Output voltage HIGH LOW Threshold HIGH Threshold LOW	$V_{IH} = \text{MAX}$	-1.0	-0.840	-0.960	-0.810	-0.900	-0.720	V
		$V_{IL} = \text{MIN}$	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	
		V_{IHA}	-1.020		-0.980		-0.900		
		V_{ILA}		-1.645		-1.630		-1.605	
I_{IH} I_{IL} I_{IL}	Input current HIGH LOW CS	$V_{IH} = \text{MAX}$		220		220		220	μA
		$V_{IL} = \text{MIN}$	-6		-6		-6		
		$V_{IL} = \text{MIN}$	10		10		10		
I_{EE}	Supply current	$V_{IL} = \text{MIN}$		150		150		150	mA
C_{IN} C_{OUT}	Capacitance Input Output							8 8	pF

NOTES

1. Voltages are defined with respect to ground, pin 18.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow >400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $0^\circ C \leq T_A \leq +75^\circ C$

PARAMETER	10470			10470A			UNIT
	Min	Typ	Max	Min	Typ	Max	
T_{AA}	Address access time		35			25	ns
T_{BD}	Chip select recovery time		10	15	10	15	ns
T_{BS}	Chip select access time		10	15	10	15	ns
T_{WD}	Write disable time ¹		7	15		15	ns
T_{WP}	Write pulse width		25		16		ns
T_{WR}	Write recovery time ¹		10	20	10	20	ns
T_{WHA}	Address hold time ¹		5	1	5	1	ns
T_{WHC}	Chip select hold time ¹		5	1	5	1	ns
T_{WHD}	Data hold time ¹		5	1	5	1	ns
T_{WSA}	Address setup time ¹		Note 8	5	Note 8	5	ns
T_{WSC}	Chip select setup time ¹		5	1	5	1	ns
T_{WSD}	Data setup time ¹		5	1	5	1	ns
t_f	Output fall time ²			5		5	ns
t_r	Output rise time ²			5		5	ns

NOTES

1. To guarantee a write into the slowest bit.
2. Measured between 20% and 80% points.
3. AC limits apply after thermal equilibrium has been established.
4. Unit is in a test socket or mounted on a printed circuit board with transverse air flow >400 ft/min.
5. Setup and hold times are guaranteed for $T_{WV} \geq T_{WV \text{ MIN}}$.
6. After propagation measurements to output are measured from 50% of the input pulse to a valid output level ($V_{IH \text{ MIN}}$ or $V_{IL \text{ MAX}}$).
7. Typical values are at $V_{EE} = -5.2V$, $T_A = 25^\circ C$ and maximum loading.
8. $T_{WSA \text{ MIN}} + T_{WHA \text{ MIN}} = 15\text{ns}$.

4096-BIT ECL RAM (4096 × 1)

10470/10470A

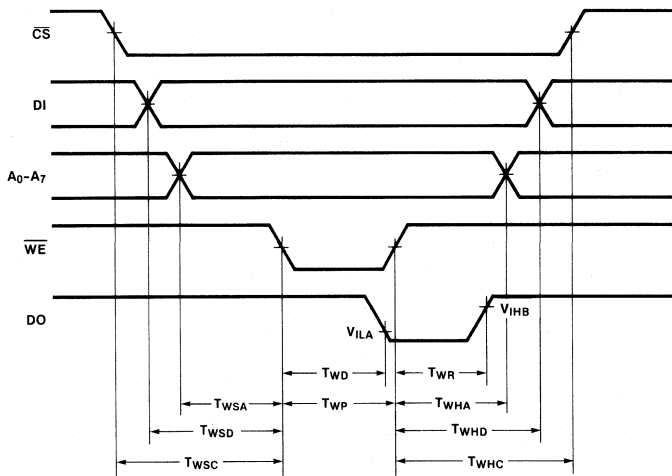
TRUTH TABLE

INPUTS			OUTPUT	MODE
\overline{CS}	\overline{WE}	D_{IN}		
H	X	X	L	Disable
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

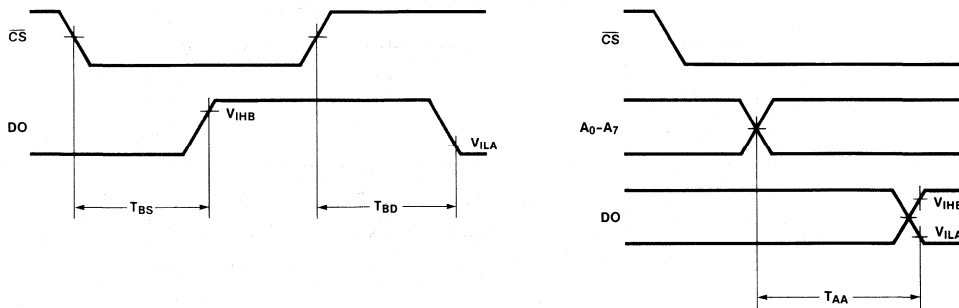
H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

TIMING DIAGRAMS

WRITE MODE



READ MODE



6

4096-BIT ECL RAM (1024×4)

10474/10474A

Preview

DESCRIPTION

The 10474/10474A device is a 1024 words by 4 bits fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines.

The 10474/10474A is compatible with the 10K ECL families and includes on-chip voltage compensation for improved noise margin.

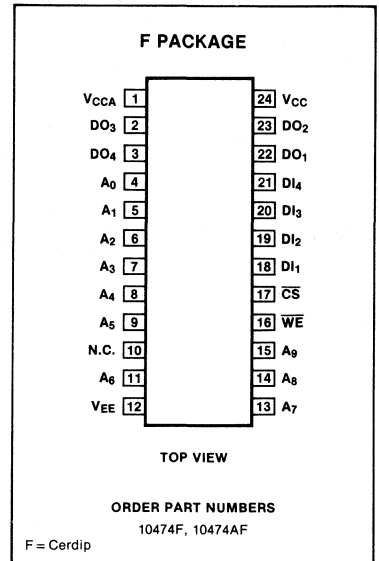
The device is specified with two different read cycle times:

- 10474 : 25ns max
- 10474A: 20ns max

FEATURES

- Organization: 1024 words by 4 bits
- Fully compatible with 10K ECL families
- Operating temperature: 0°C to +75°C
- Address access times:
 - 10474: 25ns max
 - 10074A: 20ns max
- Low supply current of 195mA max

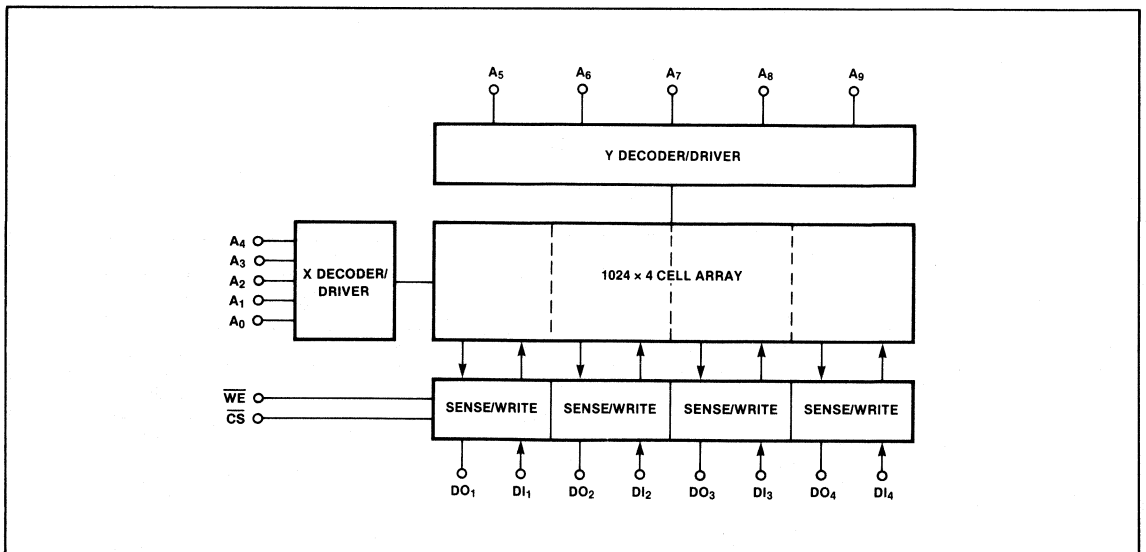
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{EE} Supply voltage	- 7	Vdc
V _{IN} Input voltage	+ 0.5 to V _{EE}	Vdc
I _O Output current	- 30	mA
T _A Operating	0 to + 75	°C
T _{stg} Storage	- 55 to + 150	°C

BLOCK DIAGRAM



4096-BIT ECL RAM (1024 × 4)

10474/10474A

Preview

DC ELECTRICAL CHARACTERISTICS $V_{CC}=0V, V_{EE} = -5.2V \pm 5\%, R_L = 50\Omega$ to $-2V, 0^\circ C \leq T_A \leq +75^\circ C$

PARAMETER	TEST CONDITIONS	0°C		+25°C		+75°C		UNIT
		Min	Max	Min	Max	Min	Max	
V_{IH} V_{IL} V_{IHA} V_{ILA}	Input voltage HIGH LOW Threshold HIGH Threshold LOW		-0.840		-0.810		-0.720	V
V_{OH} V_{OL} V_{OHA} V_{OLA}	Output voltage HIGH LOW Threshold HIGH Threshold LOW	$V_{IH} = \text{MAX}$ $V_{IL} = \text{MIN}$ V_{IHA} V_{ILA}	-1.0 -1.870 -1.020 -1.645	-0.840 -1.665 -0.980 -1.630	-0.960 -1.850 -0.980 -1.630	-0.810 -1.650 -0.900 -1.630	-0.900 -1.830 -0.900 -1.605	V
I_{IH} I_{IL} I_{IL}	Input current HIGH LOW CS	$V_{IH} = \text{MAX}$ $V_{IL} = \text{MIN}$ $V_{IL} = \text{MIN}$		220		220		μA
I_{EE}	Supply current	$V_{IL} = \text{MIN}$		195		195		mA
C_{IN} C_{OUT}	Capacitance Input Output						8 8	pF

NOTES

1. Voltages are defined with respect to ground, pins 1 and 24.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow >400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC}=0V, V_{EE} = +5.2V \pm 5\%, R_L = 50\Omega$ to $-2V, 0^\circ C \leq T_A \leq +75^\circ C$

PARAMETER	10474			10474A			UNIT
	Min	Typ	Max	Min	Typ	Max	
T_{AA}	Address access time		25			20	ns
T_{BD}	Chip select recovery time		10	15	10	15	ns
T_{BS}	Chip select access time		10	15	10	15	ns
T_{WD}	Write disable time ¹		6	15	6	15	ns
T_{WP}	Write pulse width	16		12			ns
T_{WR}	Write recovery time ¹		8	20	8	20	ns
T_{WHA}	Address hold time ¹	Note 8	1	Note 8	1		ns
T_{WHC}	Chip select hold time ¹	5	1	5	1		ns
T_{WHD}	Data hold time ¹	5	1	5	1		ns
T_{WSA}	Address setup time ¹	Note 8	3	Note 8	3		ns
T_{WSC}	Chip select setup time ¹	5	1	5	1		ns
T_{WSD}	Data setup time ¹	5	1	5	1		ns
t_f	Output fall time ²		5		5		ns
t_r	Output rise time ²		5		5		ns

NOTES

1. To guarantee a write into the slowest bit.
2. Measured between 20% and 80% points.
3. AC limits apply after thermal equilibrium has been established.
4. Unit is in a test socket or mounted on a printed circuit board with transverse air flow >400 ft/min.
5. Setup and hold times are guaranteed for $T_{WP} > T_{W} \text{ MIN}$.
6. After propagation measurements to output are measured from 50% of the input pulse to a valid output level ($V_{IH} \text{ MIN}$ or $V_{IL} \text{ MAX}$).
7. Typical values are at $V_{EE} = -5.2V, T_A = 25^\circ C$ and maximum loading.
8. $T_{WSA} \text{ MIN} + T_{WHA} \text{ MIN} = 14\text{ns}$.



1024-BIT ECL RAM (1024 × 1)

100415/100415A/100415B

DESCRIPTION

The 100415 device is a 1024-word by 1-bit, fully encoded ECL Read/Write Random Access Memory designed for high speed scratch pad, control, and buffer storage applications. The 100415 contains voltage and temperature compensation circuits making it 100K family compatible. The device also includes full address decoding on-chip, separate data in and noninverting data out lines and an active LOW chip select.

- **Address access times:**
 - 100415: 20ns max
 - 100415A: 15ns max
 - 100415B: 10ns max
- **Low power dissipation of 0.7mW/bit**
- **Operating temperature: 0°C to +85°C (ambient)**
- **Blanked outputs**
- **CS with 50K pull-down resistor**

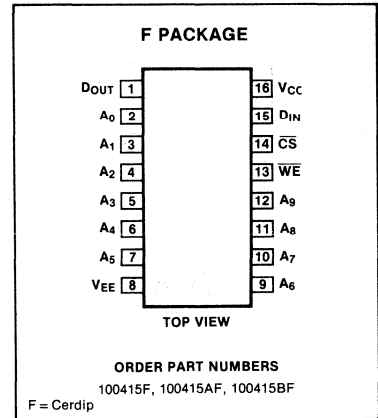
FEATURES

- 1024 words × 1 bit organization
- Fully compatible with 100K series ECL families

APPLICATIONS

- Buffer memory
- Scratch pad memory
- Writeable microcode store

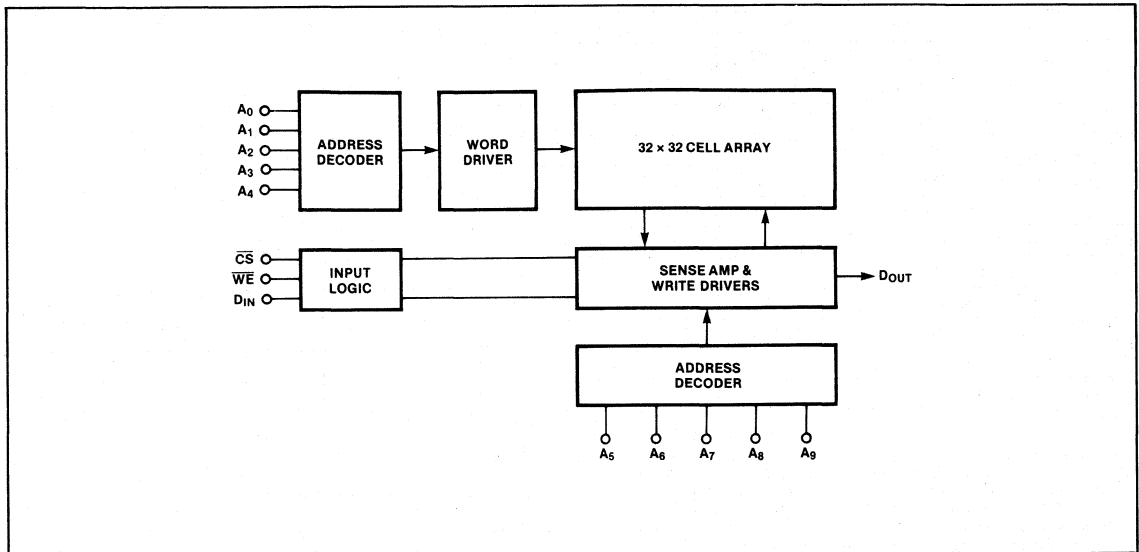
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{EE} Supply voltage	- 7	Vdc
V _{IN} Input voltage	+ 0.5 to V _{EE}	Vdc
I _O Output source current	- 30	mA
T _A Operating	0 to + 85	°C
T _J Operating junction	125	°C
T _{stg} Storage	- 55 to + 150	°C

BLOCK DIAGRAM



1024-BIT ECL RAM (1024 × 1)

100415/100415A/100415B

DC ELECTRICAL CHARACTERISTICS $V_{EE} = -4.5V \pm 5\%$, $V_{CC} = GND$, $0^\circ C \leq T_A \leq +85^\circ C$, Loading is 50Ω to -2.0V

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IL} Input voltage LOW		-1.810			V
V_{IH} Input voltage HIGH				-0.880	
V_{ILA} Threshold LOW				-1.475	
V_{IHA} Threshold HIGH		-1.165			
V_{OL} Output voltage LOW	$V_{IL} = \text{MIN}$	-1.810		-1.620	V
V_{OH} Output voltage HIGH	$V_{IH} = \text{MAX}$	-1.025		-0.880	
V_{OLA} Threshold LOW	$V_{IL} = \text{MAX}$			-1.610	
V_{OHA} Threshold HIGH	$V_{IH} = \text{MIN}$	-1.035			
I_{IL} Input current LOW	$V_{IL} = \text{MIN}$	-6			μA
I_{IL} Input current CS	$V_{IL} = \text{MIN}$	+10			
I_{IH} Input current HIGH	$V_{IH} = \text{MAX}$			220	
I_{EE} Supply current				150	mA

NOTES

1. Voltages are defined with respect to ground, pin 16.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurements, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{EE} = -4.5V \pm 5\%$, $0^\circ C \leq T_A \leq +85^\circ C$, $V_{CC} = GND$, Output load = 50Ω to -2.0V

PARAMETER	100415			100415A			100415B			UNIT
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T_{AA} Address access time			20			15			10	ns
T_{BD} Chip select recovery time			5			5			5	ns
T_{BS} Chip select access time			5			5			5	ns
T_{WD} Write disable time ¹		4.5	6		4.5	6		4.5	6	ns
T_{WP} Write pulse width	12			10			8			ns
T_{WR} Write recovery time ¹			10			10			10	ns
T_{WHA} Address hold time ¹	3	0		3	0		3	0		ns
T_{WHC} Chip select hold time ¹	2	0		2	0		2	0		ns
T_{WHD} Data hold time ¹	2	0		2	0		2	0		ns
T_{WSA} Address setup time ¹	1	0		1	0		1	0		ns
T_{WSC} Chip select setup time ¹	2	0		2	0		2	0		ns
T_{WSD} Data setup time ¹	2	0		2	0		2	0		ns
t_f Output fall time ²	0.5	2		0.5	2		0.5	2		ns
t_r Output rise time ²	0.5	2		0.5	2		0.5	2		ns
C_{IN} Capacitance input						5			5	pF
C_{OUT} Capacitance output						5			5	pF

NOTES

1. AC limits apply after thermal equilibrium has been established.
2. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
3. Setup and hold times are guaranteed for $T_{W} \geq T_{W} \text{ MIN}$.
4. All propagation measurements to output are measured from 50% of the input pulse to a valid output level ($V_{IH} \text{ MIN}$ or $V_{IL} \text{ MAX}$).
5. Setup and hold times are guaranteed for $T_{W} \geq T_{W} \text{ MIN}$.
6. All propagation measurements to output are measured from 50% of the input pulse to a valid output level ($V_{IH} \text{ MIN}$ or $V_{IL} \text{ MAX}$).
7. Typical values are at $V_{EE} = -4.5V$, $T_A = 25^\circ C$ and maximum loading.

1024-BIT ECL RAM (1024 × 1)

100415/100415A/100415B

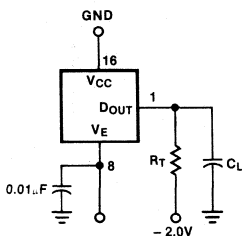
TRUTH TABLE

INPUTS			OUTPUT	MODE
CS	WE	D _{IN}		
H	X	X	L	Disable
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D _{OUT}	Read

H = HIGH voltage level
L = LOW voltage level
X = Don't care

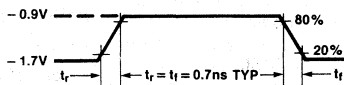
SWITCHING TIMES TEST CIRCUIT AND TIMING DIAGRAMS

LOADING CONDITIONS



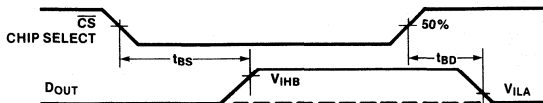
NOTES
C_L = 30pF including jig and stray capacitance
R_T = 50Ω termination of scope

INPUT LEVELS

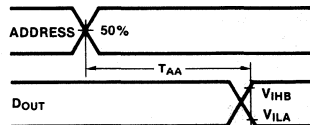


All timing measurements referenced to 60% of input levels.

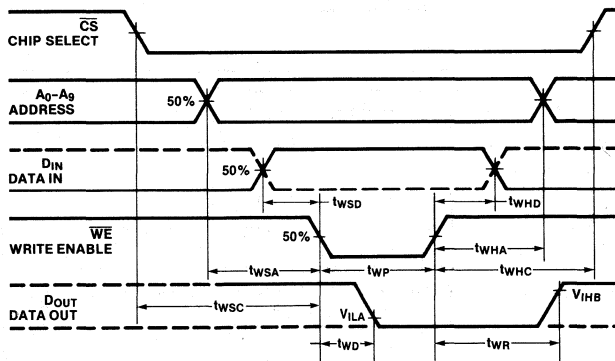
READ MODE PROPAGATION DELAY FROM CHIP SELECT



READ MODE PROPAGATION DELAY FROM ADDRESS



WRITE MODE



NOTE
Timing diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

6

1024-BIT ECL RAM (256 × 4)

100422/100422A/100422B

DESCRIPTION

The 100422 device is a 256-word by 4-bit, fully encoded ECL Read/Write Random Access Memory designed for high speed scratch pad, control, and buffer storage applications. The 100422 contains voltage and temperature compensation circuits making it 100K family compatible. The 100422 is available in a slim line 24-pin dual-in-line package. This circuit may be reconfigured as 512×2 or 1024×1 organization by utilizing the block select feature. Each block has its own LOW active block select to enable the output. Write enable LOW active enables the write function in selected blocks. The memory has eight Address inputs, four Data inputs, four Block Select inputs, one Write Enable input and four Data outputs. The outputs require external resistance terminations as they are not terminated internally through resistance to the V_{EE} supply voltage. The input pull-down resistor to V_{EE} is 50,000Ω typical for the block selects.

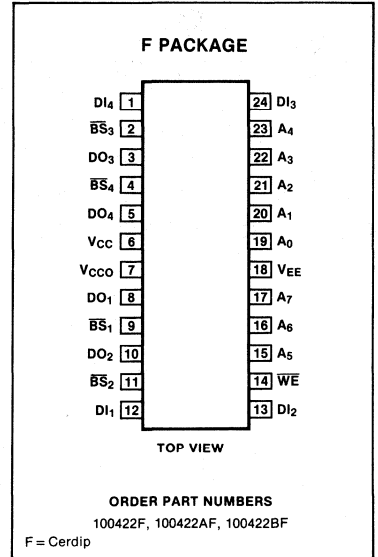
FEATURES

- 256 words × 4 bits organization
- Fully compatible with 100K series ECL families
- Address access times:
 - 100422: 20ns max
 - 100422A: 15ns max
 - 100422B: 10ns max
- Low power dissipation of 0.8mW/bit
- Operating temperature: 0°C to +85°C (ambient)
- Block select allows variable organization

APPLICATIONS

- High speed scratch pad
- Control and buffer storage

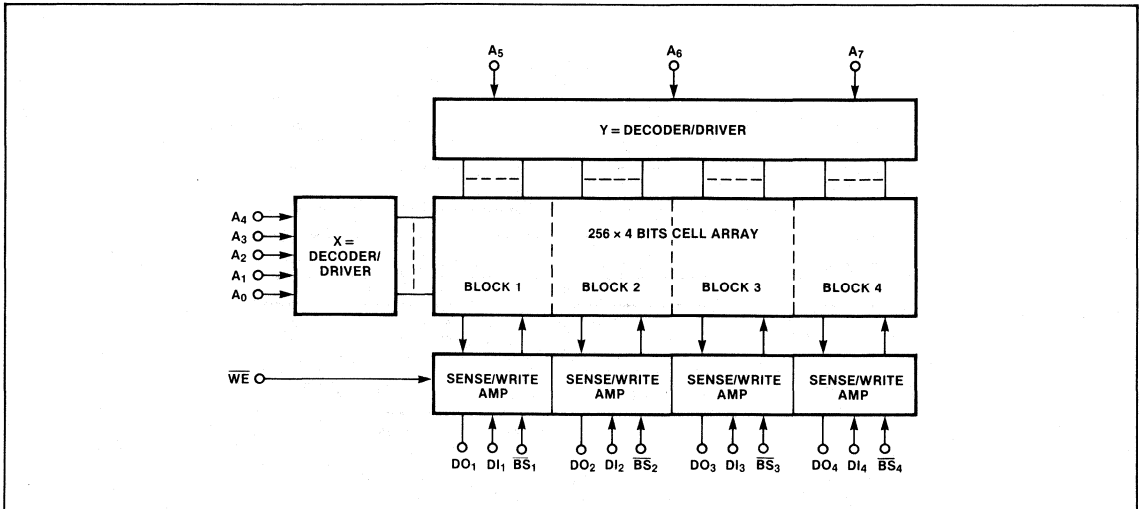
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{EE} Supply voltage	- 7	Vdc
V _{IN} Input voltage	0 to V _{EE}	Vdc
I _O Output source current temperature range	- 30	mAdc
T _A Operating	0 to + 85	°C
T _J Operating junction	125	°C
T _{stg} Storage	- 55 to + 150	°C

BLOCK DIAGRAM



1024-BIT ECL RAM (256 × 4)

100422/100422A/100422B

DC ELECTRICAL CHARACTERISTICS $V_{CC}=0V$, $V_{EE} = -4.5V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $0^\circ C \leq T_A \leq +85^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
		Min	Typ	Max		
Input voltage V_{IL} LOW V_{IH} HIGH V_{ILA} Threshold LOW V_{IHA} Threshold HIGH		-1.810		-0.880 -1.475	V	
	Output voltage V_{OL} LOW V_{OH} HIGH V_{OLA} Threshold LOW V_{OHA} Threshold HIGH	$V_{IL} = \text{MIN}$	-1.810		-1.620	V
		$V_{IH} = \text{MAX}$	-1.025		-0.880	
		$V_{IL} = \text{MAX}$			-1.610	
$V_{IH} = \text{MIN}$		-1.035				
Input current I_{IL} LOW I_{IL} BS I_{IH} HIGH	$V_{IL} = \text{MIN}$	-6			μA	
	$V_{IL} = \text{MIN}$	+10				
	$V_{IH} = \text{MAX}$			220		
I_{EE} Supply current				195	mA	
Capacitance C_{IN} Input C_{OUT} Output				8	pF	
				8		

NOTES

1. Voltages are defined with respect to ground, pins 6 and 7.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC}=0V$, $V_{EE} = -4.5V \pm 5\%$, $R_L = 50\Omega$ to $-2V$, $0^\circ C \leq T_A \leq +85^\circ C$

PARAMETER	100422			100422A			100422B			UNIT
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
T_{AA} Address access time			20			15			10	ns
T_{BD} Block select recovery time			5			5			5	ns
T_{BS} Block select access time			5			5			5	ns
T_{WD} Write disable time ¹			5			5			5	ns
T_{WP} Write pulse width	12			10			8			ns
T_{WR} Write recovery time ¹		4.5	9		4.5	9		4.5	9	ns
T_{WHA} Address hold time ¹	5	0		5	0		5	0		ns
T_{WHC} Block select hold time ¹	4	0		4	0		4	0		ns
T_{WHD} Data hold time ¹	4	0		4	0		4	0		ns
T_{WSA} Address setup time ¹	2	0		2	0		2	0		ns
T_{WSC} Block select setup time ¹	3	0		3	0		3	0		ns
T_{WSD} Data setup time ¹	3	0		3	0		3	0		ns
t_f Output fall time ²		2			2			2		ns
t_r Output rise time ²		2			2			2		ns

NOTES

1. To guarantee a write into the slowest bit.
2. Measured between 20% and 80% points.
3. AC limits apply after thermal equilibrium has been established.
4. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
5. Setup and hold times are guaranteed for $T_{WP} \geq T_{WY}$ MIN.
6. All propagation measurements to output are measured from 50% of the input pulse to a valid output level (V_{IH} MIN or V_{IL} MAX).
7. Typical values are at $V_{EE} = -4.5V$, $T_A = 25^\circ C$ and maximum loading.

1024-BIT ECL RAM (256 × 4)

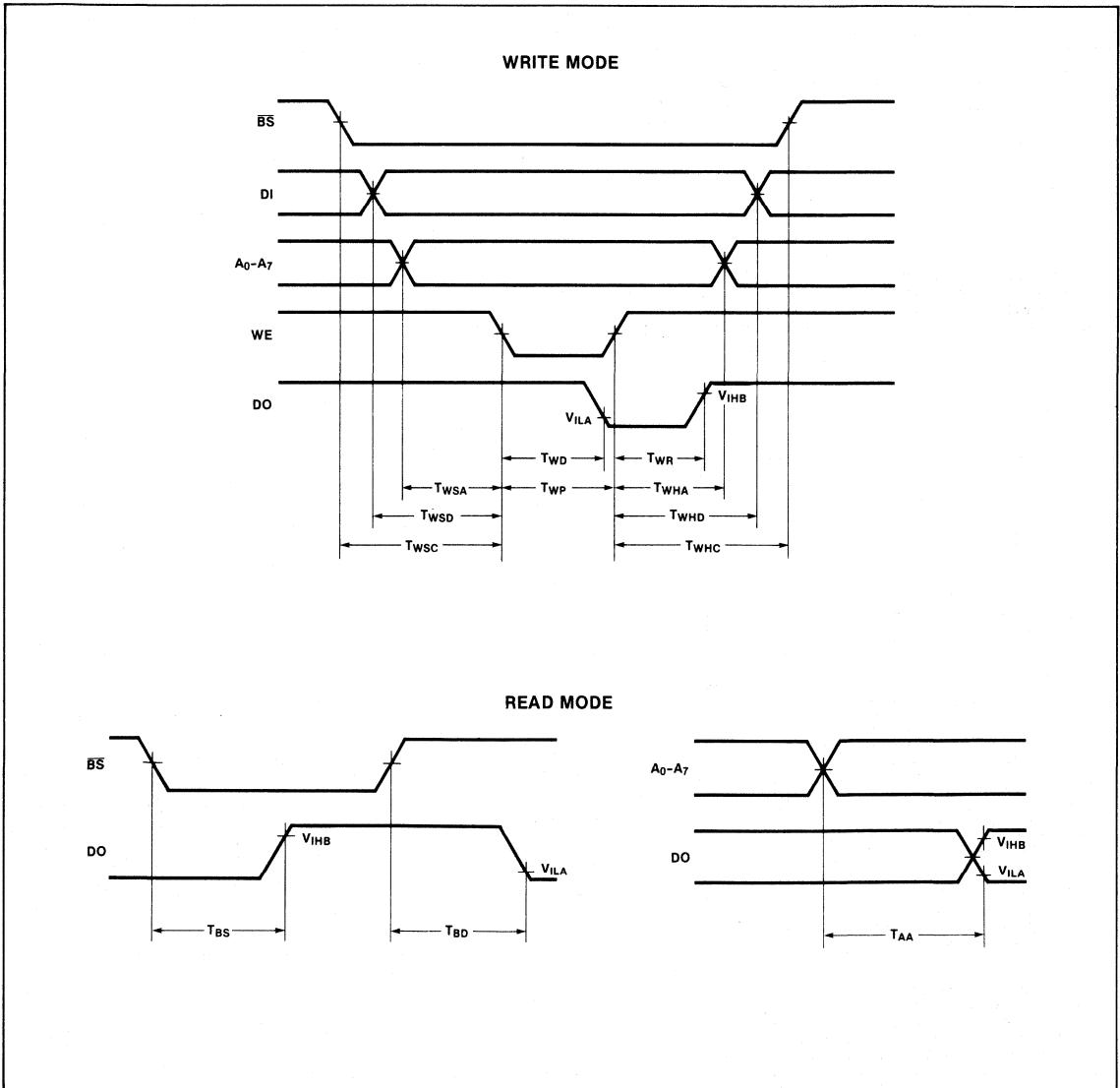
100422/100422A/100422B

TRUTH TABLE (Positive Logic)

INPUTS			OUTPUT	MODE
\overline{BS}_N	\overline{WE}	DI_N	DO_N	
H	X	X	L	Disable
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care
 N = Blocks 1-4

TIMING DIAGRAMS



4096-BIT ECL RAM (4096 × 1)

100470/100470A

Advance Information

DESCRIPTION

The 100470/100470A device is a 4096 words by 1 bit fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control, and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines, and an active LOW Chip Select input.

The 100470/100470A is compatible with the 100K ECL families and includes on-chip voltage and temperature compensation.

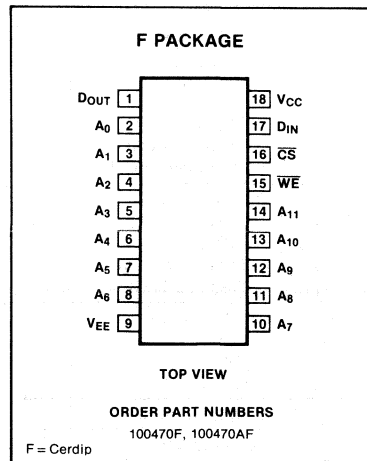
The device is specified with two different read cycle times:

- 100470 : 35ns max
- 100470A: 25ns max

FEATURES

- Organization: 4096 words by 1 bit
- Fully compatible with 100K ECL families
- Operating temperature: 0°C to +85°C
- Address access times:
 - 100470: 35ns max
 - 100470A: 25ns max
- Low supply current of 150mA max

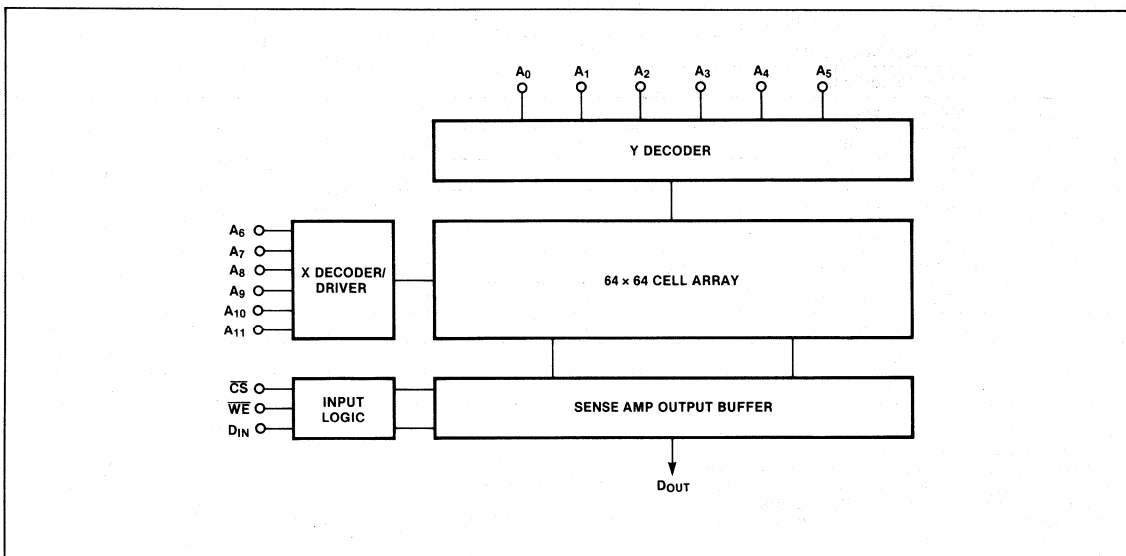
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{EE} Supply voltage	- 7	Vdc
V _{IN} Input voltage	+ 0.5 to V _{EE}	Vdc
I _O Output current	- 30	mA
T _A Operating	0 to + 85	°C
T _{stg} Storage	- 55 to + 150	°C

BLOCK DIAGRAM



4096-BIT ECL RAM (4096 × 1)

100470/100470A

Advance Information

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, 0^\circ C \leq T_A \leq +85^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
Input voltage V_{IL} LOW V_{IH} HIGH V_{ILA} Threshold LOW V_{IHA} Threshold HIGH		-1.810		-0.880 -1.475	V
Output voltage V_{OL} LOW V_{OH} HIGH V_{OLA} Threshold LOW V_{OHA} Threshold HIGH	$V_{IL} = \text{MIN}$ $V_{IH} = \text{MAX}$ $V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}$	-1.810 -1.025 -1.035		-1.620 -0.880 -1.610	V
Input current I_{IL} LOW I_{IL} CS I_{IH} HIGH	$V_{IL} = \text{MIN}$ $V_{IL} = \text{MIN}$ $V_{IH} = \text{MAX}$	-6 +10		220	μA
I_{EE} Supply current				150	mA
Capacitance C_{IN} Input C_{OUT} Output				8 8	pF

NOTES

1. Voltages are defined with respect to ground, pin 18.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.

AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, 0^\circ C \leq T_A \leq +85^\circ C$

PARAMETER	100470			100470A			UNIT
	Min	Typ	Max	Min	Typ	Max	
T_{AA} Address access time			35			25	ns
T_{BD} Chip select recovery time		10	15		10	15	ns
T_{BS} Chip select access time		10	15		10	15	ns
T_{WD} Write disable time ¹		7	15		7	15	ns
T_{WP} Write pulse width	25			16			ns
T_{WR} Write recovery time ¹		10	20		10	20	ns
T_{WHA} Address hold time ¹	5	1		5	1		ns
T_{WHC} Chip select hold time ¹	5	1		5	1		ns
T_{WHD} Data hold time ¹	5	1		5	1		ns
T_{WSA} Address setup time ¹	Note 8	5		Note 8	5		ns
T_{WSC} Chip select setup time ¹	5	1		5	1		ns
T_{WSD} Data setup time ¹	5	1		5	1		ns
t_f Output fall time ²		5			5		ns
t_r Output rise time ²		5			5		ns

NOTES

1. To guarantee a write into the slowest bit.
2. Measured between 20% and 80% points.
3. AC limits apply after thermal equilibrium has been established.
4. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
5. Setup and hold times are guaranteed for $T_W \geq T_W \text{ MIN}$.
6. After propagation measurements to output are measured from 50% of the input pulse to a valid output level ($V_{IH} \text{ MIN}$ or $V_{IL} \text{ MAX}$).
7. Typical values are at $V_{EE} = -5.2V, T_A = 25^\circ C$ and maximum loading.
8. $T_{WSA} \text{ MIN} + T_{WHA} \text{ MIN} = 15\text{ns}$.

4096-BIT ECL RAM (1024×4)

100474/100474A

Preview

DESCRIPTION

The 100474/100474A device is a 1024 words by 4 bits fully decoded Read/Write Random Access Memory, designed for high speed scratch pad, control, and buffer storage applications. The device also includes full address decoding, on-chip separate data in and noninverting data out lines.

The 100474/100474A, with its voltage and temperature compensation, is compatible with the 100K ECL families.

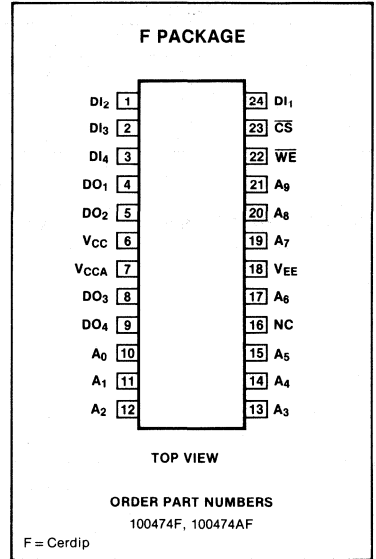
The device is specified with two different read cycle times:

- 100474 : 25ns max
- 100474A: 20ns max

FEATURES

- **Organization:** 1024 words by 4 bits
- **Fully compatible with 100K ECL families**
- **Operating temperature:** 0°C to +85°C
- **Address access times:**
 - 100474: 25ns max
 - 100074A: 20ns max
- **Low supply current of 195mA max**

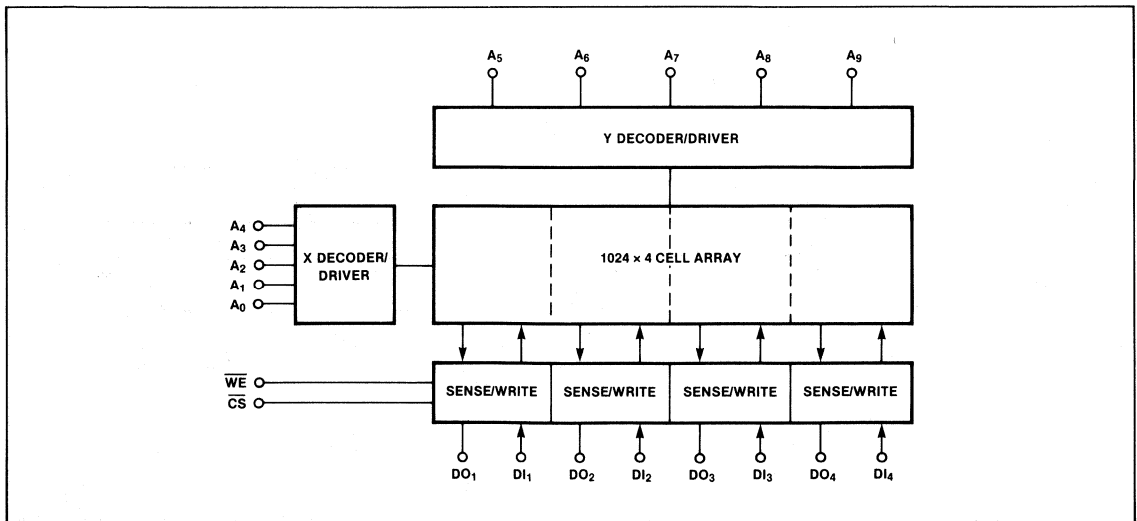
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{EE} Supply voltage	-7	Vdc
V _{IN} Input voltage	+0.5 to V _{EE}	Vdc
I _O Output current	-30	mA
T _A Operating	0 to +85	°C
T _{stg} Storage	-55 to +150	°C

BLOCK DIAGRAM



4096-BIT ECL RAM (1024 × 4)

100474/100474A

Preview

DC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, 0^\circ C \leq T_A \leq +85^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{IL} Input voltage LOW V_{IH} Input voltage HIGH V_{ILA} Threshold LOW V_{IHA} Threshold HIGH		-1.810		-0.880 -1.475	V
V_{OL} Output voltage LOW V_{OH} Output voltage HIGH V_{OLA} Threshold LOW V_{OHA} Threshold HIGH	$V_{IL} = \text{MIN}$ $V_{IH} = \text{MAX}$ $V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}$	-1.810 -1.025 -1.035		-1.620 -0.880 -1.610	V
I_{IL} Input current LOW I_{IL} Input current CS I_{IH} Input current HIGH	$V_{IL} = \text{MIN}$ $V_{IL} = \text{MIN}$ $V_{IH} = \text{MAX}$	-6 +10		220	μA
I_{EE} Supply current				195	mA
C_{IN} Capacitance Input C_{OUT} Capacitance Output				8 8	pF

NOTES

1. Voltages are defined with respect to ground, pins 6 and 7.
2. Unit is in a test socket or mounted in a printed circuit board with transverse air flow > 400 ft/min.
3. DC limits apply after thermal equilibrium has been established.
4. For current measurement, maximum is defined as the maximum absolute value.



AC ELECTRICAL CHARACTERISTICS $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, 0^\circ C \leq T_A \leq +85^\circ C$

PARAMETER	100474			100474A			UNIT
	Min	Typ	Max	Min	Typ	Max	
T_{AA} Address access time			25			20	ns
T_{BD} Chip select recovery time		10	15		10	15	ns
T_{BS} Chip select access time		10	15		10	15	ns
T_{WD} Write disable time ¹		6	15		6	15	ns
T_{WP} Write pulse width	16			12			ns
T_{WR} Write recovery time ¹		8	20		8	20	ns
T_{WHA} Address hold time ¹	Note 8	1		Note 8	1		ns
T_{WHC} Chip select hold time ¹	5	1		5	1		ns
T_{WHD} Data hold time ¹	5	1		5	1		ns
T_{WSA} Address setup time ¹	Note 8	3		Note 8	3		ns
T_{WSC} Chip select setup time ¹	5	1		5	1		ns
T_{WSD} Data setup time ¹	5	1		5	1		ns
t_f Output fall time ²		5			5		ns
t_r Output rise time ²		5			5		ns

NOTES

1. To guarantee a write into the slowest bit.
2. Measured between 20% and 80% points.
3. AC limits apply after thermal equilibrium has been established.
4. Unit is in a test socket or mounted on a printed circuit board with transverse air flow > 400 ft/min.
5. Setup and hold times are guaranteed for $T_{W} \geq T_{W \text{ MIN}}$.
6. After propagation measurements to output are measured from 50% of the input pulse to a valid output level ($V_{IH \text{ MIN}}$ or $V_{IL \text{ MAX}}$).
7. Typical values are at $V_{EE} = -5.2V, T_A = 25^\circ C$ and maximum loading.
8. $T_{WSA \text{ MIN}} + T_{WHA \text{ MIN}} = 14ns$.

4096-BIT ECL RAM (1024 × 4)

100474/100474A

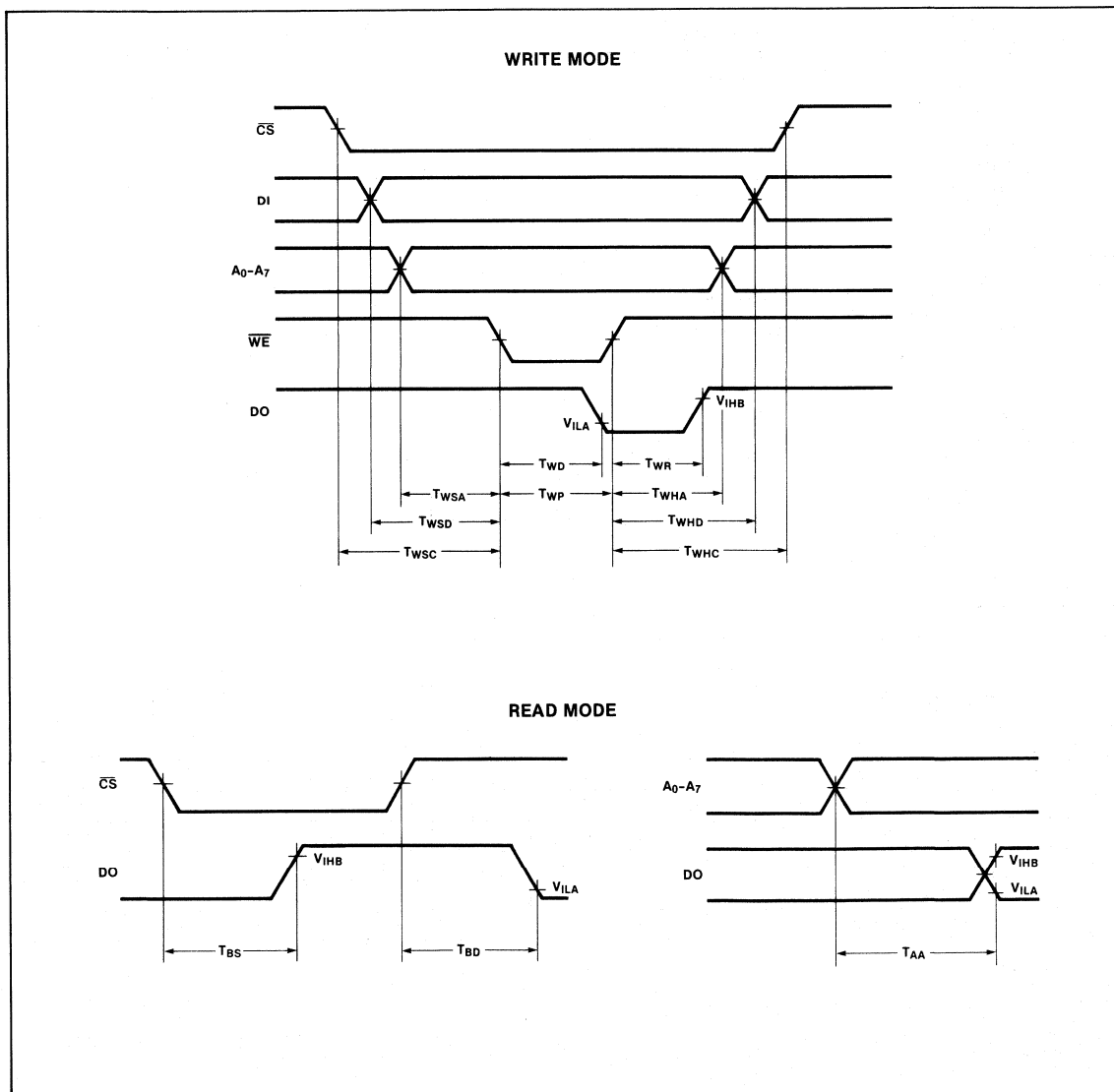
Preview

TRUTH TABLE

INPUTS			OUTPUT	MODE
\overline{CS}	\overline{WE}	D_{IN}		
H	X	X	L	Disable
L	L	L	L	Write 0
L	L	H	L	Write 1
L	H	X	D_{OUT}	Read

H = HIGH voltage level
 L = LOW voltage level
 X = Don't care

TIMING DIAGRAMS



**Section 7
PROM
Programming
Information**

GENERIC PROGRAMMING PROCEDURE

GENERIC PROGRAMMING PROCEDURE

The Signetics family of Schottky PROMs are high performance bipolar devices which use a nickel/chromium (nichrome) alloy fuse to provide the many benefits of field programming. All Signetics Schottky PROMs use a common fuse design and programming circuitry. This means that a programmer capable of programming any Signetics PROM should program the entire family. Because of the pinout variation a small selection of socket adapters may be required. Programming is accomplished by application of voltages above those used for normal operation, therefore, no special pins are required for programming (except the 82S115 which has two pins: FE₁ and FE₂). The programming voltages and timing requirements make unintentional programming virtually impossible. Arrays of devices may be programmed in the users circuit, if desirable, and isolation of programming voltages is provided.

Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of PROM programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers equipment is available on request from Bipolar Memory Marketing.

In order to consistently achieve excellent programming yields, periodic calibration of the programming equipment is required. Consult the equipment manufacturer for the recommended calibration interval. Records of programming yield, by device type, should be kept and any downward trend or sudden change should be considered as an indication of a need to recalibrate programming equipment.

The following information is provided for reference and completeness of individual data sheets.

SIGNETICS DISCOURAGES THE CONSTRUCTION AND USE OF "HOMEMADE" PROGRAMMING EQUIPMENT.

The generic family of Schottky PROMs uses no special pins for programming. The programming mode is evoked by raising the V_{CC} pin to +8.75 ± .25V. This voltage is referred to as V_{CCP}. The address pins remain TTL compatible and are used to address the unique word to be programmed. The outputs are used to supply fusing current in the programming mode.

Programming is performed one bit at a time, the word address is set up on the address inputs and the fuse to be programmed is selected by raising the output (corresponding to the bit in the word) to +17V ± 1V. This voltage is known as V_{OPF} and must be supplied by a voltage source with a low impedance and very fast transient response. Reliable programming depends on the V_{OPF} power supply and circuitry. I_{OPF} is the current which should be drawn by the part during the programming sequence. V_{OPF} should be maintained and I_{OPF} monitored. If

the current is not within specification, reliable fusing can not be assured.

Unprogrammed parts are supplied with all bits "zero", only the bits intended to be "one" will be programmed.

A fuse which does not blow during the first programming cycle should be considered a defective device and should be discarded.

Verification of the device may be performed after all addresses have been programmed.

PROGRAMMING SYSTEM SPECIFICATIONS⁴ (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V _{CCP} Power supply voltage To program ¹	I _{CCP} = 425 + 75mA, Transient or steady state	8.5		9.0	V
Verify limit					V
V _{CCVH} Upper		5.3		5.7	
V _{CCVL} Lower		4.3		4.7	
V _S Verify threshold ²		1.4		1.6	V
I _{CCP} Programming supply current	V _{CCP} = +8.75 ± .25V	350		500	mA
Input voltage					V
V _{IH} High		2.4		5.5	
V _{IL} Low		0		0.8	
Input current					μA
I _{IH} High	V _{IH} = +5.5V			50	
I _{IL} Low	V _{IL} = +0.4V			-500	
V _{OPF} Forced output voltage (program) ³	I _{OPF} = 200 ± 20mA, Transient or steady state	16.0		18.0	V
I _{OPF} Forced output current (program)	V _{OPF} = +17 ± 1V	180		220	mA
T _R Output pulse rise time		10			μs
t _p CE programming pulse width		100		125	μs
t _d Pulse sequence delay		5			μs
T _V CE verify pulse width		1			μs
T _{PVA} Address program-verify cycle				1	ms
T _{PVM} Memory program-verify time (continuous)				20	sec
F _L Fusing attempts per link				1	cycle

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. This voltage should be maintained within specified limits during the entire fusing cycle. For a transient current of 150mA, limit voltage spikes to a maximum slew rate of

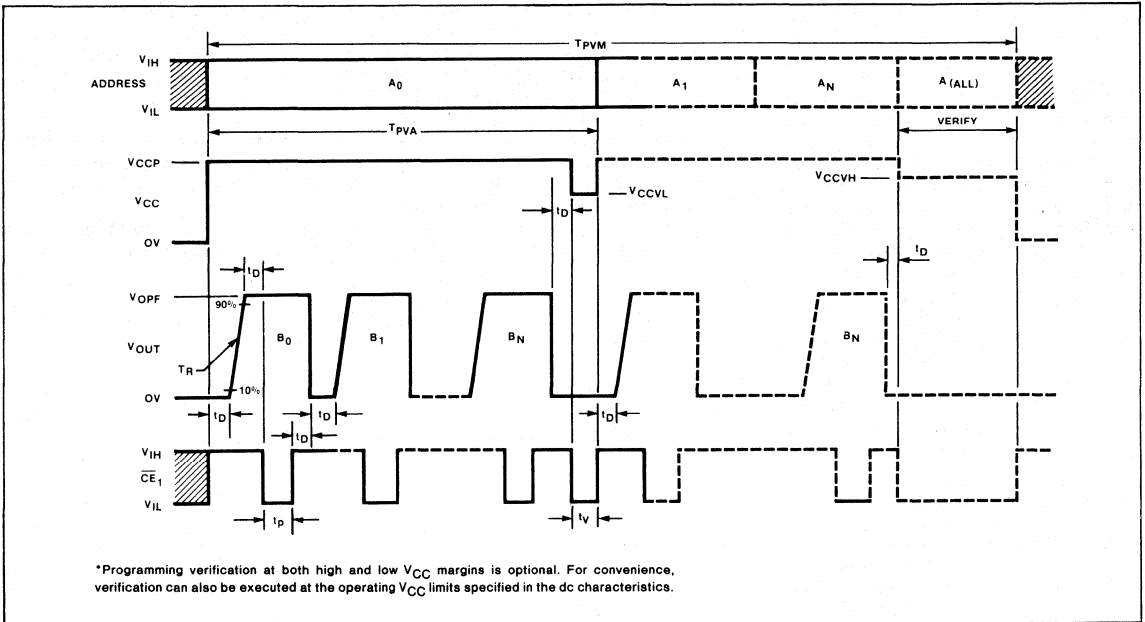
2V/μs, and 10μs maximum recovery.

4. These are specifications which a Programming System must satisfy in order to be qualified by Signetics. They contain new limits for minimizing total device programming time, which supersede, but do not obsolete the performance requirements of previously manufactured programming equipment. Programming procedure for devices not listed in table 1 are found with the device data sheet.



GENERIC PROGRAMMING PROCEDURE

TYPICAL GENERIC PROGRAMMING SEQUENCE



PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10k Ω resistor to V_{CC} (10K resistor is the pullup resistor for open collector devices).
2. Consult table 1 for CE conditions.
3. Select the Address to be programmed and raise V_{CC} to V_{CCP} .
4. After t_D delay, apply V_{OPF} to the output to be programmed. Program one output at the time. Note leading edge rise time restrictions.
5. After t_D delay, pulse the \overline{CE}_X input to logic low for a time t_p .
6. After t_D delay, remove V_{OPF} from the programmed output.
7. Repeat steps 4 through 6 to program other bits at the same address.
8. To verify programming of all bits at the same address, after t_D delay lower V_{CC} to V_{CCVL} and apply a logic low level to the \overline{CE}_X input. All programmed outputs should remain in the logic high state.
9. After t_D delay, repeat steps 3 through 8 to program and verify all other address locations.
10. After t_D delay, raise V_{CC} to V_{CCVH} and verify all memory locations by applying a logic low level to \overline{CE}_X and cycling through all device addresses.

82S115 PROGRAMMING PROCEDURE

PROGRAMMING SYSTEM SPECIFICATIONS (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ	Max	
V_{CCP} Power supply voltage To program ¹	$I_{CCP} = 200 \pm 25\text{mA}$, Transient or steady state $V_{CCP} = +5.0 \pm .25\text{V}$	4.75		5.25	V
I_{CCP} Programming supply current		175	200	225	mA
Verify limit					V
V_{CCVH} Upper		5.3	5.5	5.7	V
V_{CCVL} Lower		4.3	4.5	4.7	
V_S Verify threshold ²		0.9	1.0	1.1	V
Input voltage					V
V_{IL} Low		0		0.8	V
V_{IH} High		2.4		5.5	
Input Voltage (FE ₁ & FE ₂)					
V_{ILP} Low		4.5	5.0	0.5	V
V_{IHP} High				5.5	
Input current (FE ₁ & FE ₂ only)					μA
I_{IL} Low	$V_{IL} = +0.45\text{V}$			-100	mA
I_{IH} High	$V_{IH} = +5.5\text{V}$			10	
Input current (except FE ₁ & FE ₂)					μA
I_{IL} Low	$V_{IL} = +0.45\text{V}$			-100	mA
I_{IH} High	$V_{IH} = +5.5\text{V}$			25	
V_{OPF} Forced output voltage (program) ³	$I_{OPF} = 200 \pm 20\text{mA}$, Transient or steady state $V_{OPF} = +17 \pm 1\text{V}$	16.0	17.0	18.0	V
I_{OPF} Output current (program) ⁵		180		220	mA
T_R Output pulse rise time		10		50	μs
t_P FE ₂ programming pulse width		0.3	0.4	0.5	ms
t_D Pulse sequence delay		10			μs
T_{PR} Programming time	$V_{CC} = V_{CCP}$			12	sec
T_{PS} Programming pause	$V_{CC} = 0\text{V}$	6			sec
$\frac{T_{PR}}{T_{PR}+T_{PS}}$ Programming duty cycle ⁴				50	%

PROGRAMMING NOTES

1. Bypass V_{CC} to GND with a $0.01\mu\text{F}$ capacitor to reduce voltage spikes.
2. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
3. Care should be taken to insure the $17 \pm 1\text{V}$ output voltage is maintained during the entire fusing cycle.
4. Continuous fusing for an unlimited time is also allowed, provided that a 60% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ($V_{CC} = 0\text{V}$) of 3ms.
5. I_{OPF} is monitored as the peak programming current, abnormal fusing occurs when $I_{OPF} < \text{MIN}$ or $I_{OPF} > \text{MAX}$.

RECOMMENDED PROGRAMMING PROCEDURE

The 82S115 is shipped with all bits at logical low. To write logical high, proceed as follows:

SET-UP

1. Apply GND to pin 12.
2. Terminate all device outputs with a $10\text{K}\Omega$ resistor to V_{CC} . (Optional used for compatibility with Signetics generic programming procedure).
3. Set \overline{CE}_1 to logic low, and CE_2 to logic high (TTL levels).
4. Set Strobe to logic high level.

Program-Verify Sequence

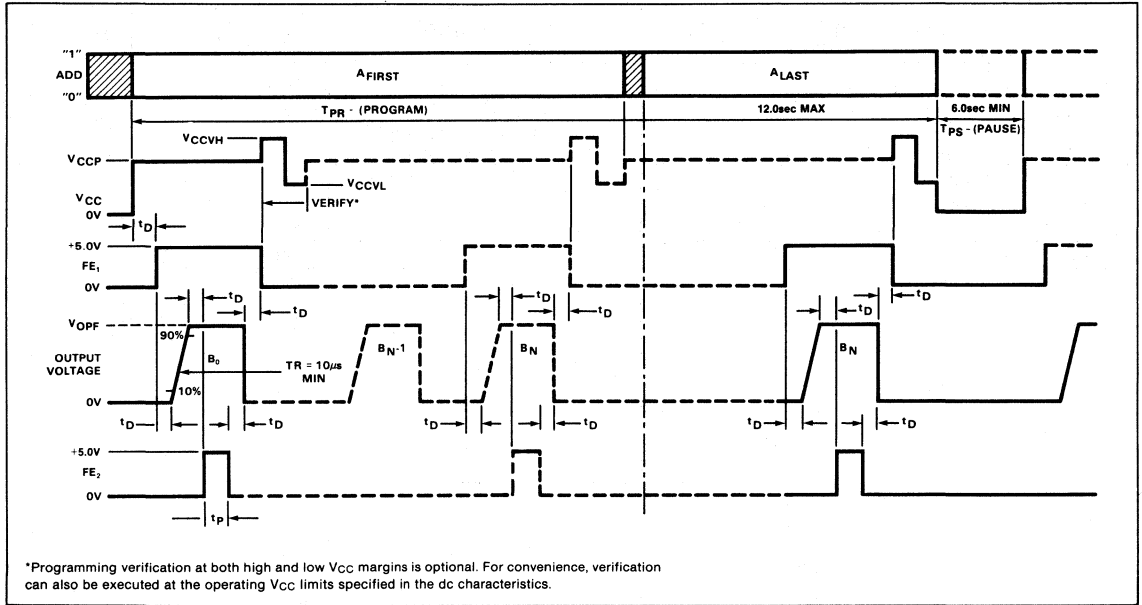
1. Raise V_{CC} to V_{CCP} , and address the word to be programmed by applying TTL high and low logic levels to the device address inputs.
2. After t_D delay, apply to FE₁ (pin 13) a voltage source of V_{IHP} , with 10mA sourcing current capability.
3. After t_D delay, apply a voltage source of V_{OPF} to the output to be programmed. Program one output at a time.
4. After t_D delay, raise FE₂ (pin 11) from V_{ILP} to V_{IHP} for a period of t_P , and then return to V_{ILP} . Pulse source must have a 10mA sourcing current capability.

5. After t_D delay, remove $+17.0\text{V}$ supply from programmed output.
6. To verify programming, after t_D delay, return FE₁ to V_{ILP} . Raise V_{CC} to V_{CCH} . The programmed output should remain in the high state. Again, lower V_{CC} to V_{CCL} , and verify that the programmed output remains in the high state.
7. Raise V_{CC} to V_{CCP} and repeat steps 2 through 6 to program other bits at the same address.
8. Repeat steps 1 through 7 to program all other address locations.



82S115 PROGRAMMING SEQUENCE

TYPICAL 82S115 PROGRAMMING SEQUENCE



10149 PROGRAMMING PROCEDURE

PROGRAMMING NOTES

- These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
- All voltages are referenced to V_{CC2} , pin 16.
- Supply should be bypassed to V_{CC2} with a capacitor so that the voltage stays within specified limits during the entire fusing cycle.
- Refer to typical Programming Circuit and Typical Programming Sequence for definition of parameters.
- V_{OPF} must be an open circuit during verify. It may be 0 volts or an open circuit while programming other outputs.

PROGRAMMING PROCEDURE

The unprogrammed state is logical "0" (low outputs). To program "1s", proceed as follows:

- Terminate all outputs with a 1.8K resistor in series with a 5.6K resistor to V_{EE} .
- Connect \overline{CE} to V_{EE} or leave it open.
- Apply V_{EEP} to the V_{EE} pin.
- Select the word to be programmed using V_{IH} and V_{IL} levels.
- After Address is valid, raise V_{CC1} to V_{CCP} .
- After T_D , apply the V_{OPF} pulse to the 1.8K resistor on the output to be programmed.
- After T_D , apply the V_{OPF} pulse to the next output to be programmed on the same word.
- Bring V_{CC1} to 0 volts and apply V_{EEVL} to the V_{EE} pin.
- After T_D , verify the code on the four outputs using V_{OH} and V_{OL} limits.
- Repeat steps 3-9 for all addresses to be programmed.
- Change V_{EE} to V_{EEVH} and verify the code at all memory locations.

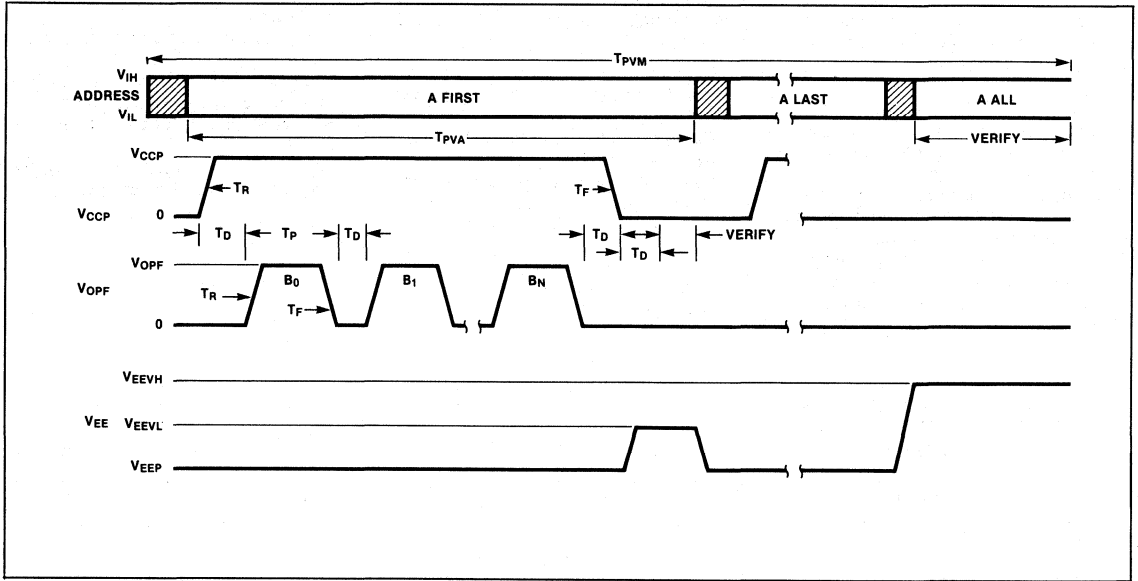
PROGRAMMING SYSTEM SPECIFICATIONS¹ (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER ⁴	TEST CONDITIONS	LIMITS ²		UNIT	
		Min	Max		
V_{IH} V_{IL}	Address Inputs Program or verify	$I_{IH} = 300\mu\text{A}$ $I_{IL} = 250\mu\text{A}$ $I_{IL} = -50\mu\text{A}$	-.85 V_{EE}	-.25 -1.80	V
V_{OH} V_{OL}	Outputs (verify)	7.4k Ω Load to V_{EE}	-1.0	-1.4	V
I_{OPF} V_{OPF} ⁵	Programming pulse	$V_{OUT} = 1.8\text{V}$ $V_{OUT} = 2.2\text{V}$ $R_1 = 1.8\text{K}, R_2 = 5.6\text{K}$	2.0 6.0	3.0 6.8	mA V
V_{EEP} V_{EEVL} V_{EEVH}	Supply voltage V_{EE} To program ³ To verify	$I_{EE} = -200\text{mA}$ (Peak - 350mA) $I_{EE} = -200\text{mA}$	-5.7 -5.7 -4.9	-5.5 -5.5 -4.7	V
V_{CC1} V_{CCP}	Programming supply V_{CC1} To verify To program ³	$I_{LOAD} = 5\text{mA}$ $I_{LOAD} = 10\text{mA}$ (Peak 150mA)	-0.1 6.0	0.1 6.8	V
T_P T_R, T_F	Programming pulse width Rise and fall time	10% to 90%	100 0.1	125 1.0	μsec μsec
T_D T_{PVA} T_{PVM} F_L	V_{CCP} and V_{OPF} Pulse sequence delay Program-verify cycle Program-verify cycle Fusing attempts per link	Single address Continuous	5	1 20 1	μsec msec sec cycle

7

10149 PROGRAMMING SEQUENCE

TYPICAL 10149 PROGRAMMING SEQUENCE



100149 PROGRAMMING PROCEDURE

PROGRAMMING NOTES

1. These are specifications which a Programming System must satisfy in order to be qualified by Signetics.
2. All voltages are referenced to V_{CC2} , pin 16.
3. Supply should be bypassed to V_{CC2} with a capacitor so that the voltage stays within specified limits during the entire fusing cycle.
4. Refer to typical Programming Circuit and Typical Programming Sequence for definition of parameters.
5. V_{OPF} must be an open circuit during verify. It may be 0 volts or an open circuit while programming other outputs.

PROGRAMMING PROCEDURE

The unprogrammed state is logical "0" (low outputs). To program "1s", proceed as follows:

1. Terminate all outputs with a 1.8K resistor in series with a 5.6K resistor to V_{EE} .
2. Connect \overline{CE} to V_{EE} or leave it open.
3. Apply V_{EEP} to the V_{EE} pin.
4. Select the word to be programmed using V_{IH} and V_{IL} levels.
5. After Address is valid, raise V_{CC1} to V_{CCP} .
6. After T_D , apply the V_{OPF} pulse to the 1.8K resistor on the output to be programmed.

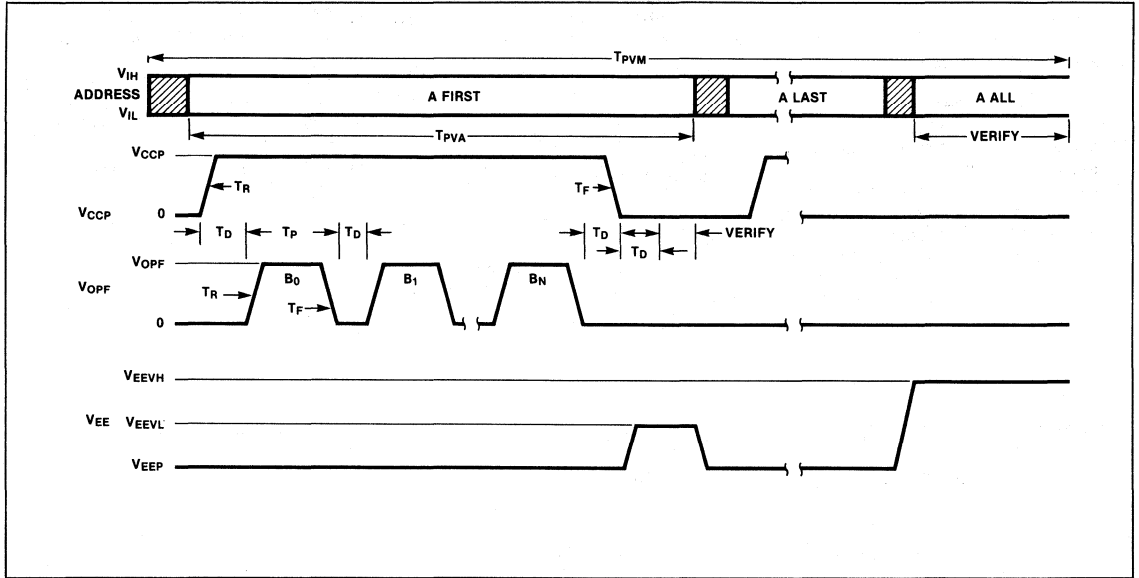
7. After T_D , apply the V_{OPF} pulse to the next output to be programmed on the same word.
8. Bring V_{CC1} to 0 volts and apply V_{EEVL} to the V_{EE} pin.
9. After T_D , verify the code on the four outputs using V_{OH} and V_{OL} limits.
10. Repeat steps 3-9 for all addresses to be programmed.
11. Change V_{EE} to V_{EEVH} and verify the code at all memory locations.

PROGRAMMING SYSTEM SPECIFICATIONS¹ (Testing of these limits may cause programming of device.) $T_A = +25^\circ\text{C}$

PARAMETER ⁴	TEST CONDITIONS	LIMITS ²		UNIT	
		Min	Max		
V_{IH} V_{IL}	Address Inputs Program or verify	$I_{IH} = 300\mu\text{A}$ $I_{IL} = 250\mu\text{A}$ $I_{IL} = -50\mu\text{A}$	-.85 V_{EE}	-.25 -1.80	V
V_{OH} V_{OL}	Outputs (verify)	7.4k Ω Load to V_{EE}	-1.0	-1.4	V
I_{OPF} V_{OPF} ⁵	Programming pulse	$V_{OUT} = 1.8\text{V}$ $V_{OUT} = 2.2\text{V}$ $R_1 = 1.8\text{K}, R_2 = 5.6\text{K}$	2.0 6.0	3.0 6.8	mA V
V_{EEP} V_{EEVL} V_{EEVH}	Supply voltage V_{EE} To program ³ To verify	$I_{EE} = -200\text{mA}$ (Peak -350mA) $I_{EE} = -200\text{mA}$	-5.7 -4.9 -4.3	-5.5 -4.7 -4.1	V
V_{CCI} V_{CCP}	Programming supply V_{CCI} To verify To program ³	$I_{LOAD} = 5\text{mA}$ $I_{LOAD} = 10\text{mA}$ (Peak 150mA)	-0.1 6.0	0.1 6.8	V
T_P T_R, T_F	Programming pulse width Rise and fall time	10% to 90%	100 0.1	125 1.0	μsec μsec
T_D T_{PVA} T_{PVM} F_L	V_{CCP} and V_{OPF} Pulse sequence delay Program-verify cycle Program-verify cycle Fusing attempts per link	Single address Continuous	5	1 20 1	μsec msec sec cycle

100149 PROGRAMMING SEQUENCE

TYPICAL 100149 PROGRAMMING SEQUENCE



Section 8 PROMs, Low-Complexity

256-BIT BIPOLAR PROM (32 × 8)

82S23 (O.C.)/82S123 (T.S.)

DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S23 and 82S123 devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S23 and 82S123 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S23/123, N or F, and for the military temperature range (-55°C to +125°C) specify S82S23/123, F or W.

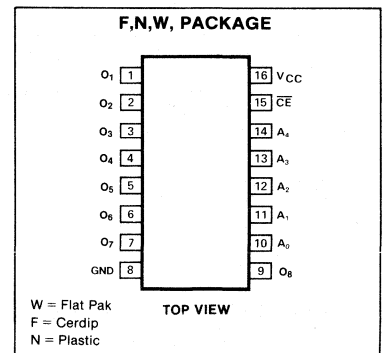
FEATURES

- **Address access time:**
N82S23/123: 50ns max
S82S23/123: 65ns max
- **Power dissipation: 1.3mW/bit typ**
- **Input loading:**
N82S23/123: -100µA max
S82S23/123: -150µA max
- **On-chip address decoding**
- **Output options:**
82S23: Open collector
82S123: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

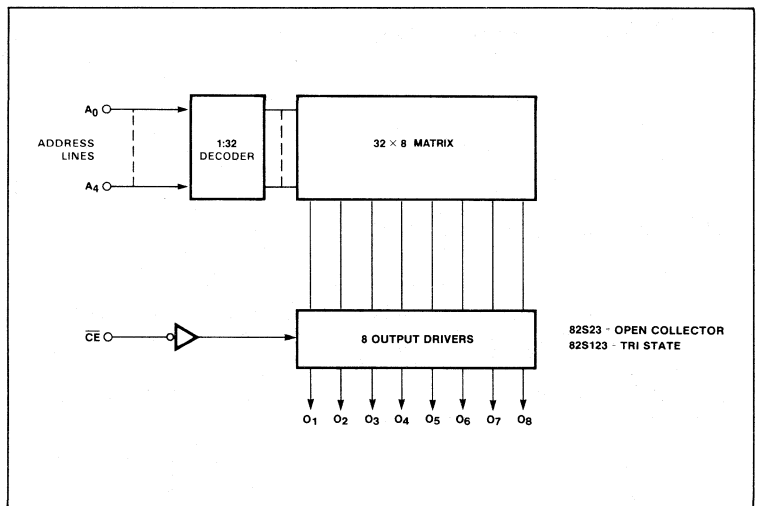
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC}	Supply voltage	+7
V _{IN}	Input voltage	+5.5
V _{OH}	Output voltage	
	High (82S23)	+5.5
V _O	Off-state (82S123)	+5.5
T _A	Temperature range	
	Operating	
	N82S23/123	0 to +75
	S82S23/123	-55 to +125
T _{STG}	Storage	-65 to +150

256-BIT BIPOLAR PROM (32 × 8)

82S23 (O.C.)/82S123 (T.S.)

DC ELECTRICAL CHARACTERISTICS N82S23/123: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S23/123: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1, 2}	N82S23/123			S82S23/123			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp I _{IN} = -18mA	2.0		0.85 -1.2	2.0		0.8 -1.2	V
V _{OL} V _{OH}	Output voltage Low High C _E = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.45	2.4		0.5	V
I _{IL} I _{IH}	Input current Low High V _{IN} = 0.45V V _{IN} = 5.5V			-100 50			-150 50	μA
I _{OLK} I _{O(OFF)}	Output current Leakage (82S23) Hi-Z state (82S123) C _E = High, V _{OUT} = 5.5V C _E = High, V _{OUT} = 5.5V C _E = High, V _{OUT} = 0.5V			40 40 -40			50 50 -50	μA μA
I _{OS}	Short circuit (82S123) ³ C _E = Low, V _{OUT} = 0V, High stored	-20		-90	-20		-100	mA
I _{CC}	V _{CC} supply current C _E = High, V _{CC} = 5.0V			77			85	mA
C _{IN} C _{OUT}	Capacitance Input Output V _{IN} = 2.0V V _{OUT} = 2.0V		5 8			5 8		pF

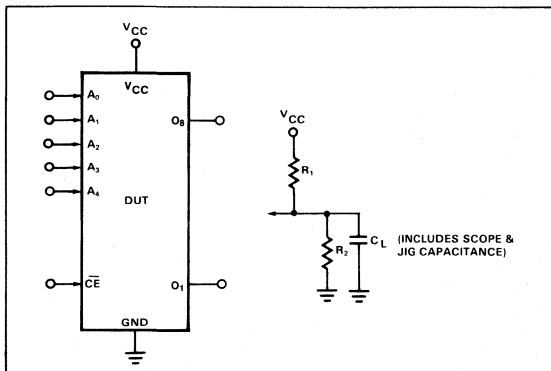
AC ELECTRICAL CHARACTERISTICS R₁ = 270Ω, R₂ = 600Ω, C_L = 30pF
 N82S23/123: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S23/123: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S23/123			S82S23/123			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T _{AA} ⁴ T _{CE}	Output Output	Address Chip enable		45	50 35			65 40	ns
T _{CD}	Output	Chip disable			35			40	ns

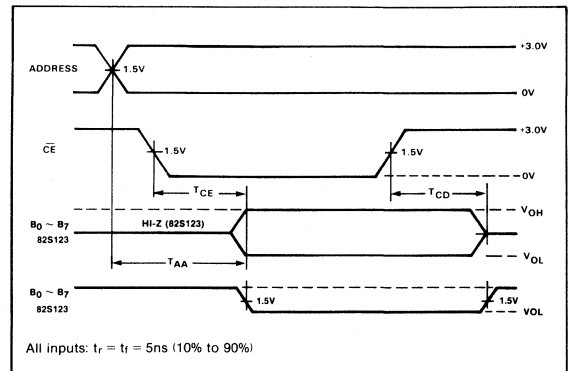
NOTES

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



1024-BIT BIPOLAR PROM (256 × 4)

82S126 (O.C.)/82S129 (T.S.)

DESCRIPTION

The 82S126 and 82S129 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S126 and 82S129 devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S126 and 82S129 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S126/129, F or N, and for the military temperature range (-55°C to +125°C) specify S82S126/129, F or R.

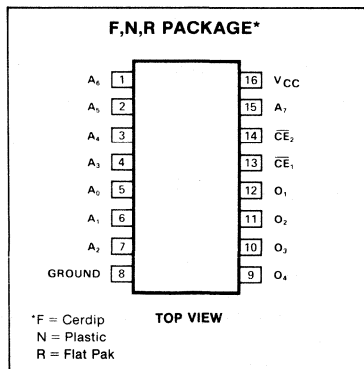
FEATURES

- **Address access time:**
N82S126/129: 50ns max
S82S126/129: 70ns max
- **Power dissipation: 0.5mW/bit typ**
- **Input loading:**
N82S126/129: -100µA max
S82S126/129: -150µA max
- **On-chip address decoding**
- **Output options:**
82S126: Open collector
82S129: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

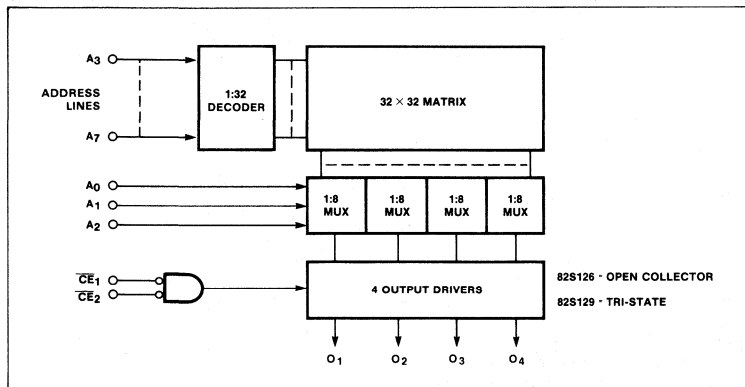
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control logic
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
Output voltage		Vdc
V _{OH} High (82S126)	+5.5	
V _O Off-state (82S129)	+5.5	
Temperature range		°C
T _A Operating		
N82S126/129	0 to +75	
S82S126/129	-55 to +125	
T _{STG} Storage	-65 to +150	



1024-BIT BIPOLAR PROM (256 × 4)

82S126 (O.C.)/82S129 (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S126/129: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S126/129: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1, 2}	N82S126/129			S82S126/129			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp I _{IN} = -18mA	2.0		.85 -1.2	2.0		.80 -1.2	V
V _{OL} V _{OH}	Output voltage Low High (82S129) C _{E1,2} = Low I _{OUT} = 16mA I _{OUT} = -2.0mA	2.4		0.45	2.4		0.5	V
I _{IL} I _{IH}	Input current Low High V _{IN} = 0.45V V _{IN} = 5.5V			-100 40			-150 50	μA
I _{OLK} I _{O(OFF)}	Output current Leakage (82S126) Hi-Z state (82S129) C _{E1} or C _{E2} = High, V _{OUT} = 5.5V C _{E1} or C _{E2} = High, V _{OUT} = 5.5V C _{E1} or C _{E2} = High, V _{OUT} = 0.5V			40 40 -40			60 60 -60	μA μA
I _{OS}	Short circuit (82S129) ³ C _{E1,2} = Low, V _{OUT} = 0V, Stored high	-20		-70	-15		-85	mA
I _{CC}	V _{CC} supply current V _{CC} = 5.0V			120			125	mA
C _{IN} C _{OUT}	Capacitance Input Output C _{E1} or C _{E2} = High V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS

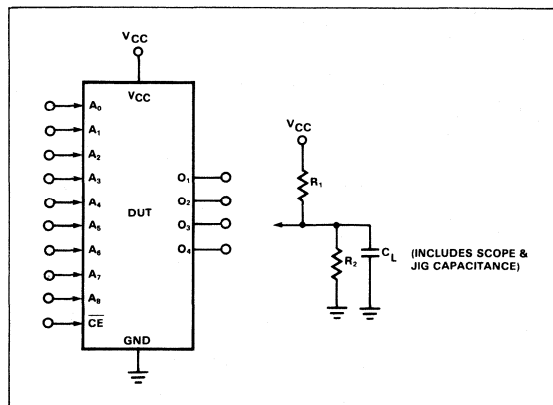
R₁ = 270Ω, R₂ = 600Ω, C_L = 30pF
 N82S126/129: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S126/129: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S126/129			S82S126/129			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T _{AA} ⁴ T _{CE}	Access time Output Output	Address Chip enable		40	50			70 35	ns
T _{CD}	Disable time Output	Chip disable			25			35	ns

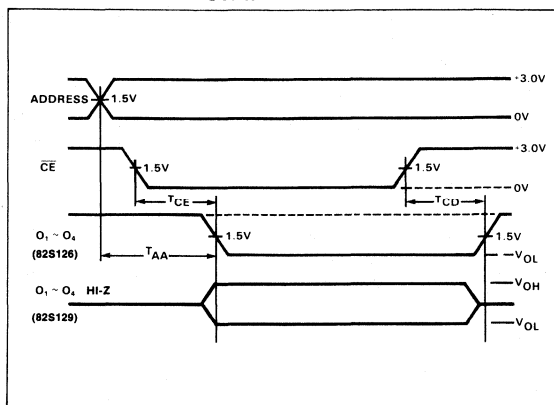
NOTES

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



1024-BIT ECL PROM (256 × 4)

10149

DESCRIPTION

The 10149 is field programmable, meaning that custom patterns are immediately available by following the fusing procedures given in this data manual. The device is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 10149 is suitable for use in high performance ECL systems. The outputs are capable of driving 50Ω loads.

A chip enable input is provided for ease of memory expansion.

FEATURES

- Address access time: 20ns max
- Power dissipation: 0.66mW/bit typ
- High impedance inputs (50kΩ pulldown)
- Open emitter outputs (50Ω drive)
- On-chip address decoding
- No separate fusing pins
- Fully compatible with ECL 10K series

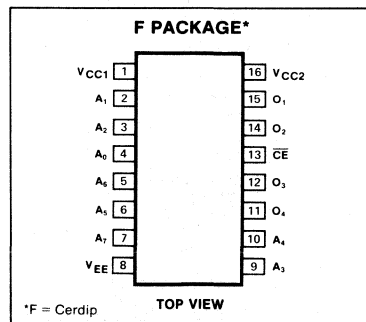
APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

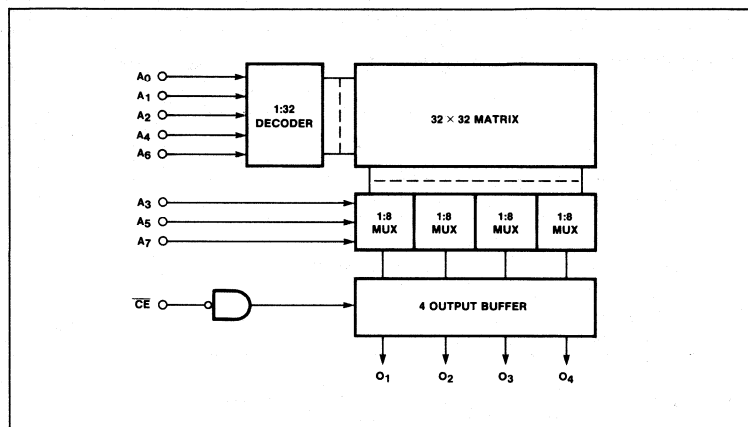
RECOMMENDED OPERATING RANGES

- $V_{CC1} = V_{CC2} = GND$
- $V_{EE} = -5.2V \pm 5\%$
- $T_A = -30^\circ C$ to $+85^\circ C$ ambient

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER ¹	RATING	UNIT	
V_{EE}	Supply voltage ($V_{CC} = 0$)	8	Vdc
V_{IN}	Input voltage ($V_{CC} = 0$)	0 to V_{EE}	Vdc
I_O	Output source current	40	mAdc
T_A	Operating	-30 to +85	°C
T_J	Operating junction	150	
T_{STG}	Storage	-55 to +165	

1024-BIT ECL PROM (256 × 4)

10149

DC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2} = 0V$, $V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2V$

PARAMETER ¹	TEST CONDITIONS	-30°C		+25°C			+85°C		UNIT
		Min	Max	Min	Typ ⁴	Max	Min	Max	
Input voltage ^{2,3} V_{IL} Low V_{IH} High V_{ILA} Low threshold V_{IHA} High threshold		-1.890		-1.850			-1.825		V
			-0.890			-0.810		-0.700	
			-1.500			-1.475		-1.440	
			-1.205		-1.105		-1.035		
Output voltage V_{OL} Low V_{OH} High	$V_{IH} = \text{max}$	-1.89	-1.675	-1.85		-1.65	-1.825	-1.615	V
	$V_{IL} = \text{min}$	-1.06	-0.89	-0.96		-0.81	-0.89	-0.70	
V_{OLA} Low threshold V_{OHA} High threshold	$V_{IHA} = \text{min}$, $V_{ILA} = \text{max}$		-1.655			-1.63		-1.595	
		-1.08		-0.98			-0.91		
Input current I_{IL} Low I_{IH} High	$V_{IH} = \text{min}$			0.5					μA
	$V_{IL} = \text{max}$		250			250		250	
I_{EE} Supply drain current	$V_{EE} = -5.2V$		160		150	160		160	mA

AC ELECTRICAL CHARACTERISTICS $V_{EE} = -5.2V \pm 5\%$, $-30^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
 $V_{CC1} = V_{CC2} = 0V$, $R_L = 50\Omega$ to $-2V$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁴	Max	
Access time T_{AA} T_{CE}	Output	Address		14	20	ns
		Chip enable		4	8	
	Output	Chip disable		4	8	
T_{CD} Disable time	Output	Chip disable		4	8	ns
Rise and fall time						
t_+ Rise time (20-80%)				4.0		ns
t_- Fall time (80-20%)				4.0		

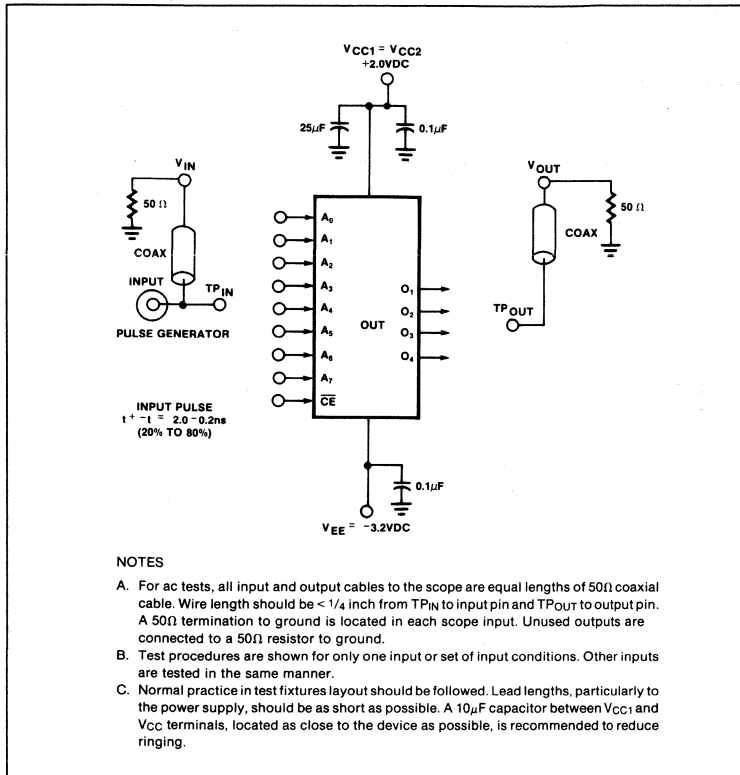
NOTES

- All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
- $V_{dc} \pm 1\%$.
- Each ECL 10K series device has been designed to meet the dc specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50 Ω resistor to -2V.
- Typical values are at $V_{EE} = -5.2V$, $T_A = 25^\circ\text{C}$

1024-BIT ECL PROM (256 × 4)

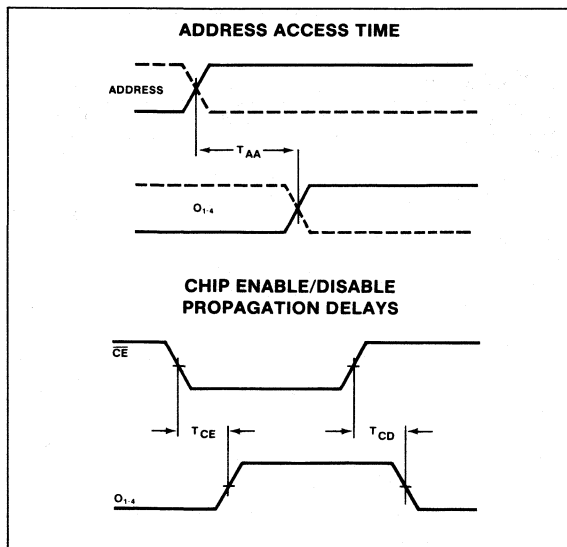
10149

TEST LOAD CIRCUIT



8

VOLTAGE WAVEFORMS



1024-BIT ECL PROM (256 × 4)

100149

DESCRIPTION

The 100149 is field programmable, meaning that custom patterns are immediately available by following the fusing procedures given in this data manual. The device is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 100149 is suitable for use in high performance ECL systems. The outputs are capable of driving 50Ω loads.

A chip enable input is provided for ease of memory expansion.

FEATURES

- Address access time: 20ns max
- Power dissipation: 0.66mW/bit typ
- High impedance inputs (50kΩ pulldown)
- Open emitter outputs (50Ω drive)
- On-chip address decoding
- No separate fusing pins
- Fully compatible with ECL 100K series

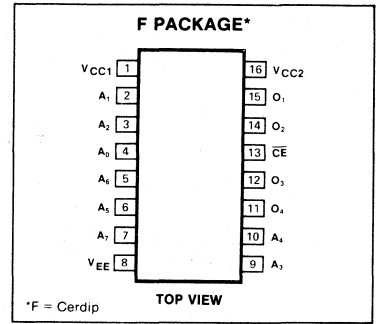
APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

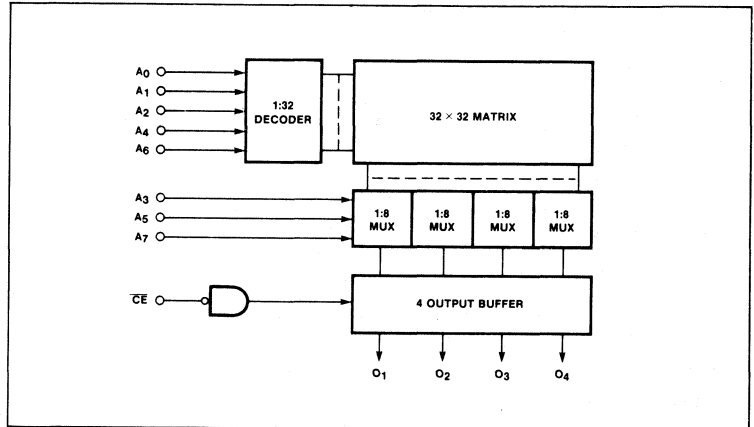
RECOMMENDED OPERATING RANGES

- $V_{CC1} = V_{CC2} = GND$
- $V_{EE} = -4.5V \pm 5\%$
- $T_A = 0^\circ C$ to $+85^\circ C$ ambient

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER ¹	RATING	UNIT
V _{EE}	- 8	Vdc
V _{IN}	0 to V _{EE}	Vdc
I _O	40	mAdc
Temperature range		
T _A	0 to + 85	°C
T _J	150	
T _{STG}	- 55 to + 165	

1024-BIT ECL PROM (256 × 4)

100149

DC ELECTRICAL CHARACTERISTICS³ $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, 0^\circ C \leq T_A \leq +85^\circ C$

PARAMETER	TEST CONDITIONS	LIMITS			UNIT
		Min	Typ ⁵	Max	
Input voltage					V
V _{IL} LOW		-1.810			
V _{IH} HIGH				-0.880	
V _{ILA} Threshold LOW				-1.475	
V _{IHA} Threshold HIGH		-1.165			
Output voltage					V
V _{OL} LOW	V _{IL} = MIN	-1.810		-1.620	
V _{OH} HIGH	V _{IH} = MAX	-1.025		-0.880	
V _{OLA} Threshold LOW	V _{IL} = MAX			-1.610	
V _{OHA} Threshold HIGH	V _{IH} = MIN	-1.035			
Input current					μA
I _{IL} LOW	V _{IL} = MIN	0.5			
I _{IH} HIGH	V _{IH} = MAX			220	
I _{EE} Supply current	V _{EE} = -4.5V		150	180	mA

AC ELECTRICAL CHARACTERISTICS³ $V_{CC} = 0V, V_{EE} = -4.5V \pm 5\%, R_L = 50\Omega$ to $-2V, 0^\circ C \leq T_A \leq +85^\circ C$

PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
Access time						ns
T _{AA}	Output	Address	15	20		
T _{CE}	Output	Chip enable	5	8		
T _{CD}	Output	Chip disable	5	8		ns
Rise and fall time						ns
t ₊ Rise time (20-80%)			4.0			
t ₋ Fall time (80-20%)			4.0			

NOTES

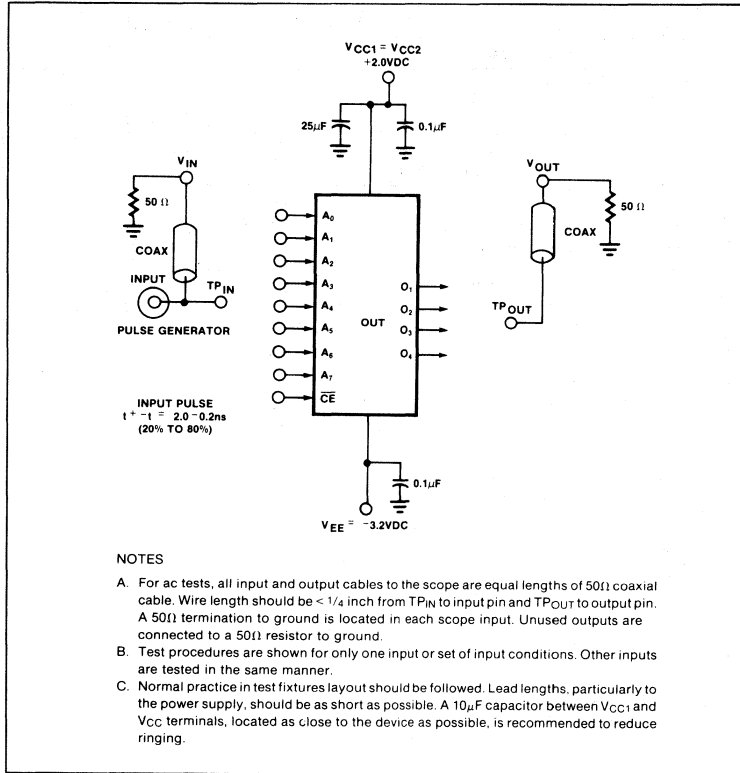
1. All voltage measurements are referenced to the ground terminal. Terminals not specifically referenced are left electrically open.
2. V_{dc} ± 1%.
3. Each ECL 100K series device has been designed to meet the dc specification after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 400 linear fpm is maintained. Voltage levels will shift approximately 4mV with an air flow of 200 linear fpm. Outputs are terminated through a 50Ω resistor to -2V.
4. For current measurements, maximum is defined as the maximum absolute value.
5. Typical values are at V_{EE} = -4.5V, T_A = 25°C.

8

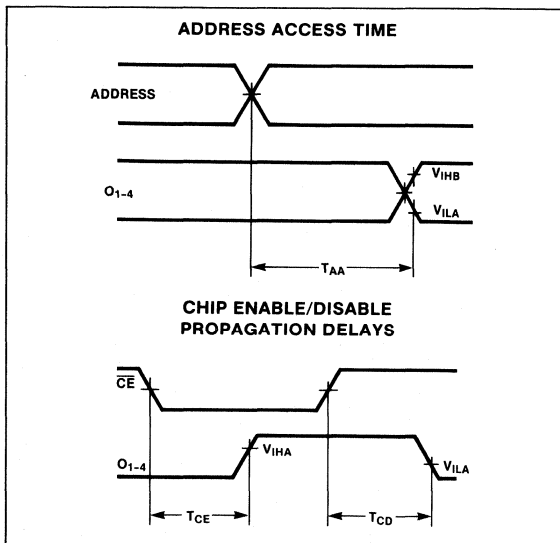
1024-BIT ECL PROM (256 × 4)

100149

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



2048-BIT BIPOLAR PROM (512 × 4)

82S130 (O.C.)/82S131 (T.S.)

DESCRIPTION

The 82S130 and 82S131 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82S130 and 82S131 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S130 and 82S131 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0° to +75°C) specify N82S130/131, F or N, and for the military temperature range (-55°C to +125°C) specify S82S130/131, F or R.

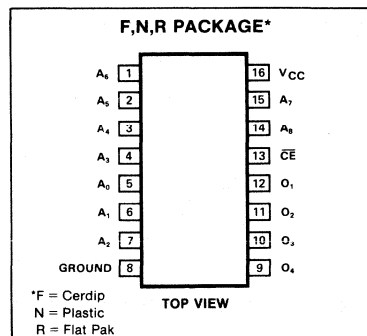
FEATURES

- **Address access time:**
N82S130/131: 50ns max
S82S130/131: 70ns max
- **Power dissipation:** 0.3mW/bit typ
- **Input loading:**
N82S130/131: -100µA max
S82S130/131: -150µA max
- **On-chip address decoding**
- **Output options:**
82S130: Open collector
82S131: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

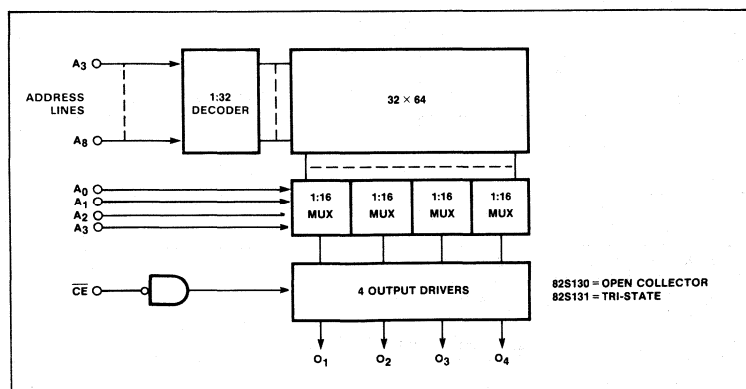
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
Output voltage		Vdc
V _{OH} High (82S130)	+5.5	
V _O Off-state (82S131)	+5.5	
Temperature range		°C
T _A Operating		
N82S130/131	0 to +75	
S82S130/131	-55 to +125	
T _{STG} Storage	-65 to +150	

2048-BIT BIPOLAR PROM (512 x 4)

82S130 (O.C.)/82S131 (T.S.)

DC ELECTRICAL CHARACTERISTICS N82S130/131: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S130/131: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1,2}	N82S130/131			S82S130/131			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V _{IL} Input voltage Low	I _{IN} = -18mA	2.0		.85	2.0		.80	V
V _{IH} High								
V _{IC} Clamp								
V _{OL} Output voltage Low	CE = Low I _{OUT} = 16mA	2.4		0.45	2.4		0.5	V
V _{OH} High (82S131)								
I _{IL} Input current Low	V _{IN} = 0.45V			-100			-150	μA
I _{IH} High								
I _{OLK} Output current Leakage (82S130)	CE = high, V _{OUT} = 5.5V			40			60	μA
I _{O(OFF)} Hi-Z state (82S131)								
I _{OS} Short circuit (82S131) ³								
I _{CC} V _{CC} supply current	CE = Low, V _{OUT} = 0V, Stored high	-20		-70	-15		-85	mA
C _{IN} Input capacitance	CE = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5				5	pF
C _{OUT} Output capacitance								

AC ELECTRICAL CHARACTERISTICS R₁ = 270Ω, R₂ = 600Ω, C_L = 30pF

N82S130/131: 0° ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

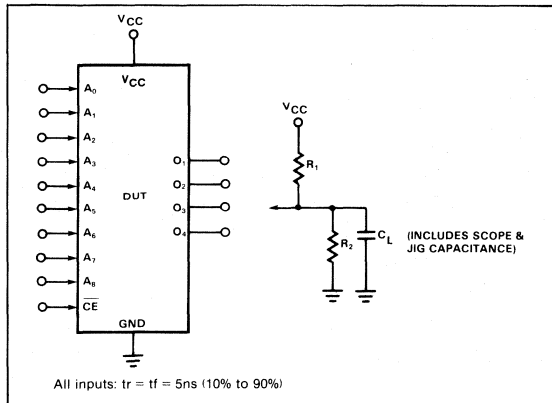
S82S130/131: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S130/131			S82S130/131			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T _{AA} ⁴ Access time	Output	Address			50			70	ns
T _{CE} Chip enable									
T _{CD} Disable time	Output	Chip disable			30			40	ns

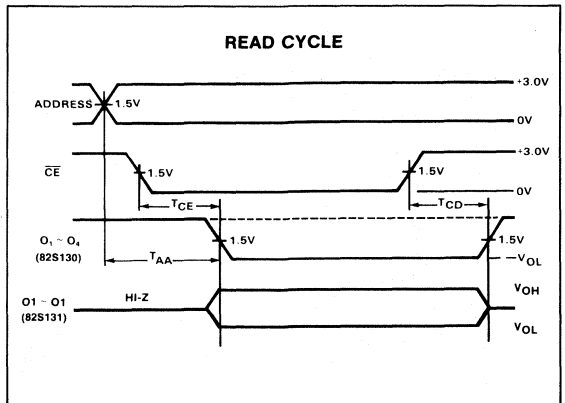
NOTES

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Section 9
PROMs,
4K-Bit

4096-BIT BIPOLAR PROM (512 × 8)

82S115 (T.S.)

DESCRIPTION

The 82S115 is field programmable and includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations. A D-type latch is used to enable the tri-state output drivers. In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the bit drivers will be controlled solely by \overline{CE}_1 and CE_2 lines.

In the Latched Read mode, outputs are held in their previous state (high, low, or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

The 82S115 is available in the commercial and military temperature range. For the commercial temperature range (0°C to +75°C) specify N82S115, F or N, and for the military temperature range (-55°C to +125°C) specify S82S115, F, R, or I.

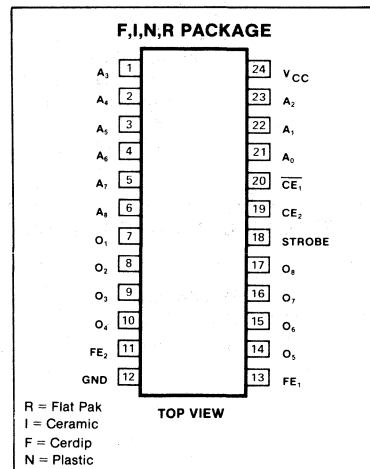
FEATURES

- **Address access time:**
N82S115: 60ns max
S82S115: 90ns max
- **Power dissipation:** 165 μ W/bit typ
- **Input loading:**
N82S115: -100 μ A max
S82S115: -150 μ A max
- **On-chip storage latches**
- **Schottky clamped**
- **Fully TTL compatible**

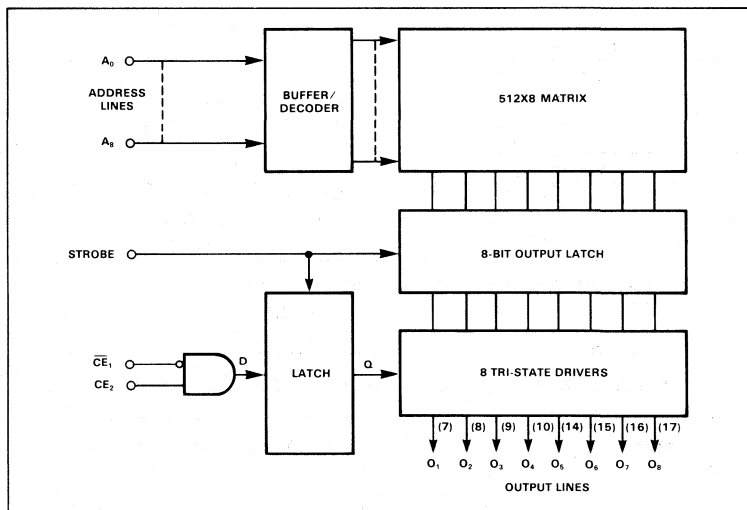
APPLICATIONS

- **Microprogramming**
- **Hardwire algorithms**
- **Character generation**
- **Control store**
- **Sequential controllers**

PIN CONFIGURATIONS



BLOCK DIAGRAM



4096-BIT BIPOLAR PROM (512 × 8)

82S115 (T.S.)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	V _{dc}
V _{IN} Input voltage	+5.5	V _{dc}
T _A Operating Temperature range		°C
N82S115	0 to +75	
S82S115	-55 to +125	
T _{STG} Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS N82S115: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S115: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ⁵	N82S115			S82S115			UNIT
		Min	Typ ⁸	Max	Min	Typ	Max	
V _{IL} Input voltage Low	I _{IN} = -18mA	2.0		.85	2.0		.8	V
V _{IH} Input voltage High								
V _{IC} Input voltage Clamp								
V _{OL} Output voltage Low	C _{E1} = Low, C _{E2} = High, I _{OUT} = 9.6mA	2.7	0.4	0.45	2.4		0.5	V
V _{OH} Output voltage High								
I _{IL} Input current Low								
I _{IH} Input current High	V _{IN} = 0.45V							
I _{IH} Input current High	V _{IN} = 5.5V			-100			-150	μA
I _{OS} Output current Hi-Z state	C _{E1} = High or C _{E2} = Low, V _{OUT} = 5.5V C _{E1} = High or C _{E2} = Low, V _{OUT} = 0.5V C _{E1} = Low, C _{E2} = High, V _{OUT} = 0V, High Stored	-20		40	-15		100	μA
I _{OS} Output current Short circuit ¹								
I _{CC} V _{CC} supply current								
I _{CC} V _{CC} supply current			130	175			185	mA
C _{IN} Capacitance Input	C _{E1} = High or C _{E2} = Low, V _{CC} = 5.0V V _{IN} = 2.0V		5				5	pF
C _{OUT} Capacitance Output								
			8				8	

AC ELECTRICAL CHARACTERISTICS R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82S115: 0° ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S115: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	TEST CONDITIONS	N82S115			S82S115			UNIT
				Min	Typ ⁸	Max	Min	Typ	Max	
T _{AA} ⁶ Access time	Output	Address	Latched or transparent read ^{2,4}	40	60			90	ns	
T _{CE} Chip enable										
T _{CD} Disable time	Output	Chip disable		20	40			55	ns	
T _{CDS} Setup time	Output	Chip enable		Latched read only ^{3,4}	40	10		50		ns
T _{CDH} Hold time										
T _{ADH} Hold time	Output	Address	0				5			
T _{SW} Pulse width Strobe			30		15		40		ns	
T _{SL} Latch time Strobe			60	35		90		ns		
T _{DL} Delatch time Strobe					35			45	ns	

NOTES on following page.

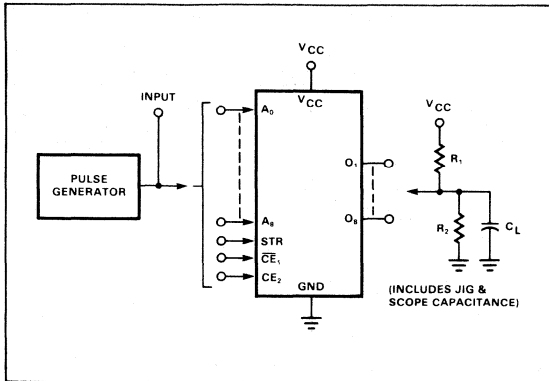
4096-BIT BIPOLAR PROM (512 × 8)

82S115 (T.S.)

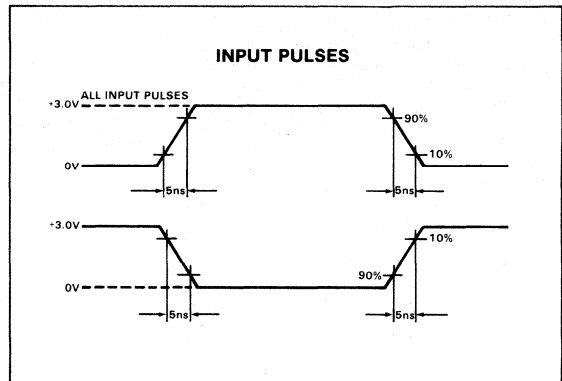
NOTES

1. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
2. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed to T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or high impedance state after it has been enabled.
3. In latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
4. During operation the fusing pins FE1 and FE2 may be grounded or left floating.
5. Positive current is defined as into the terminal referenced.
6. Tested at an address cycle time of 1 μ sec.
7. Areas shown by crosshatch are latched data from previous address.
8. (Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$)

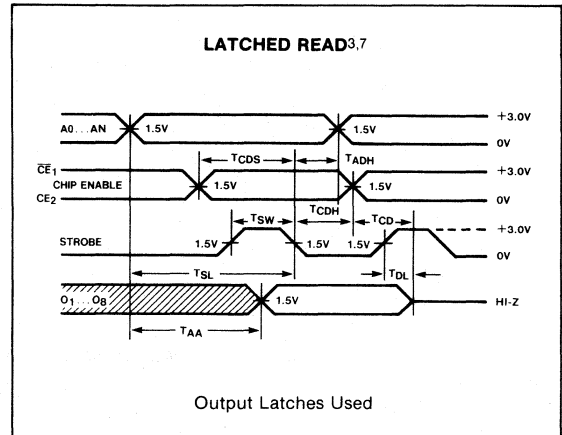
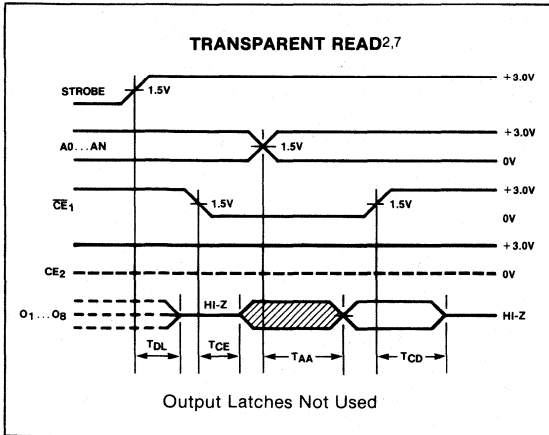
TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAMS



4096-BIT BIPOLAR PROM (1024 × 4)

82S137 (T.S.)

DESCRIPTION

The 82S137 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S137 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

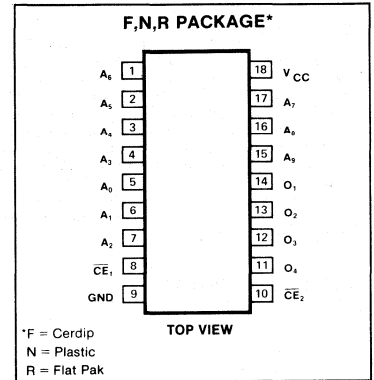
These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in bused organizations.

The 82S137 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S137, F or N, and for the military temperature range (-55°C to +125°C) specify S82S137, F or R.

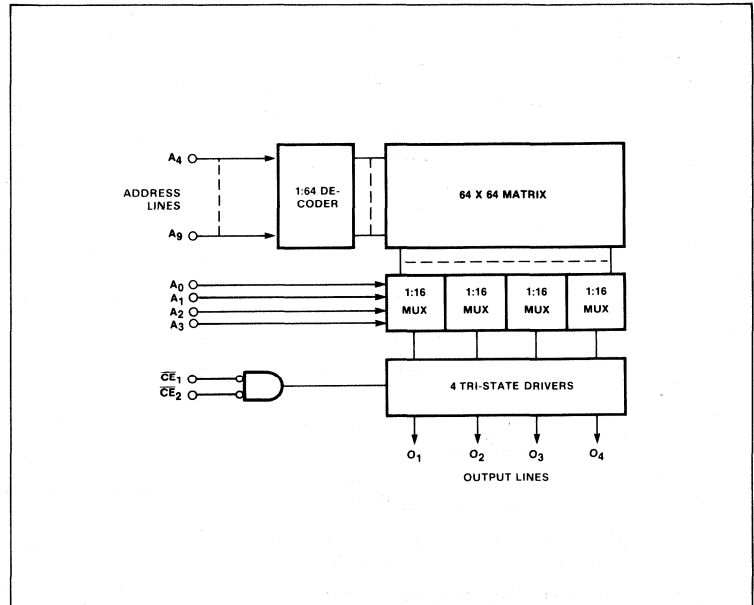
FEATURES

- **Address access time:**
N82S137: 60ns max
S82S137: 80ns max
- **Power dissipation: .13mW/bit typ**
- **Input loading:**
N82S137: -100µA max
S82S137: -150µA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Output voltage	+5.5	Vdc
V _O Off-state (82S137)		
Temperature range		°C
T _A Operating		
N82S137	0 to +75	
S82S137	-55 to +125	
T _{STG} Storage	-65 to +150	

4096-BIT BIPOLAR PROM (1024 × 4)

82S137 (T.S.)

DC ELECTRICAL CHARACTERISTICS N82S137; N82S137A: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82S137; S82S137A: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TEST CONDITIONS ^{1,2}	N82S137/137A			S82S137/137A			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{IL} V_{IH} V_{IC}	Input voltage Low High Clamp $I_{IN} = -18\text{mA}$	2.0		.85 -1.2	2.0		.80 -1.2	V
V_{OL} V_{OH}	Output voltage Low High $\overline{CE}_{1,2} = \text{Low}$ $I_{OUT} = 16\text{mA}$ $I_{OUT} = -2\text{mA}$	2.4		0.45	2.4		0.5	V
I_{IL} I_{IH}	Input current Low High $V_{IN} = 0.45\text{V}$ $V_{IN} = 5.5\text{V}$			-100 40			-150 50	μA
$I_{O(OFF)}$	Output current Off-state $\overline{CE}_{1,2} = \text{High}$, $V_{OUT} = 0.5\text{V}$ $\overline{CE}_{1,2} = \text{High}$, $V_{OUT} = 5.5\text{V}$			40 -40 40			60 -60 60	μA μA
I_{OS}	Short circuit ³ $\overline{CE}_{1,2} = \text{Low}$, $V_{OUT} = 0\text{V}$, Stored high	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current $\overline{CE}_{1,2} = \text{High}$, $V_{CC} = 5.0\text{V}$			140			150	mA
C_{IN} C_{OUT}	Capacitance Input Output $V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$		5 8			5 8		pF

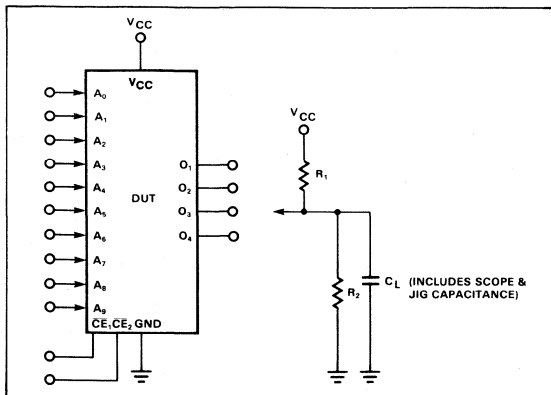
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$
 N82S137; N82S137A: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82S137; S82S137A: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TO	FROM	N82S137			S82S137		
			Min	Typ ⁵	Max	Min	Typ	Max
T_{AA} ⁴ T_{CE}	Access time Output Output	Address Chip enable		40 25	60 30			80 40
T_{CD}	Disable time Output	Chip disable		25	30			40

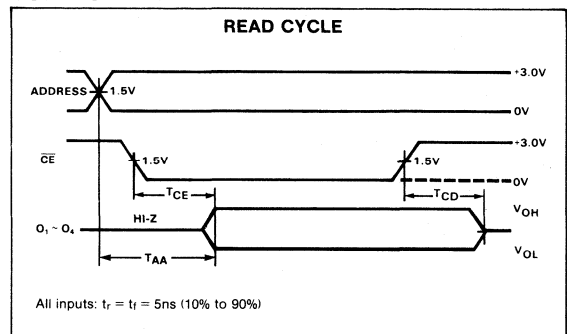
- NOTES
 1. Positive current is defined as into the terminal referenced.
 2. All voltages with respect to network ground.
 3. Duration of short circuit should not exceed 1 second.

4. Tested at an address cycle time of $1\mu\text{sec}$.
 5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



4096-BIT BIPOLAR PROM (1024 × 4)

82HS137/82HS137A (T.S.)

DESCRIPTION

The 82HS137 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82HS137 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

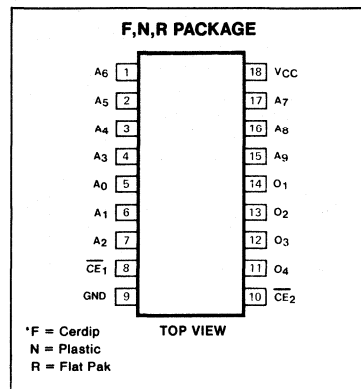
These devices include on-chip decoding and 2 chip enable inputs for ease of memory expansion. They feature tri-state outputs for optimization of word expansion in based organizations.

The 82HS137 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82HS137, F or N, or N82HS137A F or N, and for the military temperature range (-55°C to +125°C) specify S82HS137 F or R.

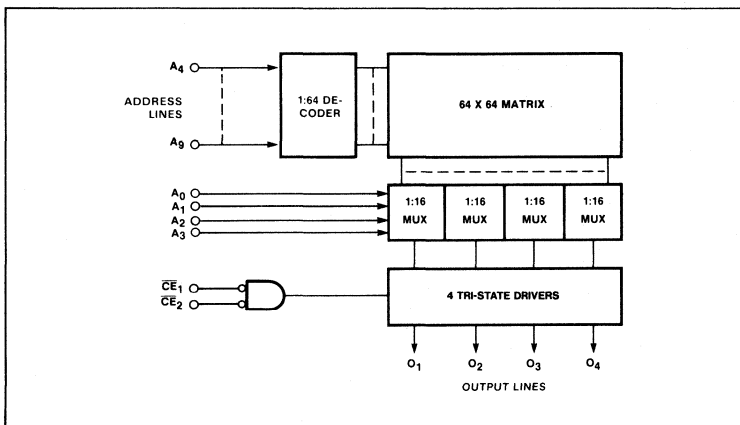
FEATURES

- **Address access time:**
 N82HS137: 45ns max
 N82HS137A: 35ns max
 S82HS137: 70ns max
- **Power dissipation: 13mW/bit typ**
- **Input loading:**
 N82HS137: -100µA max
 S82HS137: -150µA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Output voltage		Vdc
Off-state	+5.5	
Temperature range		°C
T _A Operating		
N82HS137	0 to +75	
S82HS137	-55 to +125	
T _{STG} Storage	-65 to +150	

4096-BIT BIPOLAR PROM (1024 × 4)

82HS137/82HS137A (T.S.)

DC ELECTRICAL CHARACTERISTICS N82HS137/N82HS137A: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82HS137: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TEST CONDITIONS ^{1, 2}	N82HS137/N82HS137A			S82HS137			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V_{IL} V_{IH} V_{IC}	Input voltage Low High Clamp			.85			.80	V
V_{OL} V_{OH}	Output voltage Low High			0.45			0.5	V
I_{IL} I_{IH}	Input current Low High			-100 40			-150 50	μA
$I_{O(OFF)}$	Output current Hi-Z state			40 -40			60 -60	μA
I_{OS}	Short circuit ³			40 -70	-15		60 -85	mA
I_{CC}	V_{CC} supply current			85 140			150	mA
C_{IN} C_{OUT}	Capacitance Input Output			5 8			5 8	pF

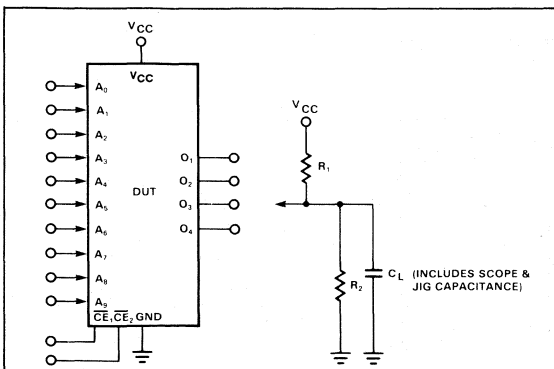
AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$
 N82HS137/N82HS137A: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82HS137; S82HS137A: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TO	FROM	N82HS137			N82HS137A			S82HS137			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	Min	Typ	Max	
T_{AA} ⁴	Access time	Output		35	45		30	35			70	ns
T_{CE}		Output	Address Chip enable		15	30		25			40	
T_{CD}	Disable time	Output	Chip disable		15	30		25			40	ns

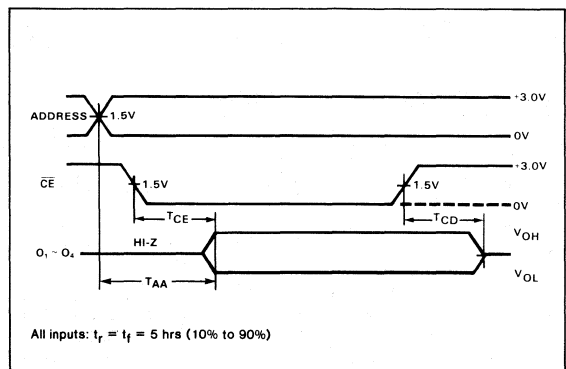
NOTES

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1 μsec .
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



4096-BIT BIPOLAR PROM (512 × 8)

82S140 (O.C.)/82S141 (T.S.)

DESCRIPTION

The 82S140 and 82S141 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82S140 and 82S141 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

Both 82S140 and 82S141 devices are available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S140/141, F or N and for the military temperature range (-55°C to +125°C) specify S82S140/141, F, or R.

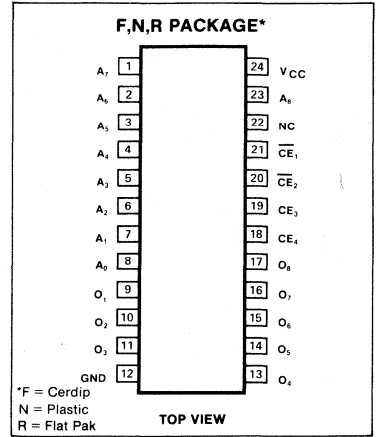
FEATURES

- **Address access time:**
N82S140/141: 60ns max
S82S140/141: 90ns max
- **Power dissipation:** .17mW/bit typ
- **Input loading:**
N82S140/141: -100µA max
S82S140/141: -150µA max
- **On-chip address decoding**
- **Output options:**
82S140: Open collector
82S141: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

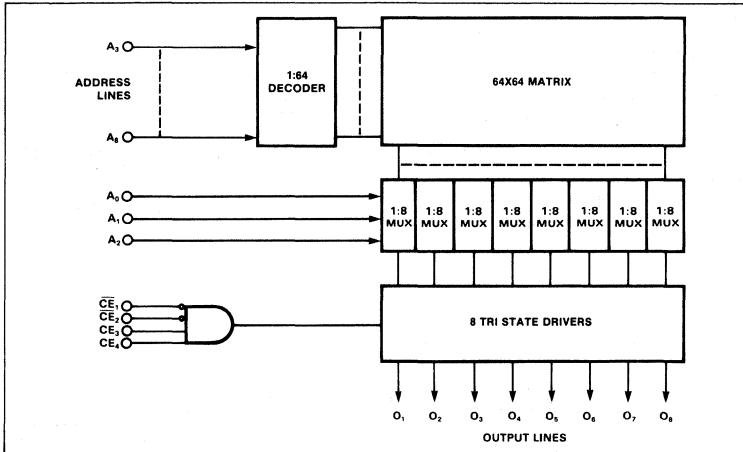
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+ 7	Vdc
V _{IN} Input voltage	+ 5.5	Vdc
Output voltage		Vdc
V _{OH} High (82S140)	+ 5.5	
V _O Off-state (82S141)	+ 5.5	
Temperature range		°C
T _A Operating		
N82S140/141	0 to +75	
S82S140/141	-55 to +125	
T _{STG} Storage	-65 to +150	

4096-BIT BIPOLAR PROM (512 × 8)

82S140 (O.C.)/82S141 (T.S.)

DC ELECTRICAL CHARACTERISTICS

N82S140/141: 0°C ≤ T_A ≤ 75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S140/141: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1, 2}	N82S140/141			S82S140/141			UNIT	
		Min	Typ ⁵	Max	Min	Typ ²	Max		
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp			.85			.80	V	
V _{OL} V _{OH}	Output voltage Low High (82S141)			0.45			0.5	V	
I _{IL} I _{IH}	Input current Low High			-100 40			-150 50	μA	
I _{OLK}	Output current Leakage (82S140)			40			60	μA	
I _{O(OFF)}	Hi-Z state (82S141)			-40			-60	μA	
I _{OS}	Short circuit (82S141) ³			-70		-15	-85	mA	
I _{CC}	V _{CC} supply current			140		175	140	185	mA
C _{IN} C _{OUT}	Capacitance Input Output			5 8			5 8	pF	

AC ELECTRICAL CHARACTERISTICS

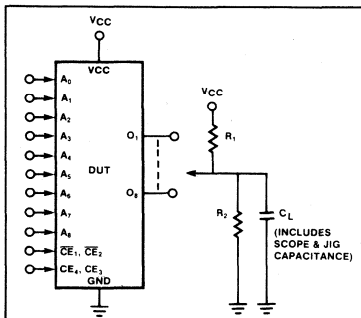
R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82S141: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S141: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S141			S82S141			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T _{AA} ⁴ T _{CE}	Access time Output	Address Chip enable		40	60		40	90	ns
T _{CD}	Disable time Output	Chip disable		20	40		20	50	ns

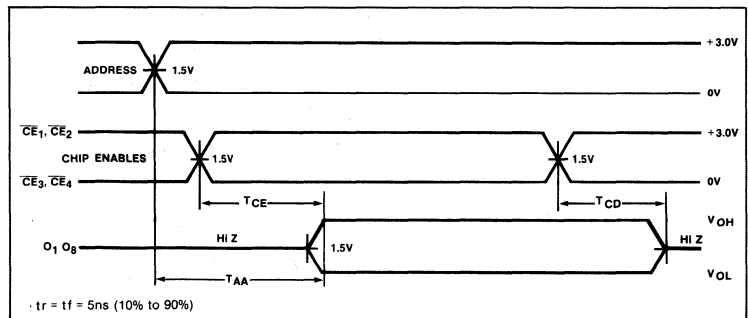
NOTES

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



4096-BIT BIPOLAR PROM (512 × 8)

82S147 (T.S.)

DESCRIPTION

The 82S147 is field-programmable, which means that custom patterns are immediately available by following the Signetics generic fusing procedure. The standard devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 82S147 includes on-chip decoding and one chip enable input for ease of memory expansion, and features three-state outputs for optimization of word expansion in based organizations.

The 82S147 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S147 F or N, and for the military temperature range (-55°C to +125°C) specify S82S147F.

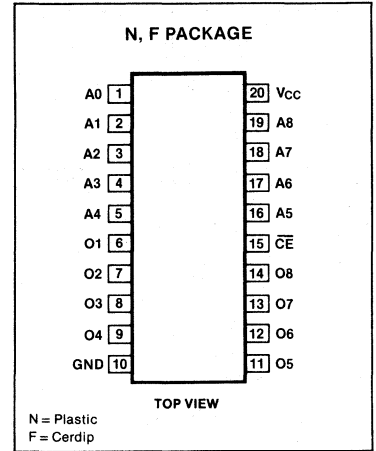
FEATURES

- Address access time:
N82S147: 60ns max
S82S147: 75ns
- Power dissipation: 625mW typ
- Input loading:
N82S147: -100µA max
S82S147: -150µA max
- One chip enable input
- On-chip address decoding
- No separate fusing pins
- Fully TTL compatible

APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

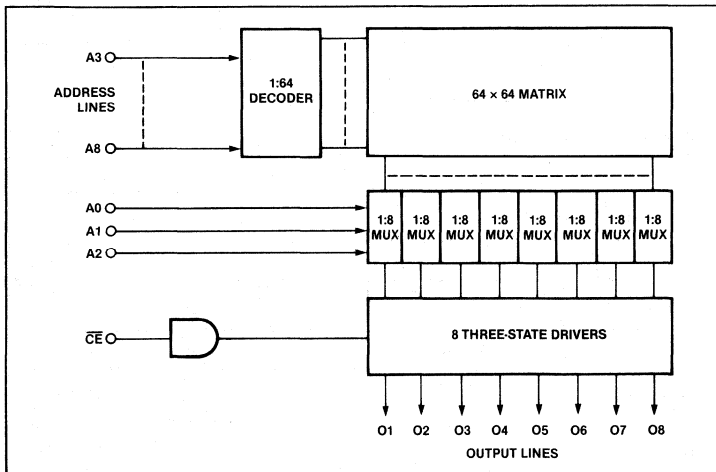
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC}	Power supply voltage	+7 Vdc
V _{IN}	Input voltage	+5.5 Vdc
V _O	Output voltage	+5.5 Vdc
	Temperature range	°C
T _A	Operating	0 to +75
T _{STG}	Storage	-65 to +150

BLOCK DIAGRAM



4096-BIT BIPOLAR PROM (512 × 8)

82S147 (T.S.)

DC ELECTRICAL CHARACTERISTICS N82S147: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S147: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITION ^{1,2}	N82S147			S82S147			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp I _{IN} = -18mA	2.0	-0.8	-1.2	2.0		-1.2	V
V _{OL} V _{OH}	Output voltage Low High I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	2.4		0.5	V
I _{IL} I _{IH}	Input current Low High V _{IN} = 0.45V V _{IN} = 5.5V			-100 40			-150 50	μA
I _{OLK} I _{O(OFF)} I _{OS}	Output current Hi-Z state Short circuit ³ C \bar{E} = High, V _{OUT} = 5.5V C \bar{E} = High, V _{OUT} = 0.5V C \bar{E} = Low, V _{OUT} = 0V	-20		40 -40 -70	-15		-60 60 -85	μA μA mA
I _{CC}	V _{CC} supply current C \bar{E} = Low		125	155			165	mA
C _{IN} C _{OUT}	Capacitance Input Output C \bar{E} = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS R1 = 470Ω, R2 = 1kΩ, C_L = 30pF
 N82S147: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S147: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

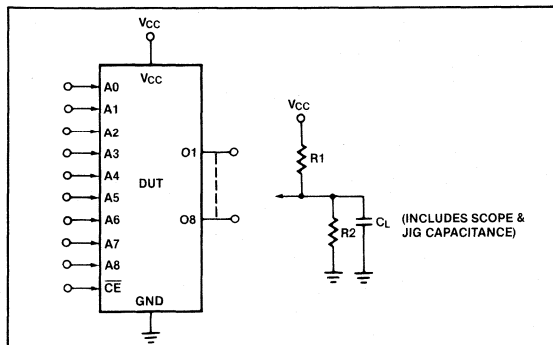
PARAMETER	TO	FROM	N82S147			S82S147			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T _{AA} ⁴ T _{CE}	Access time Output Output	Address Chip enable		45 20	60 35			75 45	ns
T _{CD}	Disable time Output	Chip disable		20	35			45	ns

NOTES

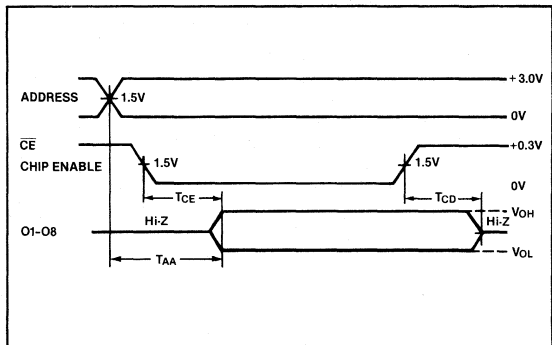
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.

4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



4096-BIT BIPOLAR PROM (512 × 8)

82HS147 (T.S.)

DESCRIPTION

The 82HS147 is field-programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard devices are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

The 82HS147 includes on-chip decoding and one chip enable input for ease of memory expansion, and features tri-state outputs for optimization of word expansion in bused organizations.

The 82HS147 device is available in the commercial temperature range (0°C to +75°C), and is specified as N82HS147, F, N.

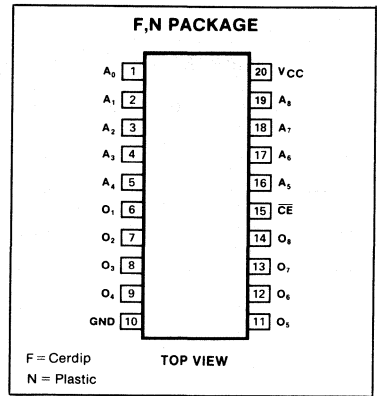
FEATURES

- Address access time: 45ns max
- Power dissipation: 853mW max
- Input loading: -100µA max
- One chip enable input
- On chip address decoding
- No separate fusing pins
- Fully TTL compatible

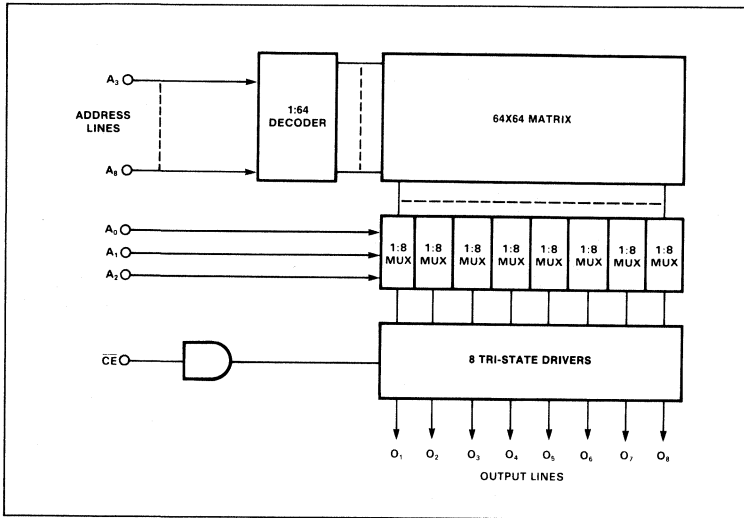
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Power supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Output voltage		Vdc
V _O Off-state	+5.5	Vdc
Temperature range		°C
T _A Operating	0 to +75	
T _{STG} Storage	-65 to +150	

4096-BIT BIPOLAR PROM (512 × 8)

82HS147 (T.S.)

DC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$.

PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT
		Min	Typ ⁵	Max	
V_{IL} V_{IH} V_{IC}	Input voltage ² Low High Clamp $I_{IN} = -18\text{mA}$	2.0		.85 -1.2	V
V_{OL} V_{OH}	Output voltage Low High $I_{OUT} = 9.6\text{mA}$ $\overline{CE} = \text{Low}, I_{OUT} = -2\text{mA}, \text{High stored}$	2.4		0.45	V
I_{IL} I_{IH}	Input current Low High $V_{IN} = 0.45\text{V}$ $V_{IN} = 5.5\text{V}$			-100 40	μA
I_{OLK} $I_{O(OFF)}$	Output current Leakage Hi-Z state $\overline{CE} = \text{High}, V_{OUT} = 5.5\text{V}$ $\overline{CE} = \text{High}, V_{OUT} = 0.5\text{V}$ $\overline{CE} = \text{High}, V_{OUT} = 5.5\text{V}$ $V_{OUT} = 0\text{V}$			40 -40 40 -70	μA μA mA
I_{OS}	Short circuit ³		-20	-70	mA
I_{CC}	V_{CC} supply current			155	mA
C_{IN} C_{OUT}	Capacitance Input Output $V_{CC} = 5.0\text{V}$ $\overline{CE} = \text{High}$ $V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$			5 8	pF

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1\text{k}\Omega$, $C_L = 30\text{pF}$, $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

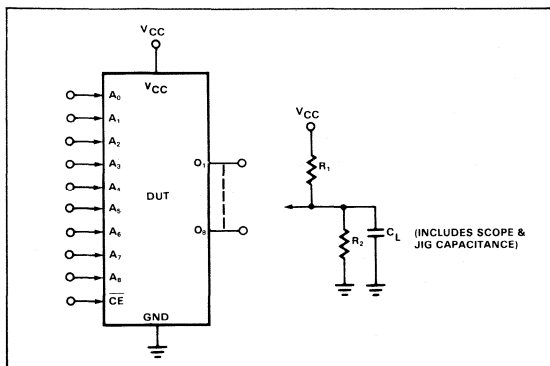
PARAMETER	TO	FROM	LIMITS			UNIT
			Min	Typ ⁵	Max	
T_{AA} ⁴ T_{CE}	Access time Output Output	Address Chip enable			45 30	ns
T_{CD}	Disable time	Output			30	ns

NOTES

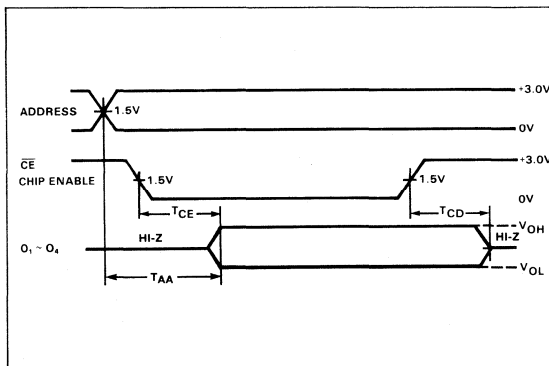
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.

4. Tested at an address cycle time of 1 μsec .
5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Section 10
PROMs,
8K-Bit

8192-BIT BIPOLAR PROM (1024 × 8)

82S180 (O.C.)/82S181 (T.S.)

DESCRIPTION

The 82S180 and 82S181 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S180 and 82S181 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of work expansion in bused organizations.

The 82S180 and 82S181 are available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S180/181 I, F or N, and for the military temperature range (-55°C to +125°C) specify S82S180/181, R, F, G, I.

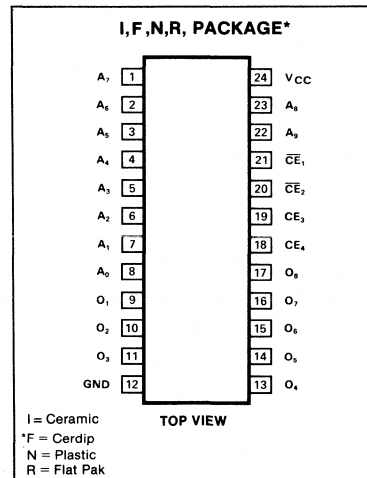
FEATURES

- **Address access time:**
N82S180/181: 70ns max
S82S180/181: 90ns max
- **Power dissipation: 85μW/bit typ**
- **Input loading:**
N82S180/181: -100μA max
S82S180/181: -150μA max
- **On-chip address decoding**
- **Output options:**
82S180: Open collector
82S181: Tri-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

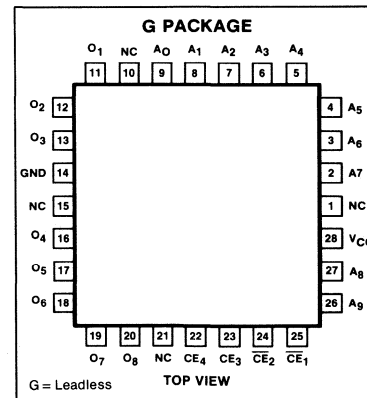
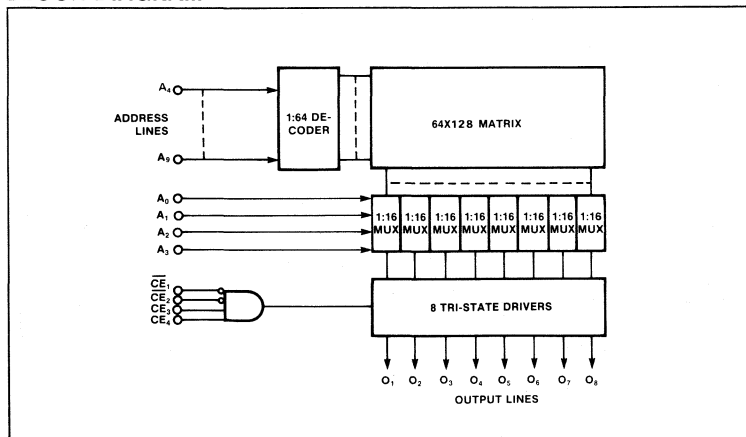
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Output voltage		Vdc
Off-state (82S181)	+5.5	
T _A Temperature range		°C
Operating	0 to +75	
N82S180/181	-55 to +125	
S82S180/181		
T _{STG} Storage	-65 to +150	

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8192-BIT BIPOLAR PROM (1024×8)**82S180 (O.C.)/82S181 (T.S.)**

DC ELECTRICAL CHARACTERISTICS N82S181: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S181: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1,2}	N82S181			S82S181			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp I _{IN} = -18mA	2.0	-0.8	-1.2	2.0		.80 -1.2	V
V _{OL} V _{OH}	Output voltage Low High C _E 1,2 = Low, C _E 3,4 = High I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	2.4		0.5	V
I _{IL} I _{IH}	Input current Low High V _{IN} = 0.45V V _{IN} = 5.5V			-100 40			-150 50	μA
I _{OLK} I _{O(OFF)} I _{OS}	Output current Leakage (82S180) Hi-Z state (82S181) Short circuit 82S181 ³ C _E 1,2 = High, C _E 3,4 = Low, V _{OUT} = 5.5V C _E 1,2 = High, C _E 3,4 = Low, V _{OUT} = 5.5V C _E 1,2 = High, C _E 3,4 = Low, V _{OUT} = 0.5V C _E 1,2 = Low, C _E 3,4 = High, V _{OUT} = 0V High Stored	-20		40 40 -40 -70	-15		60 -60 60 -85	μA μA mA
I _{CC}	V _{CC} supply current C _E 1,2 = Low, C _E 3,4 = High		125	175			185	mA
C _{IN} C _{OUT}	Capacitance Input Output C _E 1,2 = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF

N82S181: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S181: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S181			S82S181			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T _{AA} ⁴ T _{CE}	Access time Output Output	Address Chip enable		50 20	70 40			90 50	ns
T _{CD}	Disable time Output	Chip disable		20	40			50	ns

NOTES

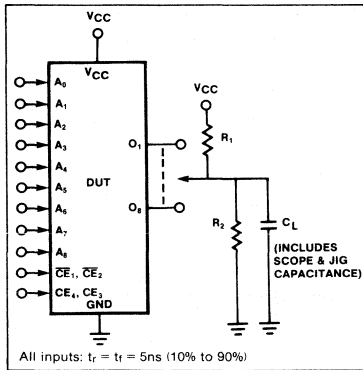
- Positive current is defined as into the terminal referenced.
- All voltages with respect to network ground.
- Duration of short circuit should not exceed 1 second.

- Tested at an address cycle time of 1μsec.
- Typical values are at V_{CC} = 5V, T_A = 25°C.

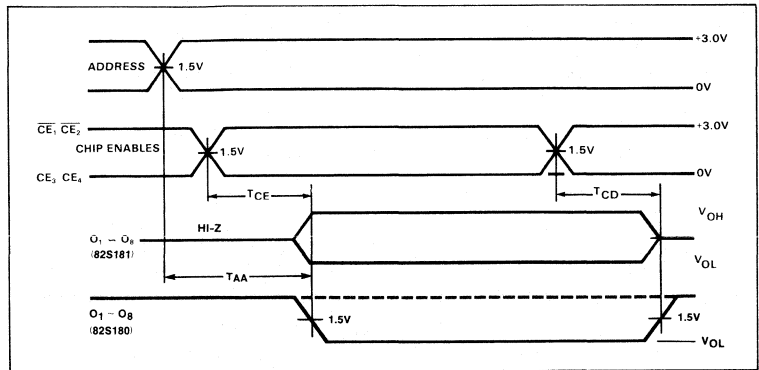
8192-BIT BIPOLAR PROM (1024x8)

82S180 (O.C.)/82S181 (T.S.)

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



8192-BIT BIPOLAR PROM (1024 × 8)

82HS181/82HS181A (T.S.)

DESCRIPTION

The 82HS181 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82HS181 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features 2 tri-state outputs for optimization of word expansion in bused organizations.

The 82HS181 is available in both the commercial and military temperature ranges. For the commercial temperature range (0° to +75°C) specify N82HS181 F or N or N82HS181A F or N, and for the military temperature range (-55°C to +125°C) specify S82HS181, R, F, G, I.

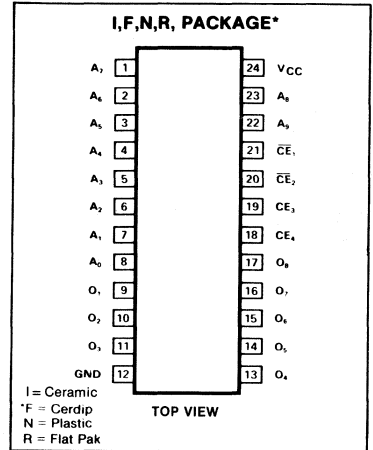
FEATURES

- Address access time:
N82HS181: 55ns max
N82HS181A: 45ns max
S82HS181: 80ns max
- Power dissipation: 85μW/bit typ
- Input loading:
N82HS181: -100μA max
S82HS181: -150μA max
- On-chip address decoding
- Output:
82HS 181: Tri-State
- No separate fusing pins
- Unprogrammed outputs are low level
- Fully TTL compatible

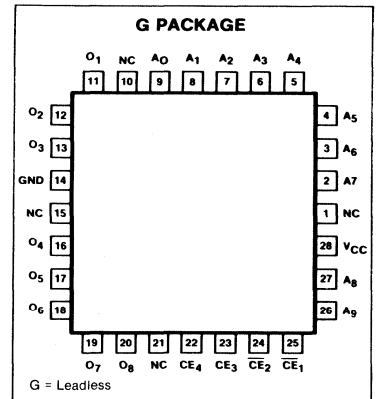
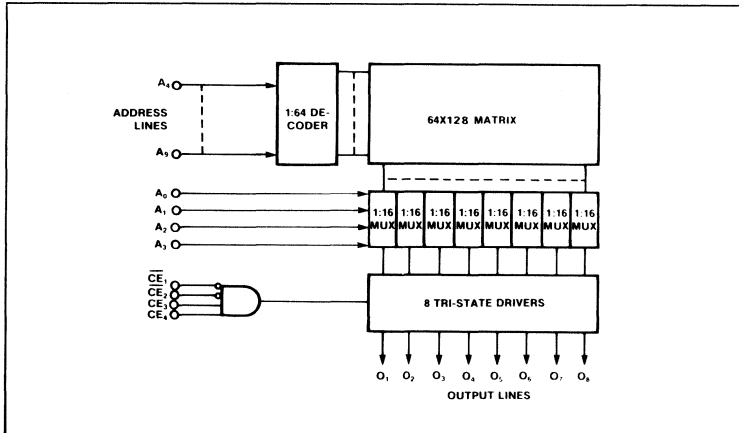
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Output voltage		Vdc
Off-state	+5.5	
T _A Temperature range		°C
Operating		
N82HS181	0 to +75	
S82HS181	-55 to +125	
T _{STG} Storage	-65 to +150	

8192-BIT BIPOLAR PROM (1024 × 8)

82HS181/82HS181A (T.S.)

DC ELECTRICAL CHARACTERISTICS N82HS181/N82HS181A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82HS181: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1,2}	N82HS181/N82HS181A			S82HS181			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp I _{IN} = -18mA	2.0	-0.8	.85 -1.2	2.0		.80 -1.2	V
V _{OL} V _{OH}	Output voltage Low High C _E 1,2 = Low, C _E 3,4 = High I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	2.4		0.5	V
I _{IL} I _{IH}	Input current Low High V _{IN} = 0.45V V _{IN} = 5.5V			-100 40			-150 50	μA
I _{OLK} I _{O(OFF)} I _{OS}	Output current Hi-Z state Short circuit ³ C _E 1,2 = High, C _E 3,4 = Low, V _{OUT} = 5.5V C _E 1,2 = High, C _E 3,4 = Low, V _{OUT} = 0.5V C _E 1,2 = Low, C _E 3,4 = High, V _{OUT} = 0V High Stored			40 -40 -70			-60 60 -85	μA μA mA
I _{CC}	V _{CC} supply current C _E 1,2 = Low, C _E 3,4 = High		125	175			185	mA
C _{IN} C _{OUT}	Capacitance Input Output C _E 1,2 = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8				5 8	pF

AC ELECTRICAL CHARACTERISTICS R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82HS181/N82HS181A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82HS181: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82HS181			N82HS181A			S82HS181			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	Min	Typ	Max	
T _{AA} ⁴ T _{CE}	Access time	Output	Address Chip enable	45 20	55 35			45 30			80 45	ns
T _{CD}	Disable time	Output	Chip disable	20	35			30			45	ns

NOTES

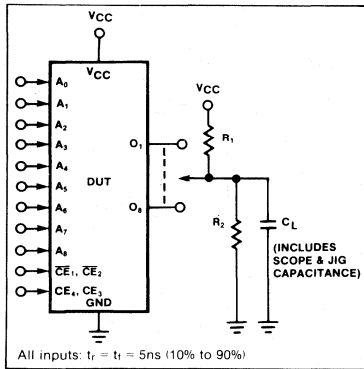
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

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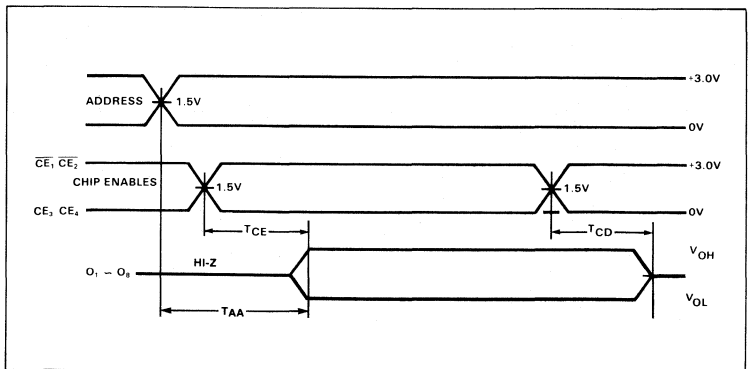
8192-BIT BIPOLAR PROM (1024 × 8)

82HS181/82HS181A (T.S.)

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



8192-BIT BIPOLAR PROM (1024×8)

82LS181 (T.S.)

DESCRIPTION

The 82LS181 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82LS181 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 4 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82LS181 is available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82LS181, F or N, and for the military temperature range (-55°C to +125°C) specify S82LS181, F,G, or R.

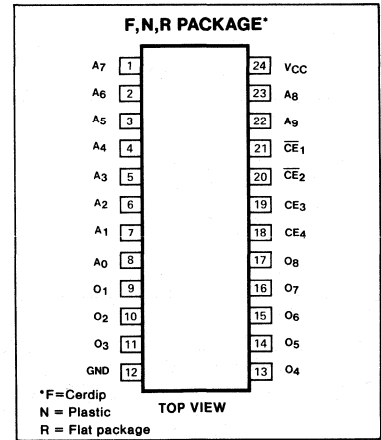
FEATURES

- **Address access time:**
N82LS181: 120ns max
S82LS181: 180ns max
- **Power dissipation: 37µW/bit typ**
- **Input loading:**
N82LS181: -100µA max
S82LS181: -150µA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

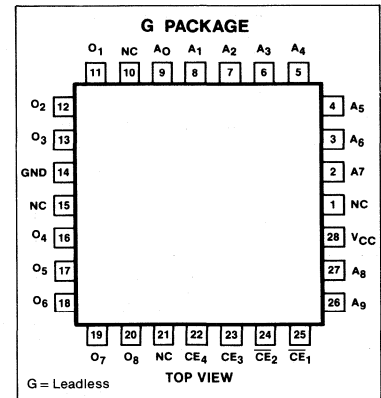
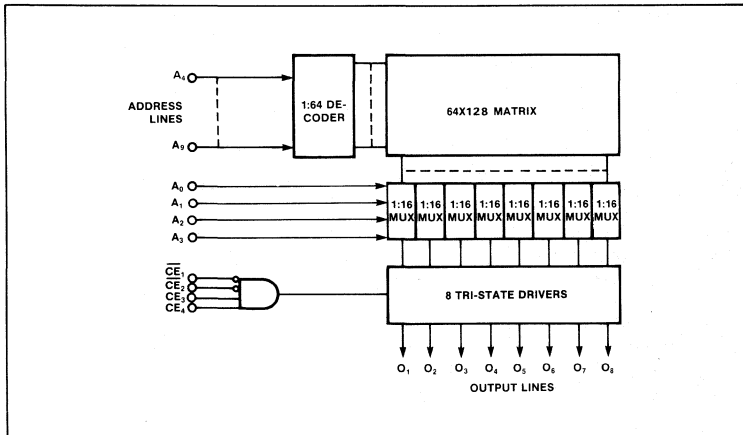
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
V _O	Output voltage	+5.5	Vdc
T _A	Operating Temperature range		°C
	N82LS181	0 to +75	
	S82LS181	-55 to +125	
T _{STG}	Storage	-65 to +150	

8192-BIT BIPOLAR PROM (1024 × 8)

82LS181 (T.S.)

DC ELECTRICAL CHARACTERISTICS N82LS181: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82LS181: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

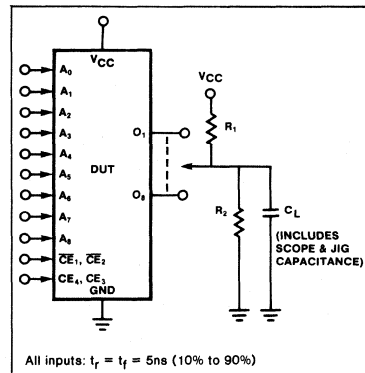
PARAMETER	TEST CONDITIONS ^{1,2}	N82LS181			S82LS181			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V_{IL} V_{IH} V_{IC}	Input voltage Low High Clamp $I_{IN} = -18\text{mA}$	2.0	-0.8	-1.2	2.0		-1.2	V
V_{OL} V_{OH}	Output voltage Low High $\overline{CE}_{1,2} = \text{Low}, CE_{3,4} = \text{High}$ $I_{OUT} = 4.8\text{mA}$ $I_{OUT} = -1\text{mA}$	2.4		0.45	2.4		0.5	V
I_{iL} I_{iH}	Input current Low High $V_{IN} = 0.45\text{V}$ $V_{IN} = 5.5\text{V}$			-100 40			-150 50	μA
$I_{O(OFF)}$ I_{OS}	Output current Hi-Z state Short circuit ³ $\overline{CE}_{1,2} = \text{High}, CE_{3,4} = \text{Low}$ $V_{OUT} = 5.5\text{V}$ $\overline{CE}_{1,2} = \text{High}, CE_{3,4} = \text{Low}$ $V_{OUT} = 0.5\text{V}$ $\overline{CE}_{1,2} = \text{Low}, CE_{3,4} = \text{High}$, high stored $V_{OUT} = 0\text{V}$	-10		-40 40 -70	-10		-60 60 -85	μA μA mA
I_{CC}	V_{CC} supply current		60	80			85	mA
C_{IN} C_{OUT}	Capacitance Input Output $\overline{CE}_{1,2} = \text{High}, CE_{3,4} = \text{Low}, V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$		5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS $R_1 = 1\text{k}\Omega$, $R_2 = 2\text{k}\Omega$, $C_L = 30\text{pF}$
 N82LS181: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82LS181: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

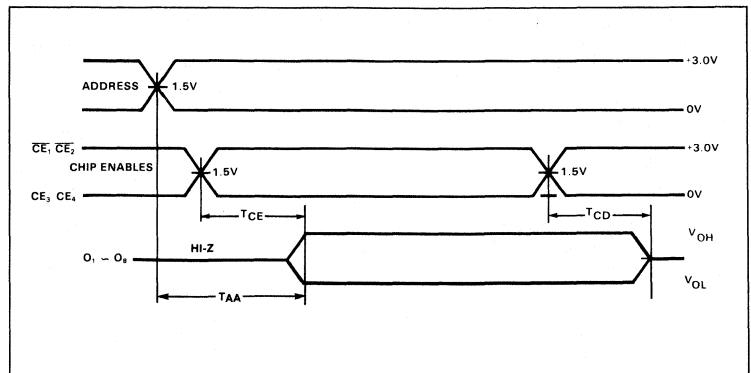
PARAMETER	TO	FROM	N82LS181			S82LS181			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T_{AA} ⁴ T_{CE}	Output	Address		100	120			180	ns
	Output	Chip enable		35	50			70	
T_{CD}	Output	Chip disable		35	50			70	ns

- NOTES
 1. Positive current is defined as into the terminal referenced.
 2. All voltages with respect to network ground.
 3. Duration of short circuit should not exceed 1 second.
 4. Tested at an address cycle time of $1\mu\text{sec}$.
 5. Typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



8192-BIT BIPOLAR PROM (1024 × 8)

82S183 (T.S.)

DESCRIPTION

The 82S183 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82S183 is supplied with all outputs at logic low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

In the Transparent Read mode, stored data is addressed by applying a binary code to the address inputs while holding Strobe high. In this mode the output drivers are controlled solely by \overline{CE}_1 , \overline{CE}_2 , and \overline{CE}_3 lines.

A D-type latch is used to enable the tri-state output drivers. In the Latched Read mode, outputs are held in their previous state (high, low, or high Z) as long as Strobe is low, regardless of the state of address or chip enable. A positive Strobe transition causes data from the applied address to reach the outputs if the chip is enabled, and causes outputs to go to the high Z state if the chip is disabled.

A negative Strobe transition causes outputs to be locked into their last Read Data condition if the chip was enabled, or causes outputs to be locked into the high Z condition if the chip was disabled.

The 82S183 is available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S183, for F or N, and for the military temperature range (-55°C to 125°C) specify S82S183, F, G or R.

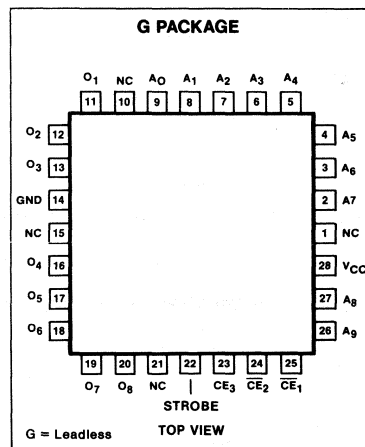
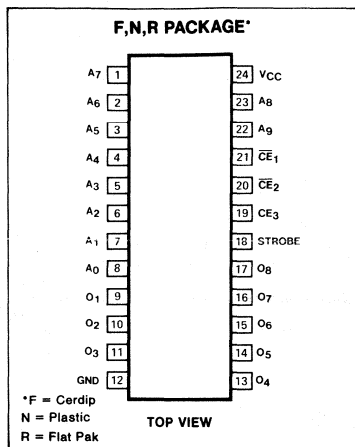
FEATURES

- **Address access time:**
 N82S183: 60ns max
 S82S183: 90ns max
- **Power dissipation:** 85μW/bit typ
- **Input loading:**
 N82S183: -100μA max
 S82S183: -150μA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

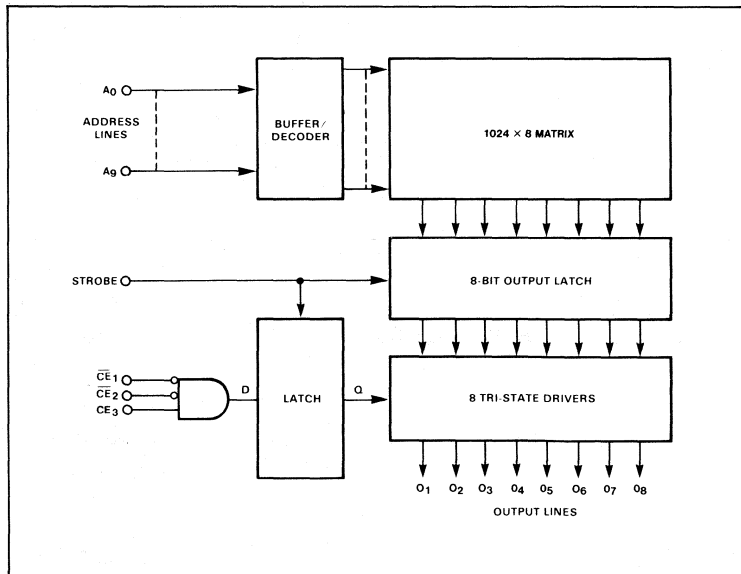
APPLICATIONS

- Prototyping / volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



10

8192-BIT BIPOLAR PROM (1024 × 8)

82S183 (T.S.)

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
T _A	Temperature range		°C
	Operating	0 to +75	
	N82S183	-55 to +125	
	S82S183		
T _{STG}	Storage	-65 to +150	

DC ELECTRICAL CHARACTERISTICS N82S183: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S183: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ⁴	N82S183			S82S183			UNIT	
		Min	Typ ⁶	Max	Min	Typ	Max		
V _{IL}	Input voltage Low	2.0	-0.8	.85	2.0		.8	V	
V _{IH}	Input voltage High								
V _{IC}	Clamp								
		I _{IN} = -18mA							
V _{OL}	Output voltage Low			0.45			0.5	V	
V _{OH}	Output voltage High								
		CE _{1,2} = Low, CE ₃ = Strobe = High I _{OUT} = 9.6mA I _{OUT} = -2.0mA							
I _{IL}	Input current ⁴ Low	25		-100			-150	μA	
I _{IH}	Input current ⁴ High								
		V _{IN} = 0.45V V _{IN} = 5.5V							
I _{O(OFF)}	Output current ⁴ Hi-Z state	-20		40			100	μA	
I _{OS}	Short circuit ¹								
		CE = High or CE = Low, V _{OUT} = 5.5V CE = High or CE = Low, V _{OUT} = 0.5V CE = Low, CE = High, V _{OUT} = 0V, High stored							
I _{CC}	V _{CC} supply current		130	175			185	mA	
C _{IN}	Capacitance Input	CE _{1,2} = High or CE ₃ = Low, V _{CC} = 5.0 V _{IN} = 2.0V							pF
C _{OUT}	Capacitance Output	V _{OUT} = 2.0V							
			5				5		
			8				8		

AC ELECTRICAL CHARACTERISTICS R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82S183: 0° ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S183: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	TEST CONDITIONS	N82S183			S82S183			UNIT
				Min	Typ ⁶	Max	Min	Typ	Max	
T _{AA}	Output	Address	Latched or transparent read		45	60			90	ns
T _{CE}										
T _{CD}	Output	Chip disable	Latched or transparent read		25	40			50	ns
T _{CDS}	Output	Chip enable	Latched read only	40			50			ns
T _{CDH}										
T _{ADH}	Output	Address		0			5			
T _{SW}			Latched read only	30	15		40			ns
T _{SL}			Latched read only	60	35		90			ns
T _{DL}			Latched read only			30			35	ns

NOTES on following page.

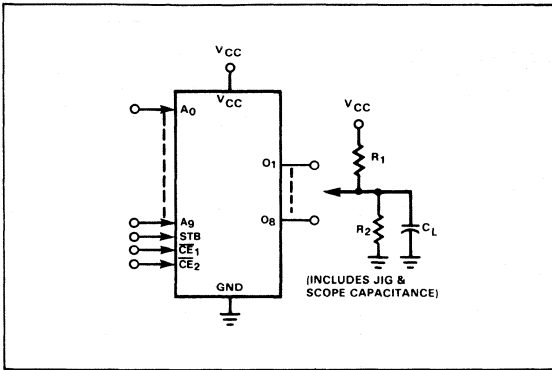
8192-BIT BIPOLAR PROM (1024×8)

82S183 (T.S.)

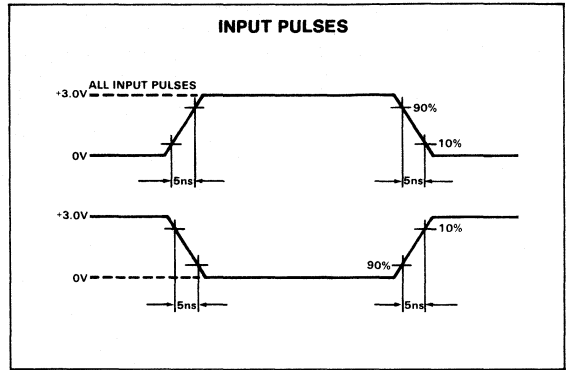
NOTES

1. No more than one output should be grounded at the same time and strobe should be disabled. Strobe is in high state.
2. If the strobe is high, the device functions in a manner identical to conventional bipolar ROMs. The timing diagram shows valid data will appear T_{AA} nanoseconds after the address has changed the T_{CE} nanoseconds after the output circuit is enabled. T_{CD} is the time required to disable the output and switch it to an off or high impedance state after it has been enabled.
3. In Latched Read Mode data from any selected address will be held on the output when strobe is lowered. Only when strobe is raised will new location data be transferred and chip enable conditions be stored. The new data will appear on the outputs if the chip enable conditions enable the outputs.
4. Positive current is defined as into the terminal referenced.
5. Areas shown by crosshatch are latched data from previous address.
6. Typical values are at $V_{CC} = 5V$, $T_A = 25^\circ C$

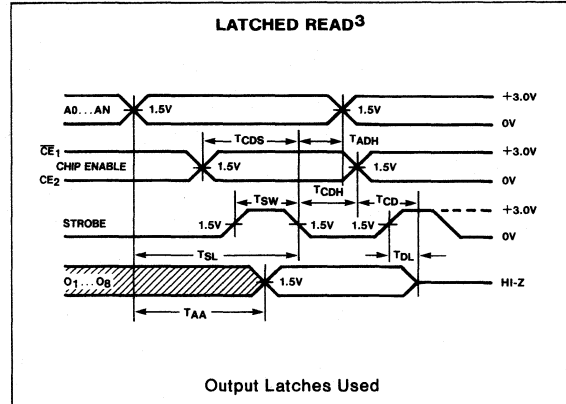
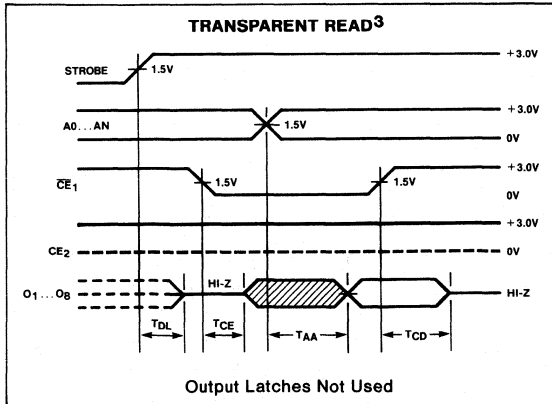
TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAMS



10

8192-BIT BIPOLAR PROM (2048 × 4)

82S185 (T.S.)

DESCRIPTION

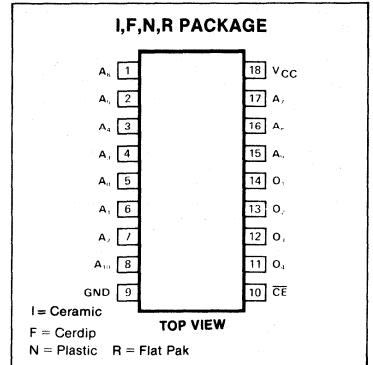
The 82S185 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82S185 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 1 chip enable input for memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S185 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S185, I, F, N, and for the military temperature range (-55°C to +125°C) specify S82S185, I, F, or R.

FEATURES

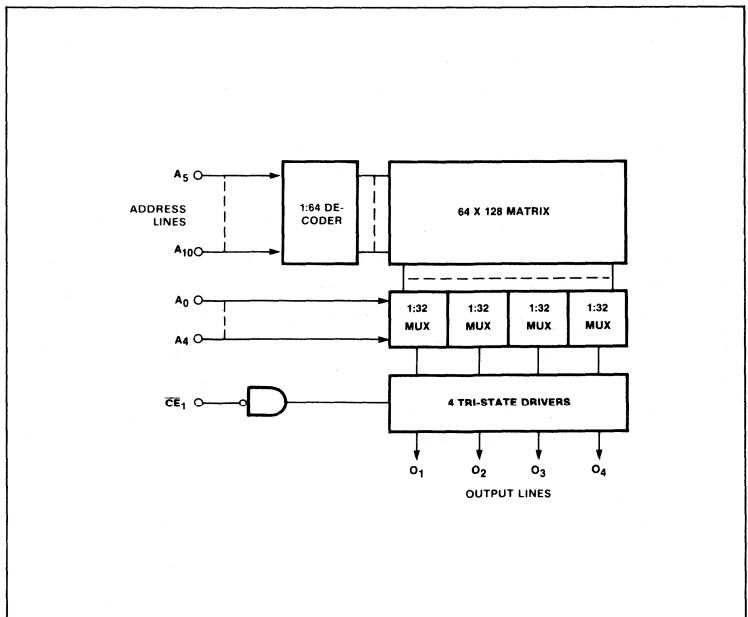
- **Low power dissipation: 50μW/bit typ**
- **Address access time:**
N82S185: 100ns max
S82S185: 115ns max
- **Input loading:**
N82S185: -100μA max
S82S185: -150μA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Output voltage	+5.5	Vdc
V _O Off-state	+5.5	Vdc
T _A Temperature range		°C
T _A Operating	N82S185	0 to +75
	S82S185	-55 to +125
T _{STG} Storage	-65 to +150	

BLOCK DIAGRAM



8192-BIT BIPOLAR PROM (2048 × 4)

82S185 (T.S.)

DC ELECTRICAL CHARACTERISTICS N82S185: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S185: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1, 2}	N82S185			S82S185			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage ¹ Low High Clamp			.85			.80	V
		2.0	-0.8	-1.2	2.0		-1.2	
	I _{IN} = -18mA							
V _{OL} V _{OH}	Output voltage ¹ Low High			0.45			0.5	V
		2.4		2.4				
	\overline{CE} = Low I _{OUT} = 16mA I _{OUT} = -2mA							
I _{IL} I _{IH}	Input current Low High			-100 40			-150 50	μA
	V _{IN} = 0.45V V _{IN} = 5.5V							
I _O (OFF) I _{OS}	Output current Hi-Z state Short circuit ³			-40 40 -70			-60 60 -85	μA mA
	\overline{CE} = High, V _{OUT} = 0.5V \overline{CE} = High, V _{OUT} = 5.5V \overline{CE} = Low, V _{OUT} = 0V High Stored	-20		-15				
I _{CC}	V _{CC} supply current		90	120			130	mA
C _{IN} C _{OUT}	Capacitance Input Output		5 8			5 8		pF
	\overline{CE} = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V							

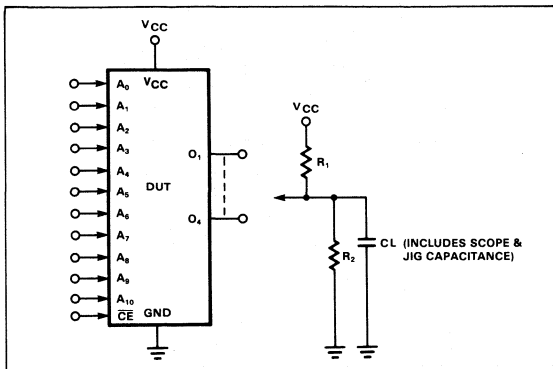
AC ELECTRICAL CHARACTERISTICS R₁ = 270Ω, R₂ = 600Ω, C_L = 30pF
 N82S185: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S185: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S185			S82S185			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T _{AA} ⁴ T _{CE}	Access time Output Output	Address Chip enable		70 30	100 40			115 50	ns
T _{CD}	Disable time Output	Chip disable		30	40			50	ns

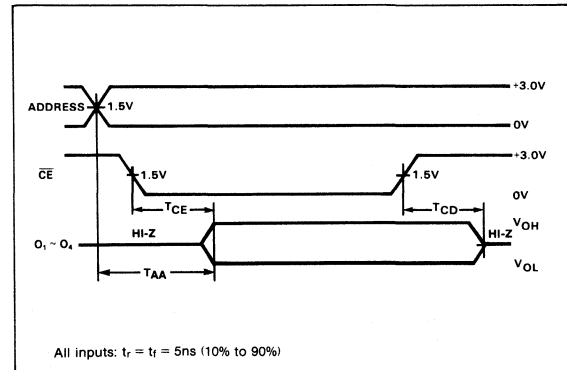
NOTES

- All voltage values are with respect to network ground terminal.
- Positive current is defined as into the terminal referenced.
- Duration of the short circuit should not exceed 1 second.
- Tested at an address cycle time of 1μsec.
- All typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



8192-BIT BIPOLAR PROM (2048 × 4)

82HS185/82HS185A (T.S.)

DESCRIPTION

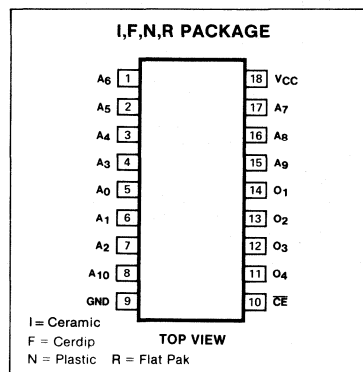
The 82HS185 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82HS185 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 1 chip enable input for memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82HS185 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82HS185, I, F, N, or N82HS185A, I, F, or N, and for the military temperature range (-55°C to +125°C) specify S82HS185, I, F, or R.

FEATURES

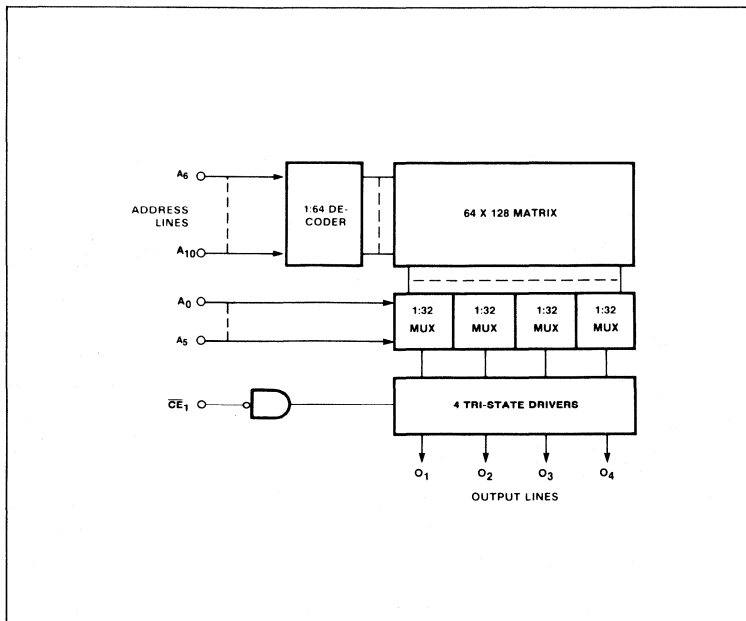
- **Low power dissipation:** 70 μ W/bit typ
- **Address access time:**
 N82HS185: 50ns max
 N82HS185A: 45ns max
 S82HS185: 80ns max
- **Input loading:**
 N82HS185: -100 μ A max
 S82HS185: -150 μ A max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Output voltage	+5.5	Vdc
V _O Off-state	+5.5	Vdc
T _A Temperature range		°C
Operating	N82HS185	0 to +75
	S82HS185	-55 to +125
T _{STG} Storage	-65 to +150	

BLOCK DIAGRAM



8192-BIT BIPOLAR PROM (2048 × 4)

82HS185/82HS185A (T.S.)

DC ELECTRICAL CHARACTERISTICS N82HS185, N82HS185A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82HS185: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1,2}	N82HS185			S82HS185			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage ¹ Low High Clamp			.85			.80	V
		2.0	-0.8	-1.2	2.0		-1.2	
	I _{IN} = -18mA							
V _{OL} V _{OH}	Output voltage ¹ Low High			0.45			0.5	V
	\overline{CE} = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4			2.4			
I _{IL} I _{IH}	Input current Low High			-100 40			-150 50	μA
	V _{IN} = 0.45V V _{IN} = 5.5V							
I _O (OFF) I _{OS}	Output current Hi-Z state Short circuit ³			-40 40 -70			-60 60 -85	μA mA
	\overline{CE} = High, V _{OUT} = 0.5V \overline{CE} = High, V _{OUT} = 5.5V \overline{CE} = Low, V _{OUT} = 0V High Stored							
I _{CC}	V _{CC} supply current		110	155			160	mA
C _{IN} C _{OUT}	Capacitance Input Output			5 8			5 8	pF
	\overline{CE} = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V							

AC ELECTRICAL CHARACTERISTICS R₁ = 270Ω, R₂ = 600Ω, C_L = 30pF
 N82HS185, N82HS185A: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82HS185: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

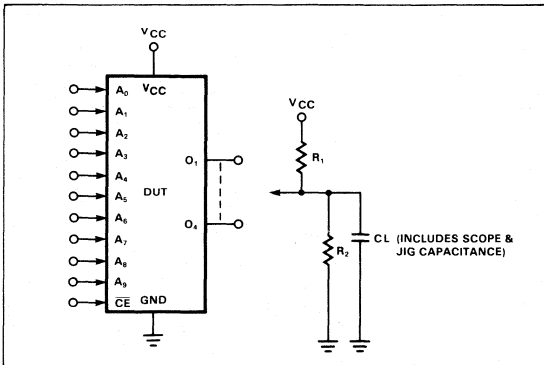
PARAMETER	TO	FROM	N82HS185			N82HS185A			S82HS185			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	Min	Typ	Max	
T _{AA} ⁴ T _{CE}	Access time Output Output	Address Chip enable		40 20	50 30			45 25			80 40	ns
TCD	Disable time Output	Chip disable		20	30			25			40	ns

NOTES

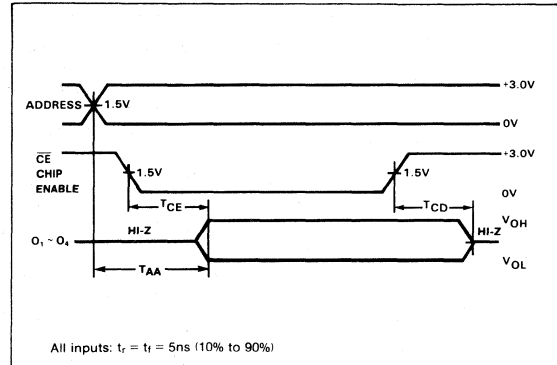
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C

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TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



8192-BIT BIPOLAR PROM (1024×8)

82S2708 (T.S.)

DESCRIPTION

The 82S2708 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S2708 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 1 chip enable input for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S2708 is available only in the military temperature range. For the military temperature range (-55°C to +125°C) specify S82S2708, F or R.

Pins 21, 19 and 18 have no internal connections, therefore -5V, +12 and programming voltages used by MOS devices will have no effect on this bipolar device.

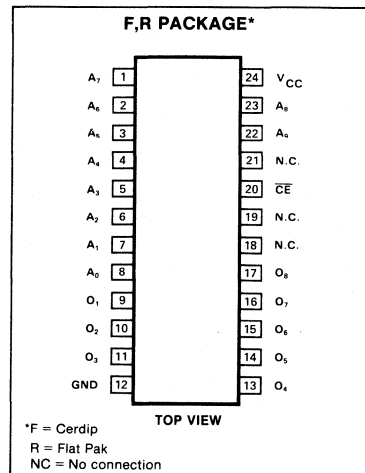
FEATURES

- Address access time:
 S82S2708: 90ns max
- Power dissipation: **85μW/bit typ**
- Input loading:
 S82S2708: -150μA max
- Chip enable input
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are low level
- Pin for pin replacement for 2708 EROM
- Fully TTL compatible

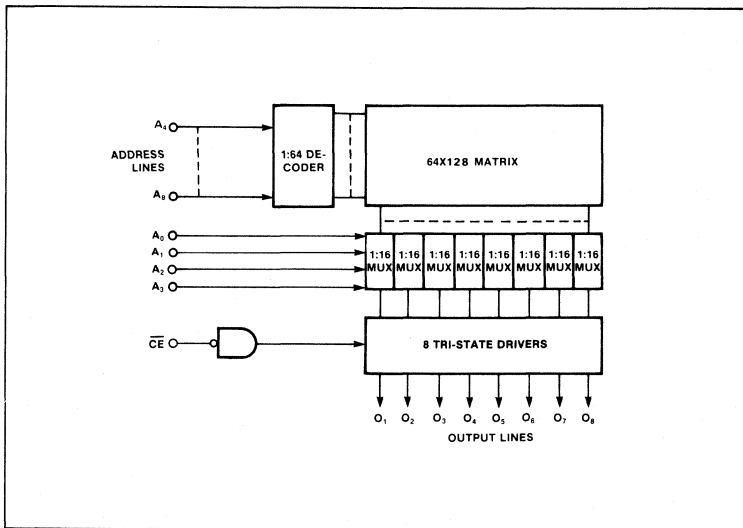
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
Output voltage		Vdc
V _{OH} High	+5.5	
V _O Off-state	+5.5	
Temperature range		°C
T _A Operating		
S82S2708	-55 to +125	
T _{STG} Storage	-65 to +150	

8192-BIT BIPOLAR PROM (1024 × 8)

82S2708 (T.S.)

DC ELECTRICAL CHARACTERISTICS S82S2708: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1, 2}	S82S2708			UNIT
		Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp I _{IN} = -18mA	2.0		.80 -1.2	V
V _{OL} V _{OH}	Output voltage Low High C _Ē = Low I _{OUT} = 9.6mA I _{OUT} = -2.0mA	2.4		0.5	V
I _{IL} I _{IH}	Input current Low High V _{IN} = 0.45V V _{IN} = 5.5V			-150 50	μA
I _{O(OFF)} I _{OS}	Output current Hi-Z state Short circuit ³ C _Ē = High, V _{OUT} = 0.5V C _Ē = High, V _{OUT} = 5.5V C _Ē = Low, V _{OUT} = 0V, Stored High	-15		-60 60 -85	μA mA
I _{CC}	V _{CC} supply current			185	mA
C _{IN} C _{OUT}	Capacitance Input Output C _Ē = High V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8		pF

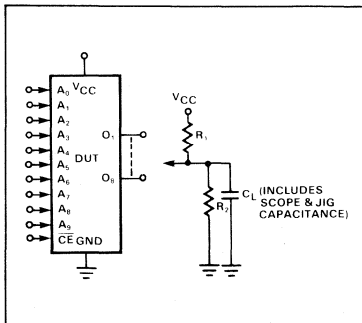
AC ELECTRICAL CHARACTERISTICS R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF S82S2708: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	S82S2708			UNIT
			Min	Typ ⁵	Max	
T _{AA} ⁴ T _{CE}	Access time Output Output	Address Chip enable		70 40	90 50	ns
T _{CD}	Disable time Output	Chip disable		40	50	ns

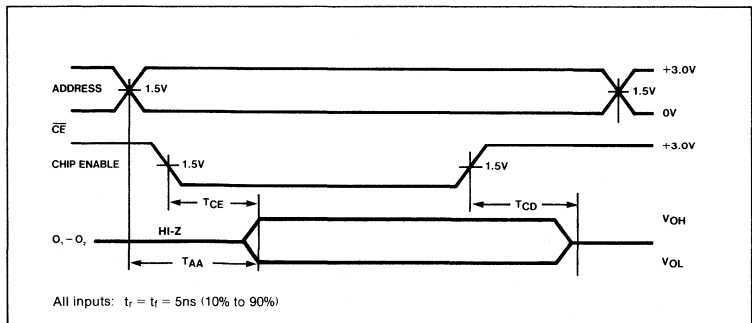
NOTES

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Section 11
PROMs,
16K-Bit

16,384-BIT BIPOLAR PROM (2048 × 8)

82S191 (T.S.)

DESCRIPTION

The 82S191 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S191 is supplied with all outputs at a logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S191 device is available in the commercial and military ranges. For the commercial temperature range (0°C to +75°C) specify N82S191, I or N and for the military temperature range (-55°C to +125°C) specify S82S191, R or G.

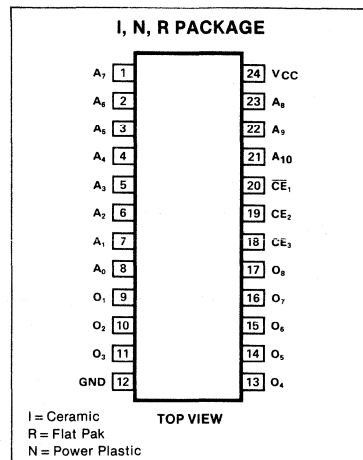
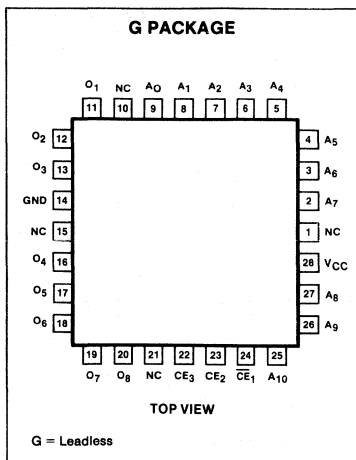
FEATURES

- **Address access time:**
 N82S191: 80ns max
 S82S191: 100ns max
- **Power dissipation:** 40µW/bit typ
- **Input loading:**
 N82S191: -100µA max
 S82S191: -150µA max
- **3 chip enable inputs**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

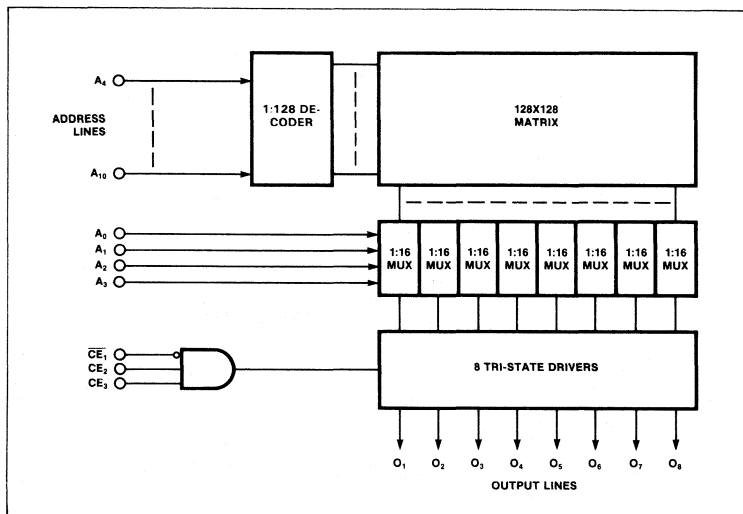
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Output voltage		Vdc
V _O Off-state	+5.5	
T _A Temperature range		°C
Operating	0 to +75	
N82S191		
S82S191	-55 to +125	
T _{STG} Storage	-65 to +150	

16,384-BIT BIPOLAR PROM (2048 × 8)

82S191 (T.S.)

DC ELECTRICAL CHARACTERISTICS N82S191: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S191: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1, 2}	N82S191			S82S191			UNIT	
		Min	Typ ⁵	Max	Min	Typ	Max		
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp			.85 -1.2			.80 -1.2	V	
V _{OL} V _{OH}	Output voltage Low High	$\overline{CE}_1 = \text{Low}, CE_{2,3} = \text{High}$ I _{OUT} = 9.6mA I _{OUT} = -2mA					0.45 2.4	0.5	V
I _{IL} I _{IH}	Input current Low High	V _{IN} = 0.45V V _{IN} = 5.5V					-100 40	-150 50	μA
I _{O(OFF)} I _{OS}	Output current Hi-Z state Short circuit ³	$\overline{CE}_1 = \text{High}, CE_{2,3} = \text{Low},$ V _{OUT} = 0.5 $\overline{CE}_1 = \text{High}, CE_{2,3} = \text{Low},$ V _{OUT} = 5.5 $\overline{CE}_1 = \text{Low}, CE_{2,3} = \text{High},$ V _{OUT} = 0V					-40 40 -70	-60 60 -85	μA mA
I _{CC}	V _{CC} supply current		130	175			185	mA	
C _{IN} C _{OUT}	Capacitance Input Output	$\overline{CE}_1 = \text{High}, CE_{2,3} = \text{Low},$ V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V					5 8	5 8	pF

AC ELECTRICAL CHARACTERISTICS R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82S191: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S191: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S191			S82S191			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T _{AA} ⁴ T _{CE}	Access time Output Output	Address Chip enable		50 20	80 40			100 50	ns
T _{CD}	Disable time Output	Chip disable		20	40			50	ns

NOTES

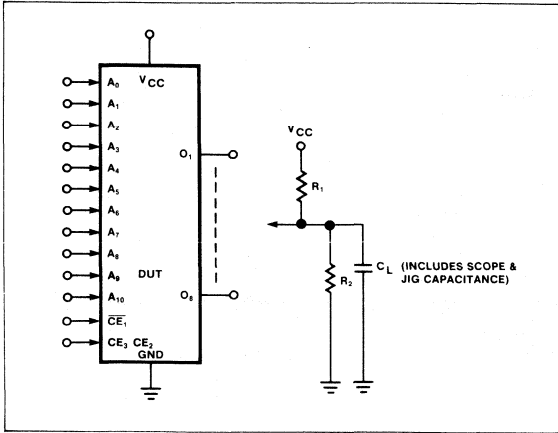
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.

4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

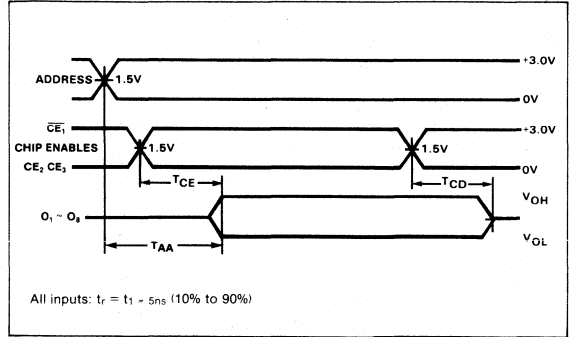
16,384-BIT BIPOLAR PROM (2048 × 8)

82S191 (T.S.)

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



16,384-BIT BIPOLAR PROM (2048 × 8)

82HS191 (T.S.)

DESCRIPTION

The 82HS191 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82HS191 is supplied with all outputs at a logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 3 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82HS191 device is available in the commercial and military ranges. For the commercial temperature range (0°C to +75°C) specify N82HS191, I or N, and for the military temperature range (-55°C to +125°C) specify S82HS191, I, R or G.

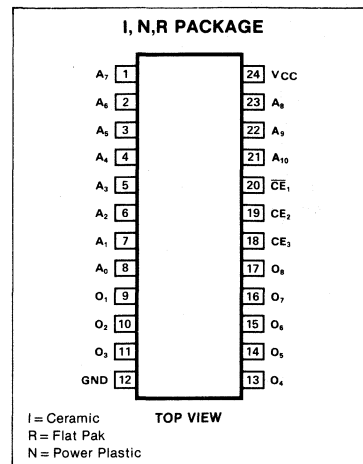
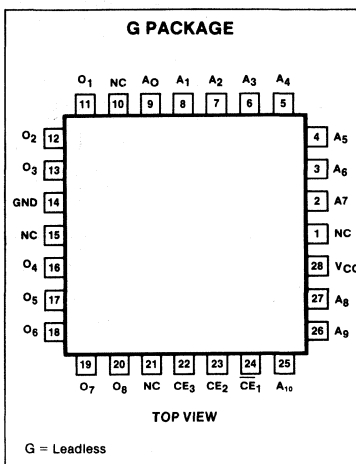
FEATURES

- Address access time:
N82HS191: 60ns max
S82HS191: 80ns max
- Power dissipation: 20μW/bit typ
- Input loading:
N82HS191: -100μA max
S82HS191: -150μA max
- 3 chip enable inputs
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are low level
- Fully TTL compatible

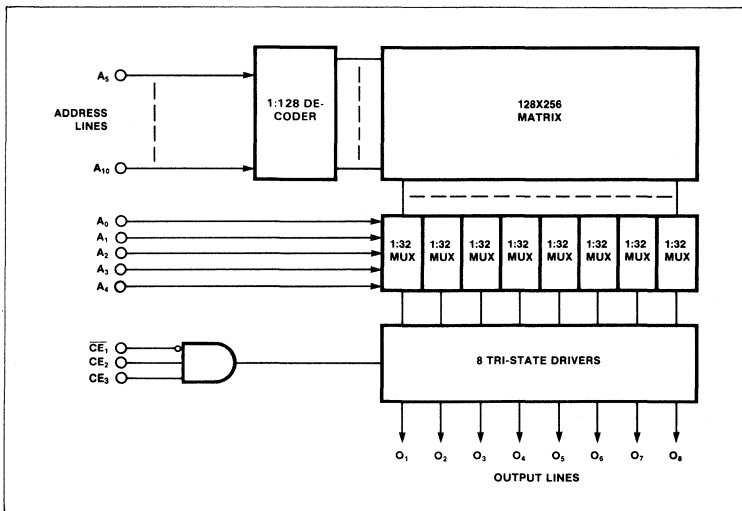
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT	
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
V _O	Output voltage		Vdc
	Off-state	+5.5	
T _A	Temperature range		°C
	Operating	0 to +75	
	N82HS191	-55 to +125	
	S82HS191		
T _{STG}	Storage	-65 to +150	

16,384-BIT BIPOLAR PROM (2048 × 8)

82HS191 (T.S.)

DC ELECTRICAL CHARACTERISTICS N82HS191: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82HS191: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1,2}	N82HS191			S82HS191			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp I _{IN} = -18mA	2.0	-0.8	.85 -1.2	2.0		.80 -1.2	V
V _{OL} V _{OH}	Output voltage Low High C _{E1} = Low, C _{E2,3} = High I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	2.4		0.5	V
I _{IL} I _{IH}	Input current Low High V _{IN} = 0.45V V _{IN} = 5.5V			-100 40			-150 50	μA
I _{O(OFF)} I _{OS}	Output current Hi-Z state Short circuit ³ C _{E1} = High, C _{E2,3} = Low, V _{OUT} = 0.5 C _{E1} = High, C _{E2,3} = Low, V _{OUT} = 5.5 C _{E1} = Low, C _{E2,3} = High, V _{OUT} = 0V	-20		-40 40 -70			-60 60 -85	μA mA
I _{CC}	V _{CC} supply current		130	175			185	mA
C _{IN} C _{OUT}	Capacitance Input Output C _{E1} = High, C _{E2,3} = Low, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8				5 8	pF

AC ELECTRICAL CHARACTERISTICS R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82HS191: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82HS191: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82HS191			S82HS191			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T _{AA} ⁴ T _{CE}	Access time Output Output	Address Chip enable		50 20	60 35			80 45	ns
T _{CD}	Disable time Output	Chip disable		20	35			45	ns

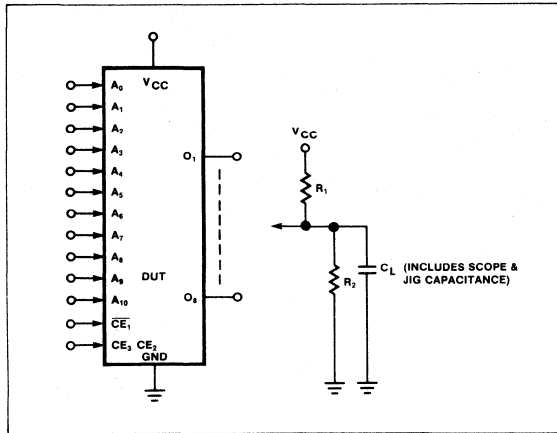
- NOTES:
 1. Positive current is defined as into the terminal referenced.
 2. All voltages with respect to network ground.
 3. Duration of short circuit should not exceed 1 second.
 4. Tested at an address cycle time of 1μsec.
 5. Typical values are at V_{CC} = 5V, T_A = 25°C.



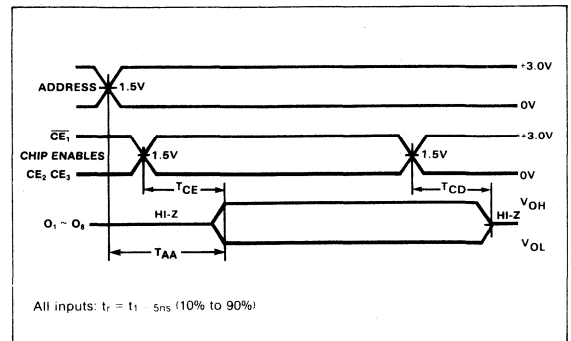
16,384-BIT BIPOLAR PROM (2048 × 8)

82HS191 (T.S.)

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



16,384-BIT BIPOLAR PROM (4096 × 4)

82S195 (T.S.)

Advance Information

DESCRIPTION

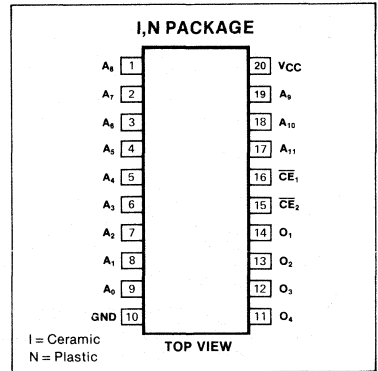
The 82S195 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The standard 82S195 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 2 chip enable inputs for memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S195 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S195, I or N, and for the military temperature range (-55°C to +125°C) specify S82S195, I.

FEATURES

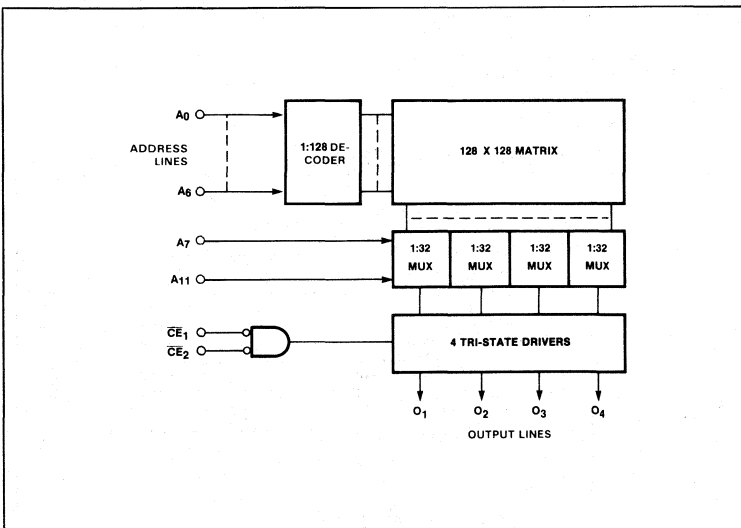
- Low power dissipation: 35µW/bit typ
- Address access time:
N82S195: 50ns max
S82S195: 70ns max
- Input loading:
N82S195: -100µA max
S82S195: -150µA max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are low level
- Fully TTL compatible



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Output voltage		Vdc
V _O Off-state	+5.5	
Temperature range		°C
T _A Operating	0 to +75	
N82S195	-55 to +125	
S82S195	-65 to +150	
T _{STG} Storage		

BLOCK DIAGRAM



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16,384-BIT BIPOLAR PROM (4096 × 4)

82S195 (T.S.)

Advance Information

DC ELECTRICAL CHARACTERISTICS N82S195: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S195: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1,2}	N82S195			S82S195			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
Input voltage ¹ V _{IL} Low V _{IH} High V _{IC} Clamp	I _{IN} = -18mA			.85			.80	V
		2.0	-0.8	-1.2	2.0		-1.2	
Output voltage ¹ V _{OL} Low V _{OH} High	\overline{CE}_1 & \overline{CE}_2 = Low I _{OUT} = 16mA I _{OUT} = -2mA			0.45			0.5	V
		2.4			2.4			
Input current I _{IL} Low I _{IH} High	V _{IN} = 0.45V V _{IN} = 5.5V			-100			-150	μA
				40			50	
Output current I _O (OFF) Hi-Z state	\overline{CE}_1 & \overline{CE}_2 = High, V _{OUT} = 0.5V \overline{CE}_1 & \overline{CE}_2 = High, V _{OUT} = 5.5V			-40			-60	μA
				40			60	
I _{OS} Short circuit ³	\overline{CE}_1 & \overline{CE}_2 = Low, V _{OUT} = 0V High Stored	-20		-70	-15		-85	mA
I _{CC} V _{CC} supply current			110	155			165	mA
Capacitance C _{IN} Input C _{OUT} Output	\overline{CE}_1 & \overline{CE}_2 = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5			5		pF
			8			8		

AC ELECTRICAL CHARACTERISTICS R₁ = 270Ω, R₂ = 600Ω, C_L = 30pF

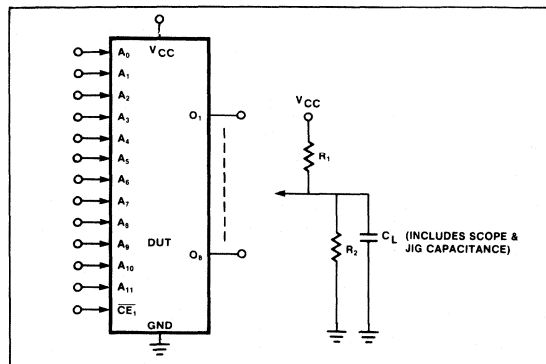
N82S195: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S195: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82S195			S82S195			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
Access time T _{AA} ⁴ T _{CE}	Output Output	Address Chip enable		40	50			70	ns
				25	30			40	
Disable time T _{CD}	Output	Chip disable		25	30			40	ns

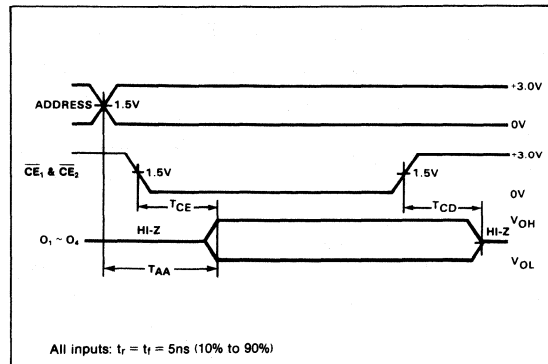
NOTES

- All voltage values are with respect to network ground terminal.
- Positive current is defined as into the terminal referenced.
- Duration of the short circuit should not exceed 1 second.
- Tested at an address cycle time of 1μsec.
- All typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



16,384-BIT BIPOLAR PROM (4096 × 4)

82HS195 (T.S.)

Advance Information

DESCRIPTION

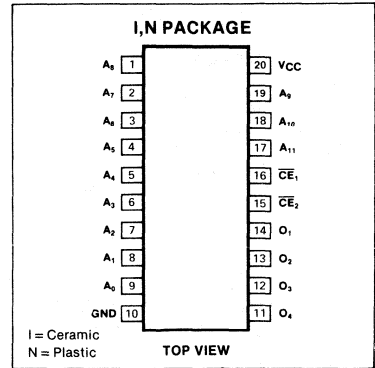
The 82HS195 is field programmable, which means that custom patterns are immediately available by following the focusing procedure given in this data manual. The standard 82HS195 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a programmable matrix.

This device includes on-chip decoding and 2 chip enable inputs for memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82HS195 device is available in the commercial and military temperature ranges. For the commercial temperature range (0°C to + 75°C) specify 82HS195, I or N, and for the military temperature range (- 55°C to + 125°C) specify S82HS195, I.

FEATURES

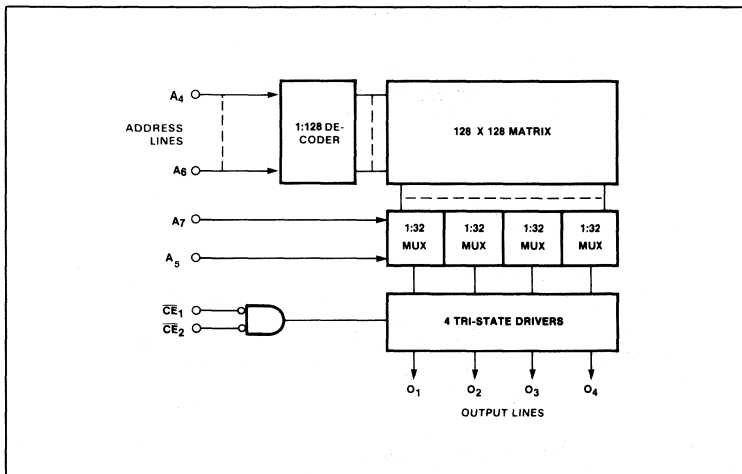
- **Low power dissipation:** 35µW/bit typ
- **Address access time:**
 N82HS195: 35ns max
 S82HS195: 50ns max
- **Input loading:**
 N82HS195: - 100µA max
 S82HS195: - 150µA max
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V _{CC}	Supply voltage	+7	Vdc
V _{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V _O	Off-state	+5.5	
	Temperature range		°C
T _A	Operating		
	N82HS195	0 to +75	
	S82HS195	-55 to +125	
T _{STG}	Storage	-65 to +150	

BLOCK DIAGRAM



16,384-BIT BIPOLAR PROM (4096 × 4)

82HS195 (T.S.)

Advance Information

DC ELECTRICAL CHARACTERISTICS N82HS195: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82HS195: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TEST CONDITIONS ^{1,2}	N82HS195			S82HS195			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V _{IL} Input voltage ¹ Low	I _{IN} = -18mA	2.0		.85	2.0		.80	V
V _{IH} High								
V _{IC} Clamp								
V _{OL} Output voltage ¹ Low	CE ₁ & CE ₂ = Low I _{OUT} = 16mA I _{OUT} = -2mA	2.4		0.45	2.4		0.5	V
V _{OH} High								
I _{IL} Input current Low	V _{IN} = 0.45V V _{IN} = 5.5V			-100			-150	μA
I _{IH} High								
I _O (OFF) Output current Hi-Z state	CE ₁ & CE ₂ = High, V _{OUT} = 0.5V CE ₁ & CE ₂ = High, V _{OUT} = 5.5V			-40			-60	μA
I _{OS} Short circuit ³								
I _{CC} V _{CC} supply current	CE ₁ & CE ₂ = Low, V _{OUT} = 0V High Stored	-20		-70	-15		-85	mA
C _{IN} Capacitance Input	CE ₁ & CE ₂ = High, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V			110	155		165	mF
C _{OUT} Output								
				5			5	pF
				8			8	

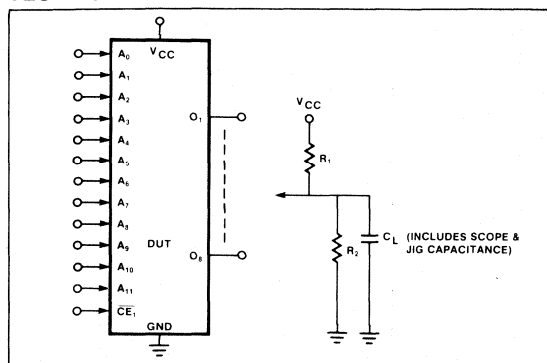
AC ELECTRICAL CHARACTERISTICS R₁ = 270Ω, R₂ = 600Ω, C_L = 30pF
 N82HS195: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82HS195: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER	TO	FROM	N82HS195			S82HS195			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T _{AA} ⁴ Access time	Output	Address			35		50	ns	
T _{CE} Output									Chip enable
T _{CD} Disable time	Output	Chip disable			25		30	ns	

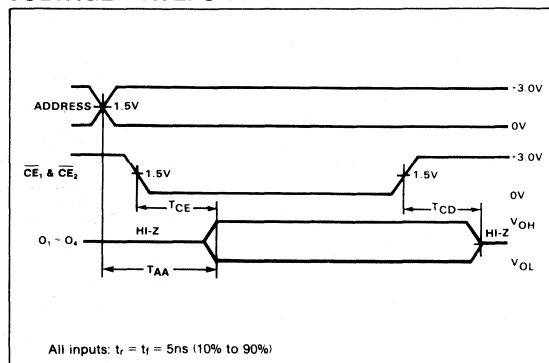
NOTES

- All voltage values are with respect to network ground terminal.
- Positive current is defined as into the terminal referenced.
- Duration of the short circuit should not exceed 1 second.
- Tested at an address cycle time of 1μsec.
- All typical values are at V_{CC} = 5V, T_A = 25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Section 12
PROMs,
32K-Bit

32,768-BIT BIPOLAR PROM (4096 × 8)

82S321 (T.S.)

Preliminary

DESCRIPTION

The 82S321 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data manual. The 82S321 is supplied with all outputs at a logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 2 chip enable inputs for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

The 82S321 device is available in the commercial and military ranges. For the commercial temperature range (0°C to +75°C) specify N82S321, I, N, and for the military temperature range (-55°C to +125°C) specify S82S321, I, R or G.

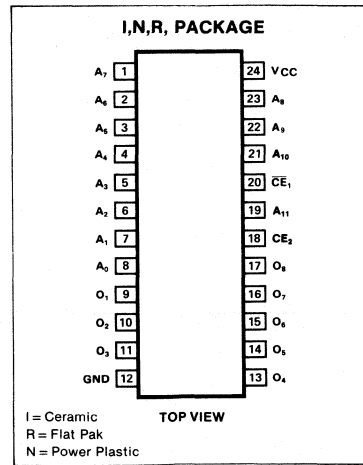
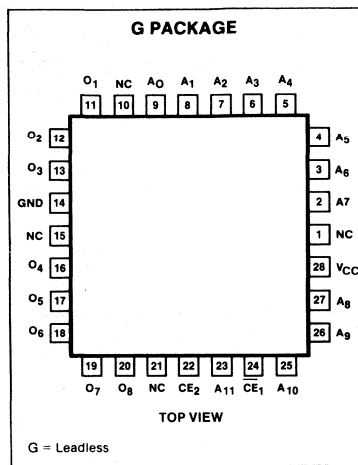
FEATURES

- Address access time:
N82S321: 80ns max
S82S321: 100ns max
- Power dissipation: 20μW/bit typ
- Input loading:
N82S321: -100μA max
S82S321: -150μA max
- 2 chip enable inputs
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are low level
- Fully TTL compatible

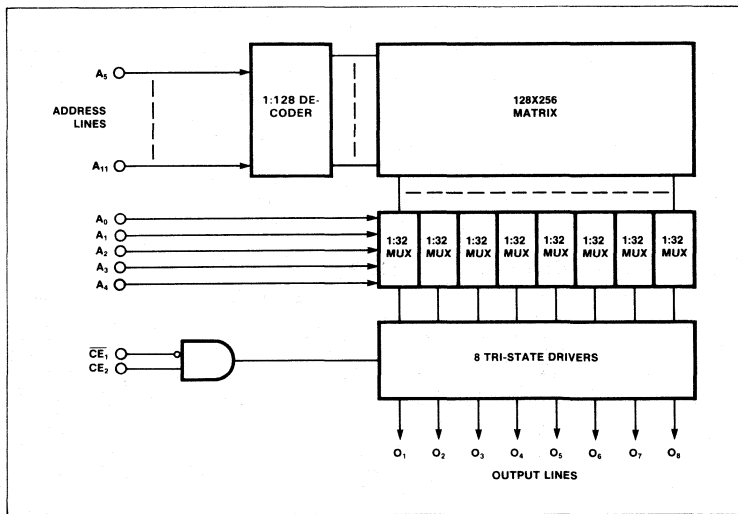
APPLICATIONS

- Prototyping/volume production
- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

PIN CONFIGURATIONS



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V _{CC} Supply voltage	17	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _O Output voltage	+5.5	Vdc
V _O Off-state	+5.5	Vdc
T _A Temperature range	Operating	°C
	N82S321	
	S82S321	-55 to +125
T _{STG} Storage	-65 to +150	

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32,768-BIT BIPOLAR PROM (4096 × 8)

82S321 (T.S.)

Preliminary

DC ELECTRICAL CHARACTERISTICS N82S321: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82S321: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TEST CONDITIONS ^{1,2}	N82S321			S82S321			UNIT
		Min	Typ ⁵	Max	Min	Typ	Max	
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp I _{IN} = -18mA	2.0	-0.8	-1.2	2.0		.85 -1.2	V
V _{OL} V _{OH}	Output voltage Low High C _{E1} = Low, C _{E2} = High I _{OUT} = 9.6mA I _{OUT} = -2mA	2.4		0.45	2.4		0.5	V
I _{IL} I _{IH}	Input current Low High V _{IN} = 0.45V V _{IN} = 5.5V			-100 40			-150 50	μA
I _{O(OFF)} I _{OS}	Output current Hi-Z state Short circuit ³ C _{E1} = High, C _{E2} = Low, V _{OUT} = 0.5 C _{E1} = High, C _{E2} = Low, V _{OUT} = 5.5 C _{E1} = Low, C _{E2} = High, V _{OUT} = 0V			-40 40			-60 60 -85	μA mA
I _{CC}	V _{CC} supply current		130	175			185	mA
C _{IN} C _{OUT}	Capacitance Input Output C _{E1} = High, C _{E2} = Low, V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82S321: $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$
 S82S321: $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$

PARAMETER	TO	FROM	N82S321			S82S321			UNIT
			Min	Typ ⁵	Max	Min	Typ	Max	
T _{AA} ⁴ T _{CE}	Access time Output	Address Chip enable		50 20	80 40			100 45	ns
T _{CD}	Disable time Output	Chip disable		20	40			45	ns

NOTES

1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.

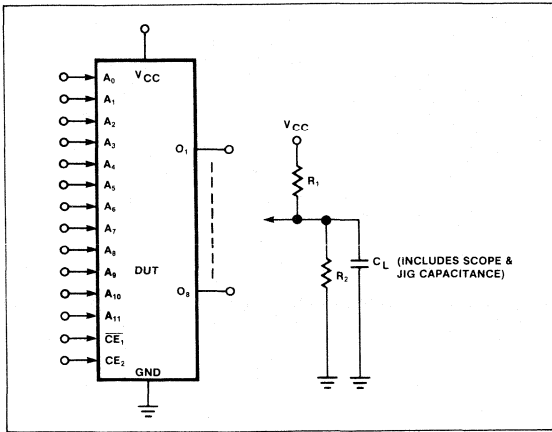
4. Tested at an address cycle time of 1μsec.
5. Typical values are at V_{CC} = 5V, T_A = 25°C.

32,768-BIT BIPOLAR PROM (4096 × 8)

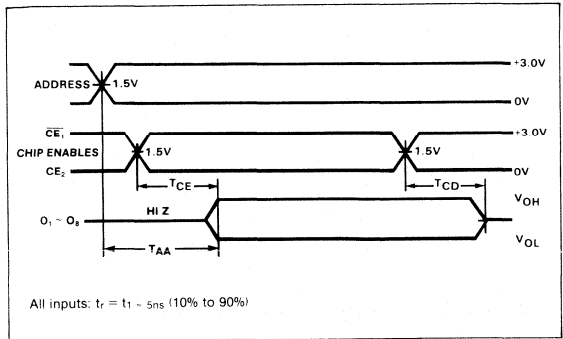
82S321 (T.S.)

Preliminary

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Section 13 Military Products

MILITARY PRODUCTS

MILITARY PRODUCTS/ PROCESS LEVELS

The Signetics MIL 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Fully compliant 883 flows on all products.
- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customer to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3, 4 and 5.

JAN QUALIFIED (JB)

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M 38510, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by the Defense Electronic Supply Center (DESC) and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883 Method 5005, is performed on each six weeks of production on each slash sheet for each package type. Group C, per Mil-Std-883 Method 5005, is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883 Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES						
	CAN		DUAL-IN-LINE				
	8-PIN	10-PIN	8-PIN	14-PIN	16-PIN	18-PIN	24-PIN
PB	—	—	FE	—	—	—	—
CB	—	—	—	F	—	—	—
EB	—	—	—	—	F	—	—
JB	—	—	—	—	—	—	F
DB	—	—	—	W	—	—	—
FB	—	—	—	—	W	—	—
ZC	—	—	—	—	—	—	Q
GC	H	—	—	—	—	—	—
IC	—	H	—	—	—	—	—
VB	—	—	—	—	—	I	—

All products listed are also available in Die form.

Table 1 MILITARY PACKAGE AVAILABILITY

	JB	RB	RC
	Jan Qualified	883B	883C
54	X	X	X
54LS	X	X	X
54S	X	X	X
82	X	X	X
8T	—	X	X
93XX	X	X	X
96XX	—	X	X
Analog	X	X	X
Bipolar Memory	X	X	X
Microprocessor	—	X	X

Table 2 MILITARY SUMMARY

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883 Method 5004, and is 100% electrically tested to industry data sheets. Devices are selectively available as custom processed parts with electricals screened to the JAN Slash Sheets.

MIL-STD-883, LEVEL C

If you need a Military temp, range device, but do not require burn in screening performed, our 883C product is ideal. 883C parts are the standard full Mil-Temperature range product to the Signetics data sheet parameters and screened to MIL-STD-883, Class C.

MILITARY GENERIC DATA

Signetics has a new program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity of running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily avail-

able before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

MILITARY PRODUCTS

PROCESS LEVEL AND MARKING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFFSHORE
JB JM38510XXXXX	2010, Cond. B	Yes	100%	100%	100%	Yes	No
RB SXXXX883B	2010, Cond. B	Yes	100%	100%	100%	No	Yes
RC SXXXX883C	2010, Cond. B	No	100%	100% dc Sample ac	Sample dc only	No	Yes

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

QUALIFIED	QUALIFIES	OPTION 1	OPTION 2
SUB-GROUPS			
A*	Electrical Test		
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within 6 weeks of the manufacturing period on the same production line through final seal.	Data selected from devices manufactured within 24 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 48 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 24 weeks of manufacturing period. If specific data not available, Option 2 will be supplied	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*

Group A is performed on each lot or subplot of Signetics devices.

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

MILITARY PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			CLASS S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
D. Dynamic Test @25°C	Sub Group 4 (for Linear Product Mainly)		X	X	X	X
E. Functional Test @25°C	Sub Group 7		X	X	X	X
F. Switching Test @25°C	Sub Group 9		X	X	X	N/A
15. Percent Defective allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @25°C (A-1). This is controlled by the slash sheets for JB products. For RB 10% is standard	10%	10% 3% Funct'l	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	As Req'd	JM38510 / XXXX Slash Sheet #	S X X X X 883B	SXXXX 883C
17. X-Ray	2012		100%	N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X
Quality Conformance Inspection per Method 5005 of Mil-Std 883						
19. Group A	Electrical Tests-Final Electricals (# 14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each Lot	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every 6 week per pkg. group	X	X	Generic Data Available	
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constant acceleration.	Every 3 months per circuit type	X	X	Generic Data Available	
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available	

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Cont'd)

MILITARY PRODUCTS SELECTION GUIDE

LOGIC—5400 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT- PACK	DIP	FLAT- PACK
5400	Quad 2-Input NAND Gate	/00104	1	1	F	W
5403	Quad 2-Input NAND Gate with o/c	/00109	—	—	F	—
5404	Hex Inverter	/00105	1	1	F	W
5411	Triple 3-Input AND Gate	—	—	—	F	W
5414	Hex Schmitt Trigger	/15102	—	—	F	W
5420	Dual 4-Input NAND Gate	/00102	1	1	F	W
5426	Quad 2-Input NAND Gate with o/c	/00805	1	—	F	—
5432	Quad 2-Input OR Gate	/16101	1	1	F	W
5442	BCD-to-Decimal Decoder	/01001	1	1	F	W
5443	Excess 3-to-Decimal Decoder	/01002	—	—	F	W
5446A	BCD-to-7 Segment Decoder/Driver	/01006	—	—	F	W
5447A	BCD-to-7 Segment Decoder/Driver	/01007	—	—	F	W
5473	Dual J-K Master-Slave Flip-Flop	/00202	1	1	F	W
5470	Dual D-Type Edge-Triggered Flip-Flop	/00205	—	—	F	W
5475	Quad Bistable Latch	/01501	1	1	F	W
5476	Dual J-K Master-Slave Flip-Flop	/00204	1	1	F	W
5477	Quad Bistable Latch	/01502	—	—	—	W
5483	4-Bit Binary Full Adder	/00602	—	—	F	W
5485	4-Bit Magnitude Comparator	/15001	1	1	F	W
5486	Quad 2-Input Exclusive-OR Gate	/00701	1	1	F	W
5491	8-Bit Shift Register	—	—	—	F	W
5493	4-Bit Binary Counter	/01302	1	1	F	W
5494	4-Bit Shift Register {PISO}	—	—	—	F	W
5496	5-Bit Shift Register	/00902	1	1	F	W
54109	Dual J-K Positive Edge-Triggered Flip-Flop	—	—	—	F	W
54116	Dual 4-Bit Latch with Clear	/01503	1	—	F	W
54121	Monostable Multivibrator	/01201	1	1	F	W
54122	Retriggerable Monostable Multivibrator	/01202	—	—	—	—
54123	Retriggerable Monostable Multivibrator	/01203	1	1	F	W
54132	Quad Schmitt Trigger	/15103	1	1	F	W
54148	8-Line to 3-Line Priority Encoder	/15602	—	—	F	W
54151	8-Line to 1-Line Mux	/01406	1	1	F	W
54153	Dual 4-Line to 1-Line Mux	/01403	1	1	F	W
54154	4-Line to 16-Line Decoder/Demux	/15201	1	—	F	W
54160	Synchronous 4-Bit Decade Counter	/01303	1	1	F	W
54161	Synchronous 4-Bit Binary Counter	/01306	1	1	F	W
54163	Synchronous 4-Bit Binary Counter	/01304	1	1	F	W
54164	8-Bit Parallel-Out Serial Shift Register	/00903	1	—	F	—
54165	Parallel-Load 8-Bit Shift Register	/00904	*	*	F	W
54174	Hex D-Type Flip-Flop with Clear	/01701	1	1	F	W
54175	Quad D-Type Edge-Triggered Flip-Flop	/01702	1	1	F	W
54180	8-Bit Odd/Even Parity Checker	/01901	1	1	F	W
54181	4-Bit Arithmetic Logic Unit	/01101	1	—	F	—
54190	Synchronous Up/Down Counter (BCD)	—	—	—	*	*
54191	Synchronous Up/Down Counter (Binary)	—	—	—	*	*
54193	Synchronous 4-Bit Binary Up/Down Counter	/01309	1	1	F	W
54194	4-Bit Bidirectional Universal Shift Register	/00905	1	1	F	W
54279	Quad S-R Latch	—	—	—	F	W
54365A	Hex Buffer w/Common Enable (3-State)	/16301	1	—	F	R
54366A	Hex Buffer w/Common Enable (3-State)	/16302	1	—	F	R
54367A	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16303	1	—	F	R
54368A	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16304	1	—	F	R
9309	Dual 4-Input Multiplexer	/01404	1	1	F	W

NOTE

1 = QPLI

2 = QPLII

* = In process

MILITARY PRODUCTS SELECTION GUIDE

LOGIC—54LS SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT- PACK	DIP	FLAT- PACK
54LS00	Quad 2-Input NAND Gate	/30001	1	1	F	W
54LS02	Quad 2-Input NOR Gate	/30301	1	1	F	W
54LS04	Hex Inverter	/30003	1	1	F	W
54LS08	Quad 2-Input AND Gate	/31004	1	1	F	W
54LS10	Triple 3-Input NAND Gate	/30005	1	1	F	W
54LS14	Hex Schmitt Trigger	/31302	1	1	F	W
54LS20	Dual 4-Input NAND Gate	/30007	1	1	F	W
54LS28	Quad 2-Input NOR Buffer	/30204	—	—	F	W
54LS30	8-Input NAND Gate	/30009	—	—	F	W
54LS32	Quad 2-Input OR Gate	/30501	1	1	F	W
54LS37	Quad 2-Input NAND Buffer	/30202	1	1	F	W
54LS42	BCD-to-Decimal Decoder	/30703	1	1	F	W
54LS51	Dual 2-Wide 2-Input A01 Gate	/30401	—	—	F	W
54LS73	Dual J-K Master-Slave Flip-Flop	/30101	2	2	F	W
54LS74	Dual D-Type Edge-Triggered Flip-Flop	/30102	1	1	F	W
54LS75	Quad Bistable Latch	31601	2	2	F	W
54LS76	Dual J-K Master-Slave Flip-Flop	30110	1	1	F	W
54LS83A	4-Bit Binary Full Adder	/31201	—	—	F	W
54LS86	4-Bit Magnitude Comparator Gate	/31101	1	1	F	W
54LS88	Quad 2-Input Exclusive-OR Gate	/30502	1	1	F	W
54LS90	Decade Counter	/31501	1	1	F	W
54LS92	Divide-by-Twelve Counter	/31510	1	1	F	W
54LS93	4-Bit Binary Counter	/31502	1	1	F	W
54LS95	4-Bit Left-Right Shift Register	/30603	1	1	F	W
54LS96	5-Bit Shift Register	/30604	1	1	F	W
54LS107	Dual J-K Master-Slave Flip-Flop	/30108	1	1	F	W
54LS109	Dual J-K Positive Edge-Triggered Flip-Flop	/30109	1	1	F	W
54LS112	Dual J-K Negative Edge-Triggered Flip-Flop	/30103	1	1	F	W
54LS113	Dual J-K Negative Edge-Triggered Flip-Flop	/30104	1	1	F	W
54LS125	Quad Bus Buffer Gate w/3-State Outputs	/32301	1	1	F	W
54LS126	Quad Bus Buffer Gate w/3-State Outputs	/32302	1	1	F	W
54LS13	Quad Schmitt Trigger	/31303	—	—	F	W
54LS136	Quad Exclusive-or with o/c	—	—	—	F	W
54LS138	3-to-8 Line Decoder/Demux	/30701	1	1	F	W
54LS139	Dual 2-to-4 Line Decoder/Demux	/30702	—	—	F	W
54LS151	8-Line to 1-Line Mux	/30901	—	—	*	*
54LS153	Dual 4-Line to 1-Line Mux	/30902	1	1	F	W
54LS154	4-Line to 16-Line Decoder/Demux	—	—	—	1	Q
54LS156	Dual 2-Line to 4-Line Decode/Demux	/32602	2	2	F	W
54LS157	Quad 2-Input Data Selector (non-inv.)	/30903	—	—	F	W
54LS158	Quad 2-Input Data Selector (inv.)	/30904	—	—	F	W
54LS160A	Synchronous 4-Bit Decade Counter	/31503	*	*	F	W
54LS161A	Synchronous 4-Bit Binary Counter	/31504	*	*	F	W
54LS162	Synchronous 4-Bit Decade Counter	/31511	—	—	F	W
54LS163	Synchronous 4-Bit Binary Counter	/31512	1	1	F	W
54LS164	8-Bit Parallel-Out Serial Shift Register	/30605	1	1	F	W
54LS173	Quad D-Type Flip-Flop (3-State) (8T10)	—	—	—	F	W
54LS174	Hex D-Type Flip-Flop with Clear	/30106	1	1	F	W
54LS175	Quad D-Type Edge-Triggered Flip-Flop	/30107	1	1	F	W
54LS181	4-Bit Arithmetic Logic Unit	/30801	1	—	F	W
54LS190	Synchronous Up/Down Counter (BCD)	/31513	1	1	F	W
54LS191	Synchronous Up/Down Counter (Binary)	/31509	1	1	F	W

NOTE

1 = Level 1 Qualification

2 = Level 2 Qualification

* = In process

MILITARY PRODUCTS SELECTION GUIDE

LOGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM385 10 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT- PACK	DIP	FLAT- PACK
54LS192	Synchronous Decade Up/Down Counter	/31507	*	*	F	W
54LS193	Synchronous 4-Bit Binary Up/Down Counter	/31508	1	1	F	W
54LS194A	4-Bit Bidirectional Universal Shift Register	/30601	—	—	F	W
54LS195A	4-Bit Parallel-Access Shift Register	/30602	1	1	F	W
54LS197	Presettable Binary Counter/Latch (8291)	/32002	*	*	F	W
54LS221	Dual Monostable Multivibrator	/31402	—	—	*	*
54LS240	Octal Inverter Buffer 3-State	/32401	*	—	F	—
54LS241	Octal Buffer 3-State	/32402	*	—	F	—
54LS242	Quad Inverting TCRS. 3-State	/32801	*	*	F	W
54LS243	Quad TCRS. 3-State	/32802	*	*	F	W
54LS244	Octal Buffer 3-State	/32403	*	—	F	—
54LS245	Octal TCRS. 3-State	/32803	*	—	F	—
54LS251	Data Selector/Mux with 3-State Outputs	/30905	—	—	*	*
54LS253	Dual 4-Line to 1-Line Data Selector/Mux	/30908	—	—	F	W
54LS257A	Quad 2-Line to 1-Line Data Selector/Mux	/30906	1	1	*	*
54LS258A	Quad 2-Line to 1-Line Data Selector/Mux	/30907	1	1	*	*
54LS260	Dual 5-Input NOR Gate	—	—	—	F	W
54LS261	2X4 Parallel Binary Multiplier	/31801	—	—	F	W
54LS266	Quad Exclusive-NOR Gate	/30303	1	1	F	W
54LS273	Octal D. Flip Flop	/32501	2	*	F	W
54LS279	Quad S-R Latch	/31602	*	*	F	W
54LS283	4-Bit Adder	/31202	—	—	F	W
54LS290	Decade Counter	/32003	1	1	F	W
54LS293	4-Bit Binary Counter	/32004	1	1	F	W
54LS295B	4-Bit Right-Shift Left-Shift Register	/30606	1	1	F	W
54LS298	Quad 2-Input Mux with Storage	—	—	—	F	W
54LS365	Hex Buffer w/ common Enable (3-State)	/32201	1	1	F	W
54LS366	Hex Buffer w/Common Enable (3-State)	/32202	—	—	F	W
54LS367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32203	1	1	F	W
54LS368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32204	1	1	F	W
54LS373	Octal Transparent Latch (3-State)	/32502	*	—	F	—
54LS374	Octal D Flip Flop (3-State)	/32503	—	—	F	—
54LS375	Quad Latch	—	—	—	F	W
54LS377	Octal D Flip Flop Clock Enable	/32504	—	—	F	—
54LS395A	4-Bit Cascadeable Shift Register (3-State)	/30607	1	1	F	W
54LS670	4X4 Register File (3-State)	/31901	—	—	F	W

NOTE

1=Level 1 Qualification

2=Level 2 Qualification

* = in Process

MILITARY PRODUCTS SELECTION GUIDE

LOGIC—8T INTERFACE SERIES

DEVICE	DESCRIPTION	JAN M38510 SHEET	MIL-STD 883	
			DIP	FLAT- PACK
8T05	7-Segment Decoder Display Driver (Active-Hi Outputs)	—	F	W
8T09	Quad Bus Driver with 3-State Outputs	—	F	W
8T13	Dual Line Driver	—	F	W
8T18	Dual 2-Input NAND (High Voltage to TTL Interface)	—	F	W
8T22	Retriggerable Monostable Multivibrator (54122/9601)	—	F	W
8T26A	Quad Bus Driver/Receiver (3-State Outputs)	—	F	R
8T28	Quad Non-Inverting Bus Driver/Receiver (3-State Outputs)	—	F	W
8T31	8-Bit Bidirectional I/O Port	—	*	*
8T32	Programmable 8-Bit, I/O Port (3-State), IV Byte	—	I	*
8T33	Programmable 8-Bit, I/O Port (Open Collector), IV Byte	—	I	*
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)	—	I	W
8T37	Hex Bus Receiver with Hysteresis-Schmitt Trigger	—	F	W
8T38	Quad Bus Transceiver (Open Collector) (DM8838)	—	F	W
8T80	Quad 2-Input NAND Gate (High Voltage)	—	F	W
8T90	Hex Inverter (High Voltage)	—	F	W
8T95	High Speed Hex Buffers/Inverters (74365/DM8095)	—	F	R
8T97	High Speed Hex Buffers/Inverters (74367/DM8097)	—	F	R
8T98	High Speed Hex Buffers/Inverters (74368/DM8098)	—	F	R
8T126	Quad 3-State Transceivers	—	F	W
8T127	Quad 3-State Transceivers	—	F	W
8T128	Quad 3-State Transceivers	—	F	W
8T129	Quad 3-State Transceivers	—	F	W

* = Qualification planned

MILITARY PRODUCTS SELECTION GUIDE

LOGIC—54S SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT- PACK	DIP	FLAT- PACK
54S00	Quad 2-Input NAND Gate	/07001	1	1	F	W
54S02	Quad 2-Input NOR Gate	/07301	1	1	F	W
54S04	Hex Inverter	/07003	1	1	F	W
54S08	Quad 2-Input AND Gate	/08003	1	1	F	W
54S10	Triple 3-Input NAND Gate	/07005	1	1	F	W
54S11	Triple 3-Input NAND Gate	/08001	1	1	F	W
54S20	Dual 4-Input NAND Gate	/07006	—	—	F	W
54S30	8-Input NAND Gate	/07008	—	—	—	—
54S40	Dual 4-Input NAND Buffer	/07201	1	1	F	W
54S51	Dual 2-Wide 2-Input A01 Gate	/07401	1	1	F	W
54S74	Dual D-Type Edge-Triggered Flip-Flop	/07101	1	1	F	W
54S85	4-Bit Magnitude Comparator	/08201	1	—	F	—
54S86	Quad 2-Input Exclusive-OR Gate	/07501	1	1	F	W
54S112	Dual J-K Negative Edge-Triggered Flip-Flop	/07102	1	1	F	W
54S113	Dual J-K Negative Edge-Triggered Flip-Flop	/07103	2	2	F	W
54S133	13-Input NAND Gate	/07009	1	1	F	W
54S135	Quad Exclusive-OR/NOR Gate	/07502	—	—	—	—
54S138	3-to-8 Line Decoder/Demux	/07701	—	—	—	—
54S139	Dual 2-to-4 Line Decoder/Demux	/07702	—	—	F	W
54S140	Dual 4-Input NAND Line Driver	/08101	1	1	F	W
54S151	8-Line to 1-Line Mux	/07901	1	1	F	W
54S153	Dual 4-Line to 1-Line Mux	/07902	1	1	F	W
54S157	Quad 2-Input Data Selector (non.inv.)	/07903	1	1	F	W
54S158	Quad 2-Input Data Selector (inv)	/07904	1	1	F	W
54S174	Hex D-Type Flip-Flop with Clear	/07105	—	—	F	W
54S175	Quad D-Type Edge-Triggered Flip-Flop	/07106	—	—	—	—
54S181	4-Bit Arithmetic Logic unit	/07801	1	—	F	*
54S182	Look-Ahead Carry Generator	/07802	—	—	*	*
54S194	4-Bit Bidirectional Universal Shift Register	/07601	—	—	—	—
54S195	4-Bit Parallel-Access Shift Register	/07602	—	—	—	—
54S251	Data Selector/Mux with 3-State Outputs	/07905	—	—	—	—
54S253	Dual 4-Line to 1-Line Data Selector/Mux	—	—	—	F	W
54S257	Quad 2-Line to 1-Line Data Selector/Mux	/07906	—	—	—	—
54S258	Quad 2-Line to 1-Line Data Selector/Mux	/07907	—	—	—	—
54S26C	Dual 5-Input NOR Gate	—	—	—	F	W
54S280	9-Bit Odd/Even Parity Generator/Checker	/07703	—	—	—	—

NOTE

Per QPL 38510-32 dated
10 January 1978

1=Level 1 Qualification

2=Level 2 Qualification

* = In Process

MILITARY PRODUCTS SELECTION GUIDE

BIPOLAR MEMORY

DEVICE	ORGANIZATION	PACKAGE	OUTPUT CIRCUIT	NUMBER OF PINS
PROMs				
82S23	32 × 8	F R	OC	16
82S115	512 × 8	I R	TS	24
82S123	32 × 8	F W	TS	16
82S126	256 × 4	F W	OC	16
82S129	256 × 4	F R	TS	16
82S130	512 × 4	F R	OC	16
82S131	512 × 4	F R	TS	16
82S137	1024 × 4	F R	TS	18
82HS137	1024 × 4	F R	TS	18
82S141	512 × 8	F R	TS	24
82S147	512 × 8	F R	TS	20
82S181	1024 × 8	F R,G	TS	24
82HS181	1024 × 8	F R,G	TS	24
82LS181	1024 × 8	F R	TS	24
82S185	2048 × 4	I R	TS	18
82HS185	2048 × 4	I R	TS	18
82S2708	1024 × 8	F R	TS	24
82S191	2048 × 8	F,I R,G	TS	24
82HS191	2048 × 8	F,I R,G	TS	24
82HS195	4096 × 4	I R	TS	20
82S321	4096 × 8	I R	TS	24
FPLF				
82S100	16 × 48 × 8	F,I R,G	TS	28
82S101	16 × 48 × 8	F,I R,G	OC	28
82S102	16 × 9	F,I R	OC	28
82S103	16 × 9	F,I R	TS	28
82S104	16 × 48 × 8	F,I R	OC	28
82S105	16 × 48 × 8	F,I R	TS	28
82S106	16 × 48 × 8	F,I R	OC	28
82S107	16 × 48 × 8	F,I R	TS	28
82S152	18 × 32 × 10	F R,G	OC	20
82S153	18 × 32 × 10	F R,G	TS	20
82S157	16 × 32 × 12	F R,G	OC	20
82S158	16 × 32 × 12	F R,G	TS	20
RAMs				
54S189	16 × 4	F R	TS	16
54S301	256 × 1	F R	OC	16
82S09	64 × 9	I R	OC	28
82S19	64 × 9	I R	OC	28
82S16	256 × 1	F R	TS	16
82LS16	256 × 1	F W	TS	16
82LS17	256 × 1	F W	OC	16
54LS301	256 × 1	F W	OC	16
82S210	256 × 9	F R	TS	24
82S212	256 × 9	F R	TS	22
8X350	256 × 8	F R	TS	22

MILITARY PRODUCTS SELECTION GUIDE**BIPOLAR MEMORY — JAN**

JAN M-38510			
DEVICE	SLASH SHEET	PKG	QUAL STATUS
82S23	/20701	F	QPL I
82S123	/20702	F	QPL I
82S126	/20301	F	QPL I
82S129	/20302	F	QPL I
82S130	/20401	F	QPL I
82S131	/20402	F	QPL I
82S137	/20602	F	QPL I
82S141	/20802	F	QPL I
82S115	/20803	F	In Process
82S181	/20904	F	QPL I
82S185	/20902	I	QPL I
82S2708	/20905	I	In Process
82S191	/21002	I	QPL I
82S100	/1501	I	In Process

Per QPL M38510-52 dated 11 Feb '82.

MILITARY PRODUCTS SELECTION GUIDE

LINEAR DEVICES

DEVICE	DESCRIPTION	PACKAGE*	
		DIP	CAN
OPERATIONAL AMPLIFIERS			
LF155	JFET Op Amp		H
LF156	JFET Op Amp		H
LH2101A	Dual Op Amp	F	
LM101/A	Hi Perf Op Amp	F	H
LM124	Quad Op Amp	F	
LM158	Dual Op Amp		H
MC1556	Hi Perf Op Amp	F	H
MC1558	Dual Op Amp	F	H
SE530	Hi Slew Op Amp	F	H
SE532	Dual Op Amp		H
SE5512	Dual Op Amp	FE	H
SE5532	Dual Op Amp	F,FE	H
SE5532A	Dual Op Amp	FE	
SE5534	Lo Noise Op Amp	F,FE	H
SE5534A	Lo Noise Op Amp	FE	H
SE5537	Sample and Hold Amp	FE	H
SE5539	High Freq Op Amp	F	—
μA747	Dual Op Amp	F	H
COMPARATORS			
SE521	Dual Differential Comparator	F	
SE522	Dual Differential Comparator	F	
SE527	Voltage Comparator	F	H
SE529	Voltage Comparator	F	H
LH2111	Dual Voltage Comparator	F	
LM111	Voltage Comparator	F	H
LM139/A	Quad Voltage Comparator	F	
LM193/A	Dual Voltage Comparator		H
DIFFERENTIAL AMPLIFIERS			
SE510	Dual Differential Amplifier	F	
SE511	Dual Differential Amplifier	F	
μA733	Video Amplifier	F	H
PHASE LOCKED LOOPS			
SE567	Tone Decoder PLL	F	H
SE564	Phase Locked Loop	F	H
TIMERS			
SE555	Timer	F,FE	H
SE556-1	Dual Timer	F	
SE558	Quad Timer	F	

DEVICE	DESCRIPTION	PACKAGE*	
		DIP/ CAN	CAN
VOLTAGE REGULATORS			
SE5553	Dual Track Reg	F	H
SE5554	Dual Track Reg	F	H
μA723	Adj Volt Reg	F	H

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
D to A CONVERTERS			
DAC-08	8-Bit Mult DAC	F,Q	H
MC1508-8	8-Bit Mult DAC	F	—
SE5008	8-Bit Mult DAC	F	—
SE5009	8-Bit Mult DAC	F	—
SE5018	8-Bit μP-Comp DAC	F	—
SE5019	8-Bit μP-Comp DAC	F	—
SE5118	8-Bit μP-Comp DAC	F	—
SE5119	8-Bit μP-Comp DAC	F	—

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
DUAL LINE RECEIVERS			
DS7820/A	Dual Line Receiver	F	—
DS7830/A	Dual Diff Line Driver	F	—

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
MOS FET SWITCH			
SD210	Switch N-Channel Enhance	EE	—
SD211	Switch N-Channel Enhance	EE	—
SD5002	Quad Analog Switch	1	

DEVICE	DESCRIPTION	PACKAGE	
		DIP	CAN
SMPS CONTROL CIRCUITS			
SE5560	SMPS Controller	F	—
SG1524	Reg Pulse Width Mod	F	—

JAN M - 38510			
DEVICE	SLASH SHEET	PKG	QUAL STATUS
SE555	10901BGC	H	QPL 1
SE556-1	10902BCB	F	QPL 1
LH2101A	10105BEB	F	QPL 1
LM101A	10103BCB	F	QPL 1
LM101A	10103BPB	FE	QPL 1
LM101AH	10103BGC	H	QPL 1
μA741	10101BGC	H	QPL 1
μA747	10102BGC	H	QPL 1
DAC-08A	11302BCB	F	IN PROCESS

NOTES
 F = Cerdip
 H = TO-5

MILITARY PRODUCTS LINEAR INDUSTRY CROSS REFERENCE

LINEAR INDUSTRY CROSS REFERENCE

FAIRCHILD	SIGNETICS
μ A111	LM111
μ A139	LM139
μ A733	μ A733
μ AF155/156	LF155/156
μ A101	LM101
μ A101A	LM101A
MC1556	MC1556
μ A1558	MC1558
μ A747	μ A747
MC1555	SE555
μ A556	SE556
μ A109	LM109
μ A79XX	79XX(7)
μ A723	μ A723

MOTOROLA	SIGNETICS
MLM111	LM111
MC1733	μ A733
LF155/56	LF155/156
MLM101	LM101
MLM101A	LM101A
MC1558	MC1558
MC1747	μ A747
MC3556	SE556
MLM109	LM109
MC78XX	78XX(7)
MC79XX	79XX(7)
MC1723	μ A723
MC1508	MC1508-8

NATIONAL	SIGNETICS
LM161	SE527
LH2111	LH2111
LM111	LM111
LM119	LM119
LM139	LM139
LM193	LM193/193A
LM733	μ A733
LF155/56	LF155/156
LH2101A	LH2101A
LH2108A	LH2108A
LM101A	LM101
LM101	LM101A
LM124	LM124
LM158	LM158
LM1558	MC1558
LM1581	SE532
LM747	μ A747
LM567	SE567
DM7820	DM7820
DM7830	DM7830
LM555	SE555
LM109	LM109
LM723	μ A723

PMI	SIGNETICS
SSS1508	MC1508-8
DAC-08	SE5008

RAYTHEON	SIGNETICS
LM111	LM111
LM139	LM139
RM733	μ A733
LF155/56/57	LF155/156
LM101	LM101
LM101A	LM101A
LM124	LM124
RM1556	MC1556
RM1558	MC1558
RM747	μ A747
RM555	SE555
LM109	LM109
RM723	μ A723

T.I.	SIGNETICS
LM111	LM111
SN52733	μ A733
LF155/56	LF155/156
SN52101A	LM101A
SN55182	DM7820
SN55183	DM7830
SN52555	SE555
SE556	SE556
LM109	LM109
μ A79XX	μ A79XX(7)
SN52723	μ A723

Section 14 Packages

PACKAGES—GENERAL INFORMATION

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
 - a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power application across VCC and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

5. Lead material: Alloy 42 (Nickel/Iron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.
9. SO Packages-microminature packages.
 - a. Lead material: Alloy-42.
 - b. Body material: Plastic (Epoxy).

Hermetic Only

10. Lead material
 - a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
 - b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated or solder dipped.
 - c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
11. Body Material
 - a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
 - b. Ceramic with glass seal at leads.
 - c. BeO ceramic with glass seal at leads.
 - d. Ceramic with ASTM alloy F-30 or equivalent.

12. Lid Material

- a. Nickel or tin plated nickel, weld seal.
 - b. Ceramic, glass seal.
 - c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
 - d. BeO Ceramic with glass seal.
13. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
 14. Recommended minimum offset before lead bend.
 15. Maximum glass climb .010 inches.
 16. Maximum glass climb or lid skew is .010 inches.
 17. Typical four places.
 18. Dimension also applies to seating plane.

PLASTIC PACKAGES

NO. OF LEADS	PACKAGE CODE	θ_{ja}/θ_{jc} (°C/W)	DESCRIPTION ¹
Standard Dual-In-Line			
8	NE	162/65	
14	NH	150/65	TO-116/MO-001
16	NJ	137/53	MO-001
18	NK	135/53	
20	NL	135/53	
22	NM	120/53	
24	NN	116/53	MO-015
24	NNE NNF	120/60	Slim Line
28	NQ	116/53	MO-015
40	NW	110/50	MO-015
Power Dual-In-Line²			
14	NHA	95/33	Butterfly
16	NJA	95/33	Butterfly
18	NKA	90/26	Butterfly
20	NLA	90/26	Butterfly
24	NNA	60/23	Heatsink
28	NQA	56/21	Heatsink
SO Packages			
8	DE	110	SO-8
14	DH	100	SO-14
16	DJ	100	SO-16

NOTES

1. Dual-in-Line packages unless otherwise described.
2. Package outline is the same as corresponding standard Dual-in-Line package with identical number of leads.

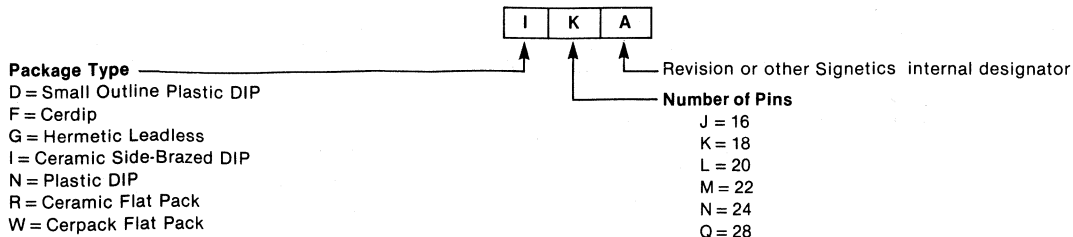
PACKAGES—GENERAL INFORMATION

HERMETIC PACKAGES

NO. OF LEADS	PACKAGE CODE	$\theta_{ja}/\theta_{jc}(^{\circ}\text{C}/\text{W})$	DESCRIPTION ¹
Metal Headers			
3	HBA	100/20	TO-5 Header
4	EC	100/20	TO-46 Header
4	EE	150/25	TO-72 Header
8	HEA/HEB	150/25	TO-5 Header
10	HFB/HFA	150/25	TO-5/TO-100 Header, Short Can
10	HFD/HFC	150/25	TO-5/TO-100 Header, Tall Can
Flat Packs			
10	QF	230/55	Flat Ceramic
10	WF	240/50	Flat Ceramic
14	QHA	185/45	Flat Ceramic Laminate
14	WH	205/50	Flat Ceramic
16	QJA	170/45	Flat Ceramic Laminate
16	RJA	133/30	Flat Ceramic, BeO
16	WJ	200/50	Flat Ceramic
18	RKA	107/22	Flat Ceramic, BeO
24	QNA	155/44	Flat Ceramic Laminate
24	RNA	107/22	Flat Ceramic, BeO
24	WN	155/40	Flat Ceramic
28	RQA	107/22	Flat Ceramic, BeO
40	RWA	95/20	Flat Ceramic, BeO
Cerdip Family			
8	FE	110/30	Dual-in-Line Ceramic
14	FH	110/30	Dual-in-Line Ceramic
16	FJ	100/30	Dual-in-Line Ceramic
18	FK	93/27	Dual-in-Line Ceramic
20	FL	90/25	Dual-in-Line Ceramic
22	FM	75/27	Dual-in-Line Ceramic
24	FN	60/26	Dual-in-Line Ceramic
28	FQ	57/27	Dual-in-Line Ceramic
Laminated Ceramic, Side Brazed Lead			
8	IEA	100/30	Dip Laminate
14	IHA	95/25	Dip Laminate
16	IJA	90/25	Dip Laminate
18	IKA/IKB	88/25	Dip Laminate
22	IMA	80/25	Dip Laminate
24	INC/INH	65/25	Dip Laminate
28	IQA	60/25	Dip Laminate
28	GQ*	90/35	Chip Carrier
40	IWA	55/25	Dip Laminate
44	GX*	75/30	Chip Carrier
48	JY*	55/25	Dual-in-Line Ceramic
50	IZA	42/20	Dip Laminate

¹Contact factory for Package drawings.

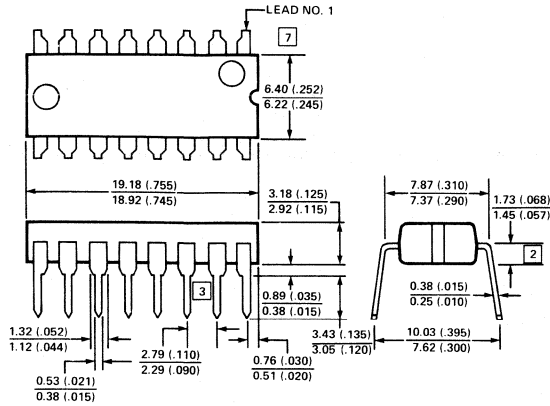
Memory Package Codes consist of two or three alphas as follows:



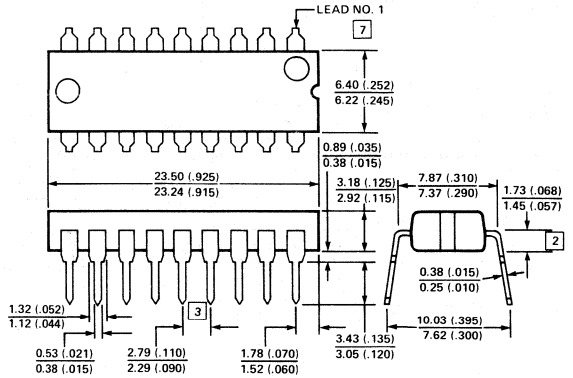
PACKAGES

PLASTIC: Standard and Power Dual-In-Line

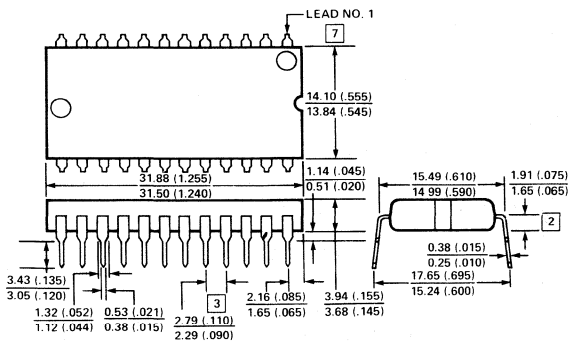
NJ Package



NK Package



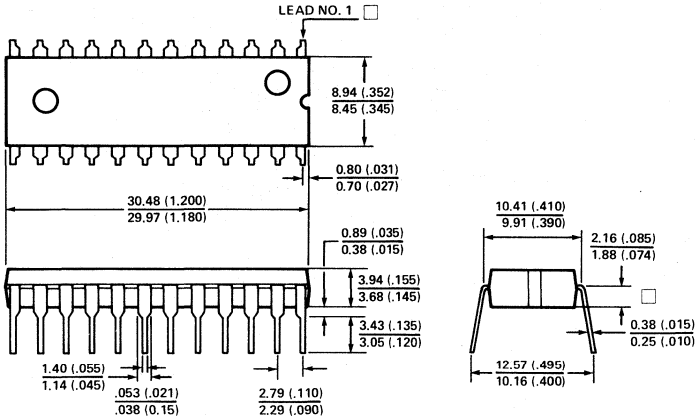
NN Package



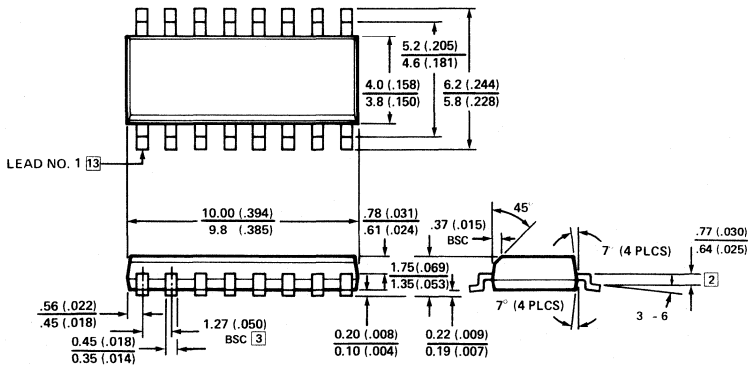
PACKAGES

PLASTIC: Standard and Power Dual-In-Line (cont'd.)

NNE/NNF Package



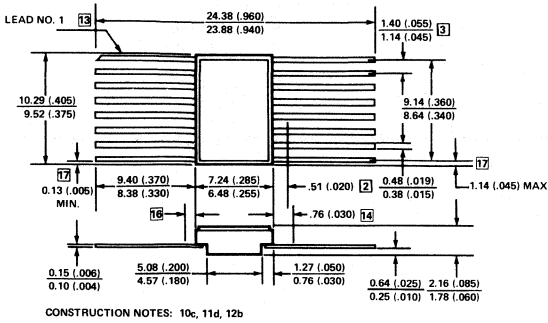
DJ Package



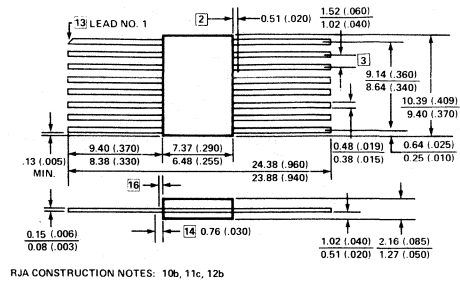
PACKAGES

HERMETIC: Flat Packs

QJA Package

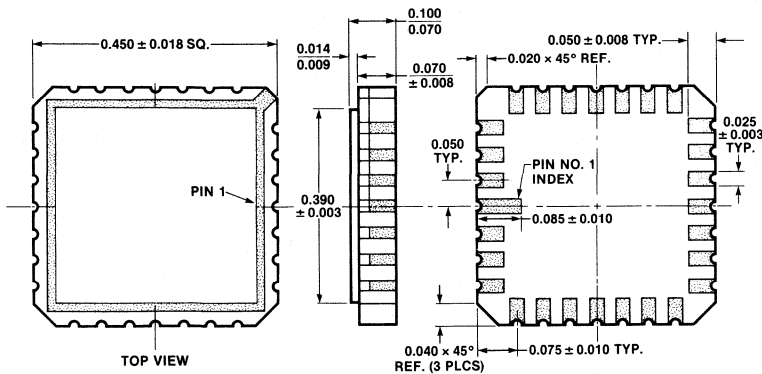


RJA Package



LEADLESS:

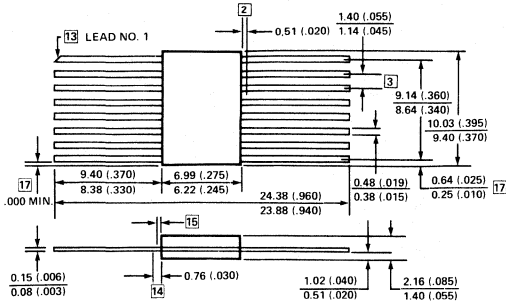
GQ Package



PACKAGES

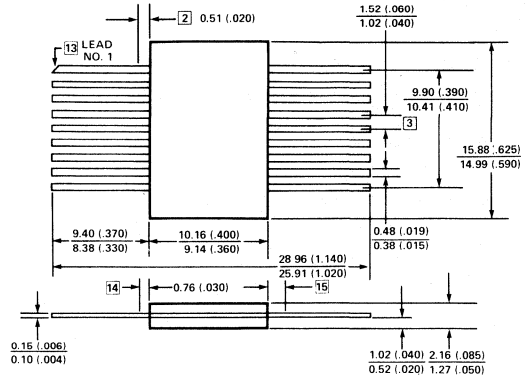
HERMETIC: Flat Packs (cont'd.)

WJ Package



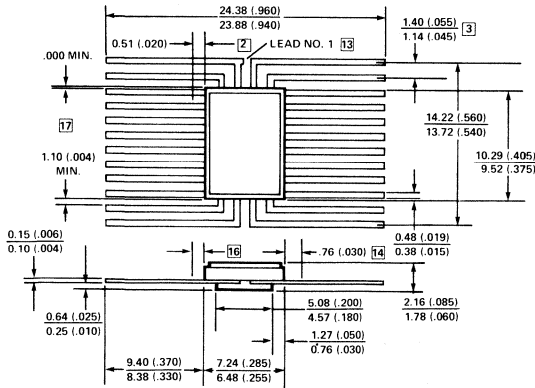
CONSTRUCTION NOTES: 10b, 11b, 12b

RKA Package



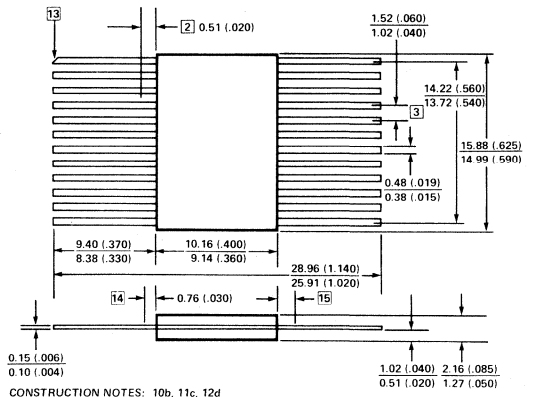
CONSTRUCTION NOTES: 10b, 11c, 12d

QNA Package



CONSTRUCTION NOTES: 10c, 11d, 12b

RNA Package

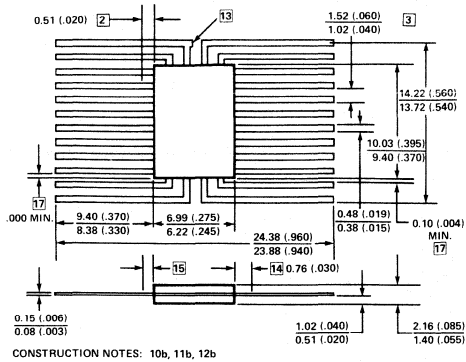


CONSTRUCTION NOTES: 10b, 11c, 12d

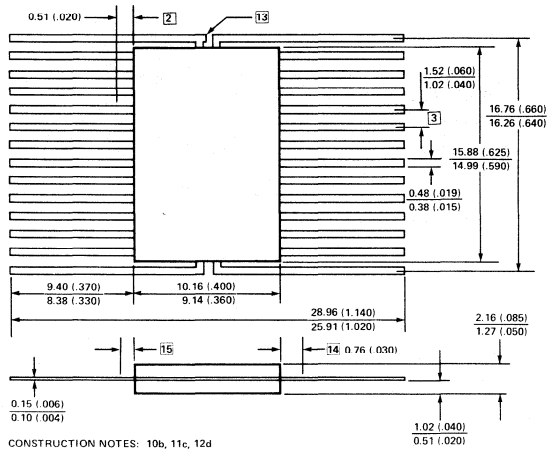
PACKAGES

HERMETIC: Flat Packs (cont'd.)

WN Package



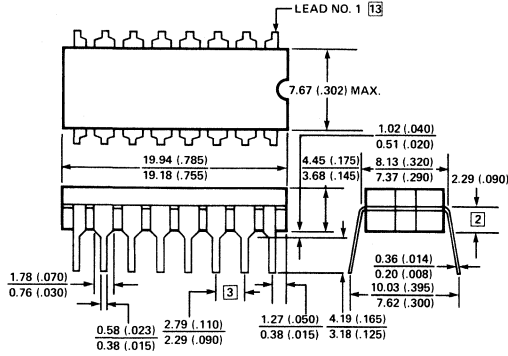
RQA Package



PACKAGES

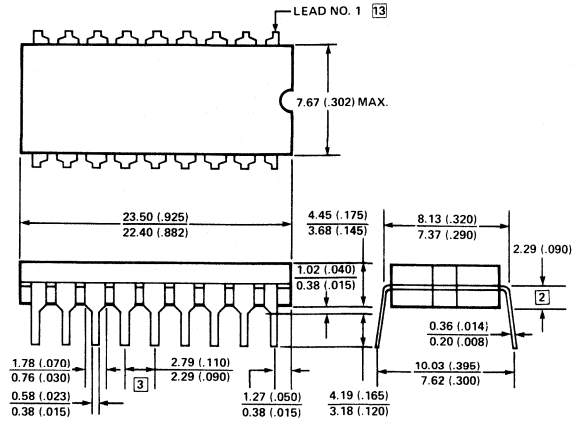
HERMETIC: Cerdip Family

FJ Package



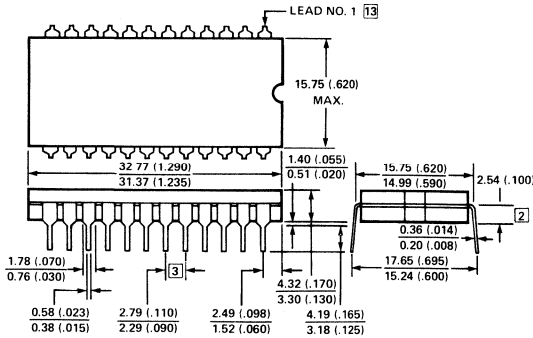
CONSTRUCTION NOTES: 10b, 11b, 12b

FK Package



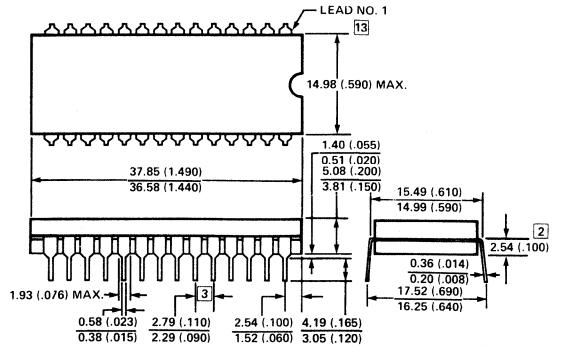
CONSTRUCTION NOTES: 10b, 11b, 12b

FN Package



CONSTRUCTION NOTES: 10b, 11b, 12b

FQ Package

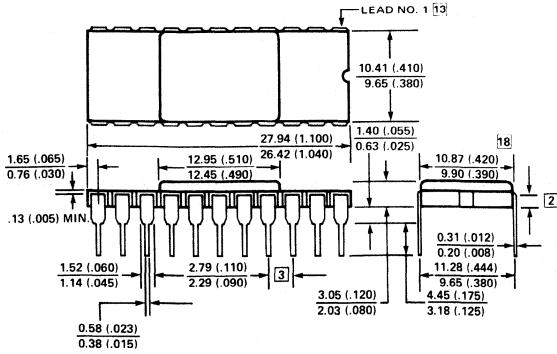


CONSTRUCTION NOTES: 10b, 11b, 12b

PACKAGES

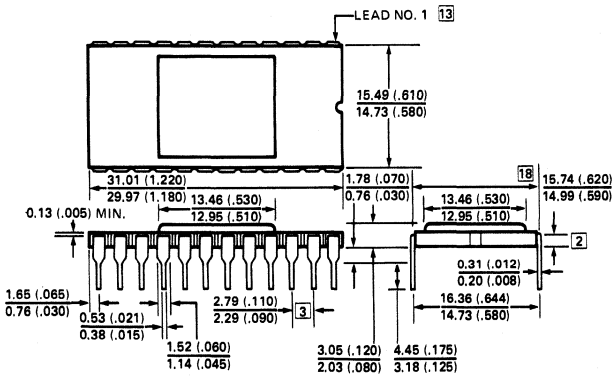
HERMETIC: Laminated Ceramic, Side Brazed Lead

IMA Package



CONSTRUCTION NOTES: 10b, 11d, 12b

INC/INH Package

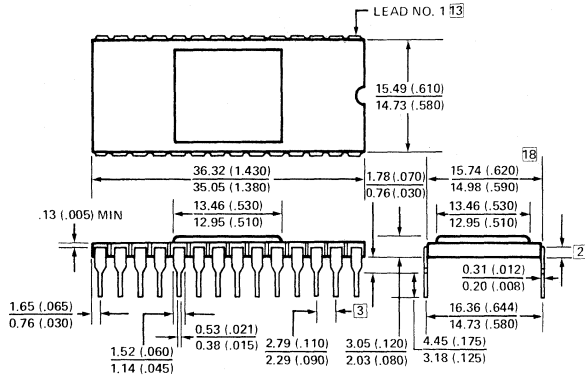


CONSTRUCTION NOTES: 10b, 11b, 12b

PACKAGES

HERMETIC: Laminated Ceramic, Side Brazed Lead (cont'd.)

IQA Package



CONSTRUCTION NOTES: 10b, 11b, 12b

Section 15 Sales Offices

Electronic components and materials for professional, industrial and consumer uses from the world-wide Philips Group of Companies

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Austria: ÖSTERREICHISCHE PHILIPS BAUELEMENTE Industrie G.m.b.H., Triester Str. 64, A-1101 WIEN, Tel. 6291 11.
Belgium: N.V. PHILIPS & MBLE ASSOCIATED, 9, rue du Pavillon, B-1030 BRUXELLES, Tel. (02) 242 74 00.
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